A Fast Built-In Sensor for CMOS Digital Applications

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Abstract — *Various testing methods have been proposed for testing digital circuits. One of those testing methods is the quiescent current testing which is now widely used due to the high fault coverage it achieves. But this method suffers from a big problem that is the voltage degradation it causes to the Circuit Under Test (CUT). In this paper, a novel built-in sensor (BIS) for digital CMOS circuit testing is proposed. The proposed BIS has no voltage degradation and it is able to detect, identify and localize both open and short circuit faults. Moreover, it has a simple realization with very small area and reaction time. PSpice simulations are made to verify that the proposed BIS can detect all short and open circuit fault cases applied to the CUT. Look-up tables are included to describe the detection and localization of all possible faults either open or short circuit faults in the given example. Also, comparison with the previous sensors is included. This BIS can be applied to any other CMOS circuit by adjusting the reference voltages it uses.*

Key Words — Digital testing – Built in Sensors – Fault detection – Catastrophic faults - Fault diagnosis

I. INTRODUCTION

Digital testing is well investigated since two decades [1-27]. The main reason for this is the ease of formulating the test generation as a mathematical problem due to the discrete signal and time values. The distinction between what does and what does not work is crisp and clear for digital circuitry.

A. Digital Testing Classification

The classification of digital testing methods is illustrated in Fig. 1. Digital testing methods are broadly classified into functional tests, design for testability and defect based tests [2]. Functional tests are further sub-divided into logic based testing and scan based testing. In logic based testing such as test pattern generation methods, input vectors are applied to the Circuit Under Test (CUT) and the logic levels at different nodes are observed for fault detection. The stuck-at fault model is generally used with this method.

A stuck-at fault is a particular fault model used by fault simulators and automatic test pattern generation (ATPG) tools to mimic a manufacturing defect within an integrated circuit. Individual signals and pins are assumed to be stuck at Logical '1', '0' and 'X'. For example, an output is tied to a logical 1 state during test generation to assure that a manufacturing defect with that type of behavior can be found with a specific test pattern. Likewise the output could be tied

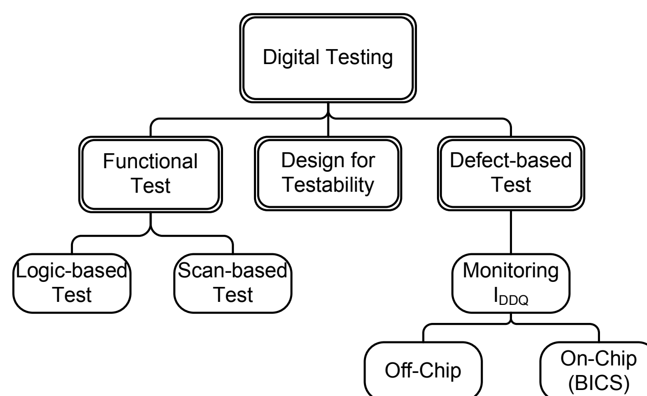


Fig. 1 The classification of digital testing

to a logical 0 to model the behavior of a defective circuit that cannot switch its output pin.

The other functional test method is the scan-based test. It has two modes of operation: normal mode and scan mode. In scan mode, input is shifted through the shift registers and observed at the output pin which has been added for the sole purpose of testing [1]. Thus additional circuitry is needed to convert circuit under test (CUT) into a shift register in scan mode.

Fault detection in high density transistor chips using functional test becomes very complex and challenging due to increase in input vectors. More over, there are many researches indicating that the functional-based testing is inadequate to explain the behavior of realistic failures in CMOS integrated circuits ICs. This is due to the unique electrical characteristics of CMOS circuits which may perform there terminal logic function in spite of the presence of some significant imperfections such as open or short circuit defects [8], [19].

The second testing methodology is the design for testability (DFT), to make the circuitry easily or better testable. The importance of this method arises with the increase in the density of transistors on a chip and complexity of the design in integrated circuits. Designers use testability measures to identify portions of a circuit that would be difficult to be tested. Such inaccessible circuits are said to have poor controllability or observability. Controllability is a measure of

the ease with which a test engineer can control signals in a circuit from the input pins. Similarly, observability is a measure of the ease of determining the behavior of a circuit from the output pins. After identifying a general section of a chip that has poor controllability or observability the engineer can then modify the circuit to be more testable [30]. The third testing method is the Defect-based test. The common application of this method is the I_{DDQ} testing [3]. I_{DDQ} stands for quiescent I_{DD}, or quiescent power-supply current. I_{DDQ} testing of CMOS ICs is shown very efficient for improving test quality. The test methodology based on the observation of quiescent current on power supply lines allows a good coverage of physical defects such as gate oxide shorts, floating gates and bridging faults, which are not very well modeled by the classic fault models, or undetectable by conventional logic tests. It is recognized as the single most sensitive test method to detect CMOS IC defects.

The major advantage of current-based testing is that it does not require propagation of a fault effect to be observed at the output; it requires only exercising the fault model and then measuring the current from the power supply. The current passing through the V_{DD} or GND terminals is monitored during the application of an input stimulus. Fully static CMOS circuits consume little power in steady state because there is no direct path between V_{DD} and ground neglecting leakage currents. If an integrated circuit draws a large amount of current under static operation it is a defective circuit. This current can be monitored using on-chip or off-chip current sensors. On-chip or Built-In Current Sensors (BICS) have speed and resolution enhancements over off-chip current sensors mainly because the large transient currents in the output drivers are by-passed and a few parasitic are encountered. On-chip current testing is both time efficient and sensitive. Moreover, on-chip current tests can also be used as an on-line testing tool, and is important when components are to be used in high reliability systems.

For high speed and high sensitivity, unaffected by large pad currents, a fast built-in current testing circuit is desired. Fig. 2 shows the block diagram of the I_{DDQ} testing with BICS. Essentially, I_{DDQ} testing technique adds a BIC sensor in series with V_{DD} or GND lines of the circuit under test. A series of input stimuli is applied to the device under test while monitoring the current of the power supply (V_{DD}) or ground (GND) terminals in the quiescent state conditions after the inputs have changed and prior to the next input change. Typically, sub-threshold current in the transistors, which are 'off' in a CMOS static circuit should be negligibly small. However, in some cases, due to charge presence in a gate oxide or latch-up, the sub-threshold current may be large enough to become an essential component of I_{DDQ}. The BICS can be designed to detect this current also.

Most of BICS detect an abnormal current by sensing a voltage drop across a sensing element. In this structure, the BICS is connected in series with the CUT and the supply current; I_{DDQ} is transformed to voltage using a resistance sensing element causing undesired degradation of the CUT supply voltage. Thus, for low voltage circuits, it is very important to minimize the voltage degradation [25]. To reduce the voltage degradation, it is better to have two modes of operation; normal and test modes. Unfortunately, these require more external pins and controlling signals and the BICS can not operate on-line [9]. Another common disadvantage exists in most of the BICS is that they can detect only short circuit faults which cause a constant current to be detected and can not detect open circuit faults.

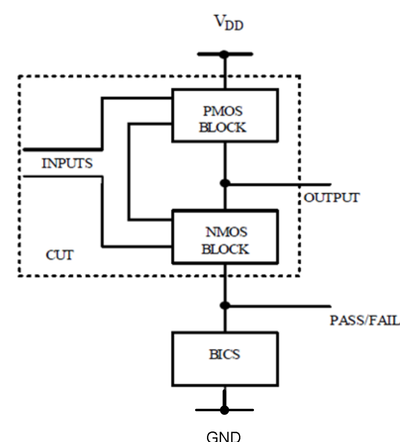


Fig. 2 Block diagram of BICS testing

A. B. Fault Definition and Fault Categories

In the context of fault diagnosis, a fault is understood as any kind of malfunction in the system that leads to an unacceptable anomaly in the overall system performance. A fault in a system can be very costly in terms of loss of production, equipment damage and economic setback. Faults are developed in a system due to normal wear and tear, design or manufacturing defects or improper operation leading to stress beyond endurable limits and also is subject to blemishes and imperfections. These imperfections may cause either catastrophic failure in the operation of any individual IC or minor variations in the performance from one IC to the next.

The faults causing catastrophic failures are called catastrophic faults or hard faults such as open nodes, shorts between nodes, and other topological changes in a circuit caused due to dust particles, over etching or extra metal extensions which join the lines [2]. On the other hand parametric faults or soft faults refer to any change in the value of an element with respect to its nominal value outside the tolerance limits, without affecting its connectivity. These faults cause minor variation in performance. According to the number of faults, faults in analog circuits are often categorized into two types: single fault and multiple faults. The number of single faults in electronic devices accounts for 70 – 80 percent of total faults [29]. The classification of faults is shown in Fig. 3. In digital circuits, the catastrophic faults are dominant faults, due to the nature of the digital circuits.

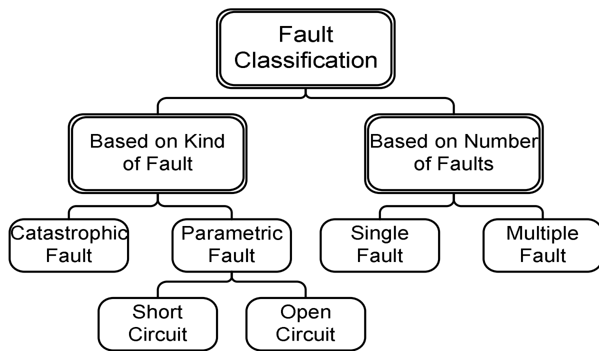


Fig. 3 The Classification of Faults

In this study we choose the short and open fault model of CMOS transistor as in [18]. Open faults are hard faults in which the component terminals are out of contact with the rest of the circuit creating a high resistance at the incidence of fault in the circuit. Addition of a combination of high resistance in parallel with a small capacitor, in series (e.g., R_{open}=1MΩ and C_{open}=1fF) with the component can simulate the open faults. Short faults, on the other hand, are a short between terminals of the component (effectively shorting out the component from the circuit). A small resistor in parallel (e.g., R_{short} =100 Ω) with the component can simulate this type of fault. It is worth noting that the catastrophic fault model considered here does not include shorts between the gate and the source or drain of the transistors, or opens in the gate contacts. Also, it has been considered that all the faults have the same probability of occurrence. Tests can be classified into three tasks as described in Fig. 4. They are fault detection, fault location or fault prediction. In the manufacturing process or during maintenance, a quick check is needed to pass the good parts and reject the bad parts for maximum product throughput. So, only fault detection is needed to evidence the faults.

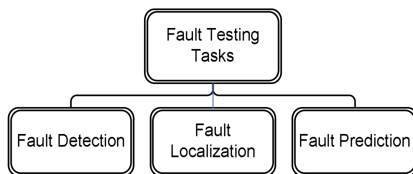


Fig. 4 The classification of fault testing

At other times, fault location is needed to detect failed modules or components for repair. The third task of fault testing is the fault prediction which is used mainly with highly reliable products or safety related products. Fault prediction continuously monitors the circuit under test to identify whether any of its elements are about to fail allowing for a preventive repair. The choice between fault location and fault detection calls for a compromise. Fault location needs better isolation of the components and provides better test coverage. It may be used during both production and repair, but it may slow down the testing process and the throughput. In order to locate every fault, most nodes need to be accessed in the circuit, a requirement that may be impossible to meet in modern fabrication process [1].

The objective of this paper is to produce testing scheme for digital circuits, this scheme can be classified under defect-based test but it overcome most of the disadvantages of the BICS method. The paper is organized as follows: the next section provide a fast survey for the existed BICS. Section III propose the new Built in Sensor (BIS) scheme with the aid of simulation results. A 4x4 multiplier circuit is tested with the proposed BIS in Section IV. Then, a comparison between the proposed BIS and the existed BICS is presented in Section V. Finally, the work is concluded and future work is suggested in Section VI.

II. A Survey on BICS

Recent research has been devoted to the development of effective BICS and several schemes have been proposed [2-24]. Table I compares among BICS which are designed for digital CMOS circuits. The big problem exists in most of the BICS designs is the performance degradation imposed on the CUT. Typical BICS has a sensing element that is inserted in series with either the V_{DD} or GND bus of the CUT. This sensing element may be a MOS transistor operating in the linear region [17, 23], a diode-connected MOS transistor [11, 13, 14, 20, 24], a diode-connected bipolar transistor [5, 6, 7, 22], a resistor [9, 16], or a parallel combination of a transistor and diode to limit the voltage drop across the sensing element [8, 10, 12, 15]. Duo to the voltage drop across such sensing element and increased parasitic load, significant performance degradation of the CUT is gained [21]. The voltage degradation is reduced in [21] thanks to the use of a voltage regulator to regulate the supply voltage of the CUT to compensate the varying load voltage. On the other hand, the BICS designed in [9] employs an op-amp as its current supply device. Using this scheme, the performance degradation can be minimized by adjusting the circuit parameters in the BICS to allow the CUT to have the same V_{DD} and GND levels as originally intended. The voltage degradation is reduced in the BICS design found in [15] using a sensing element consists of a parallel combination of MOS transistor and a diode driven by two additional different power supplies. Another simple method to overcome the voltage degradation problem is to employ two modes of operation for the BICS; the normal mode and the test mode. In the normal mode of operation, the BICS is isolated from the CUT and the CUT is connected directly to the supply voltage and GND. In the test mode, the sensing element is inserted in series with the CUT through the V_{DD} or GND bus. The disadvantage of this method is using external bins and that the BICS can not operate on-line in this case [24]. About the ability to detect faults, most of the BICS are able to detect short circuit faults [5-9, 11-16, 20, 21, 23, 24]. However, few BICS are designed to detect open circuit faults [22]. Moreover, the BICS that are able to detect open and short faults cannot define the fault type (short or open)

[10]. Another disadvantage in some of the BICS designs is the need for clock schemes [5-8, 10-14].

TABLE I
A COMPARISON AMONG RECENT BICS DESIGNED FOR CMOS DIGITAL CIRCUITS.

REF.	Sensing Element	Voltage Degradation	Using Ref. current	Type of detected fault		Using clock scheme
				Short circuit	Open circuit	
[5], [6] [7]	Diode-connected BJT transistor	Exists	Yes	Yes	No	Yes
[8] [12]	NMOS in linear region parallel with diode	Exists	Yes	Yes	No	Yes
[9]	Resistor	Reduced using op-amp to adjust the supply of CUT	No	Yes	No	No
[10]	NMOS in linear region parallel with diode	Exists	Yes	Yes	Yes	Yes
[11]	Diode-connected NMOS transistor	Exists	No	Yes	No	Yes
[13]	Diode-connected NMOS transistor	Exists	Yes	Yes	No	Yes
[14]	Two diode-connected transistors connected in series	Exists	No	Yes	No	Yes
[15]	PMOS in linear region parallel with diode	Reduced due to using more than one supply voltage	No	Yes	No	No
[16]	Resistor	Exists	Yes	Yes	No	Yes
[20]	Diode-connected NMOS transistor	Exists	No	Yes	No	No
[21]	NMOS pass transistor	Reduced due to using voltage regulator	No	Yes	No	Yes
[22]	Diode-connected BJT transistor	Exists	Yes	No	Yes	No
[23]	NMOS transistor in linear region	Exists in both modes	No	Yes	No	No
[24]	Diode-connected NMOS transistor	Nearly zero due to using two modes of operation	Yes	Yes	No	No

III. THE PROPOSED BUILT-IN SENSOR

From the previous survey, one can conclude that disadvantages exist in the BICS can be summed up as follows:

1. supply voltage degradation caused by the voltage drop on the sensing element.
2. extra control pins utilized for multimode of operation.
3. detecting of short circuit faults only that cause abnormal current to follow from the supply to GND.

The configuration of the proposed technique using the Built In Sensor (BIS) is shown in Fig. 5. The proposed BIS overcomes all the above problems, it has nearly zero voltage degradation because it does not test the I_{DDQ} current. Instead, it tests the internal node voltages of the CUT. So, it does not use a sensing element and thus, it can operate on line. It can also detect open and short circuit faults, define the fault type and locate it. Moreover, it has a simple and compact structure and does not use any current source references. The proposed BIS is designed to test circuits which operate in frequencies in the range of tens of MHz. In this range of frequencies, when

an open circuit exists in the PMOS (NMOS) network, it cuts the path to the supply voltage (ground). So, due to the existence of parasitic capacitances, the internal voltage node is decreased (increased) by few of mV, and it depends on the previous value stored before in this node. If the previous voltage is zero, the internal node voltage at the existence of open circuit error will drop below (be above) the zero by tens of mV, and if the previous voltage is logic high, the internal node voltage will drop below (be above) the V_{DD} by tens of mV. In case of short circuit fault, the internal nodes have a voltage smaller than V_{DD} or greater than GND by hundreds of mV based on the location of the fault.

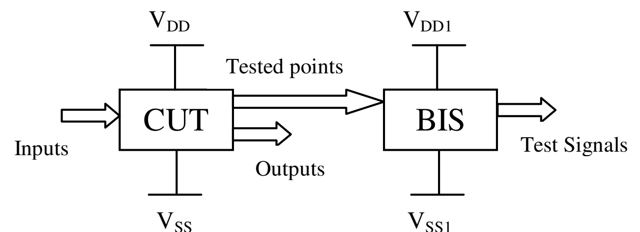


Fig. 5 The block diagram of the new BIS topology

A. The structure of the proposed BIS:

The structure of the proposed BIS is shown in Fig. 6. The proposed BIS structure is composed of two parts; the upper part which generates the signal Pass/Fail1, checks on the existence of short circuit fault. The lower part is designed to detect open circuit faults with the output signal: PasslFail2.

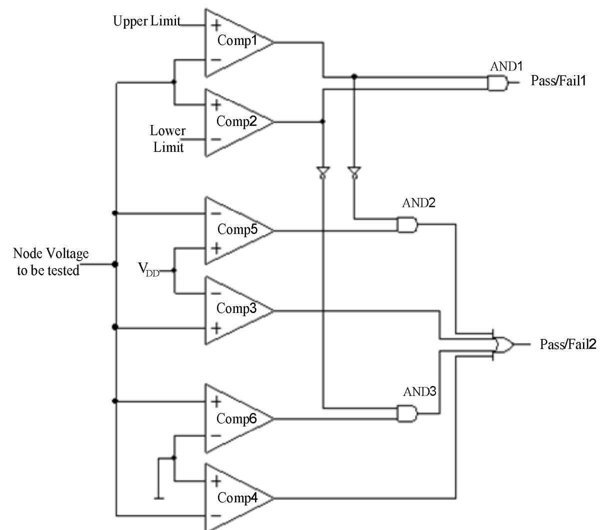


Fig. 6 The structure of the proposed BIS

To simplify the operation of the proposed circuit, the available ranges of the internal node voltage is shown in Fig. 7. There is one range for the short circuit fault which is between the Lower and Upper limits and is detected by the

AND operation between the output of Comparator1 and Comparator2 to produce the signal Pass/Fail1. The open circuit fault has four ranges; below the logic low, above logic low and below the lower limit, above the upper limit and below logic high and above logic high. So, Pass/Fail2 signal should be designed to detect any open circuit fault exist in one of the previous explained four ranges. Pass/Fail2 is the output of OR function between four input signals. Each input signal tests on the existence of the internal node voltage to be in one of the four ranges. The first one is the output of AND2 which tests the existence of the internal voltage in the third open circuit fault range. The second input to the OR gate is the output of Comparator3 which check on the existence of the tested voltage in the fourth open circuit faulty range. The third input to the OR gate is the output of AND3 which tests the internal voltage to be in the second open circuit fault range. The last input to the OR gate is the output of Comparator4 which indicate the existence of the internal voltage in the first open circuit faulty range.

B. Simulation results for the proposed BIS

In order to verify the performance of the proposed BIS, it is used to test a CMOS adder circuit, which is shown in Fig. 8. It is worth noting that this circuit is used before as the CUT in [24]. It consists of three digital inputs; A, B and C and two outputs (Carry and Sum). Assuming the output stages (M25→M28) are fault-free, which is a reasonable assumption since if the output stage is faulty; it is impossible to detect any fault. Then, two internal voltages V_C and V_S are selected as the testing points for each adder. It is clear that they are the inversion of the outputs, so testing of these two internal voltages are equivalent to testing the two outputs under the previous assumption. The logic expressions for both internal nodes V_C and V_S are shown in Equations (1) and (2) respectively.

$$V_C = \overline{AB} + \overline{BC} + \overline{AC} \quad (1)$$

$$V_S = \overline{ABC} + AC\overline{B} + AB\overline{C} + \overline{A}BC \quad (2)$$

The CUT operates with supply voltage of 3V. Table II shows the aspect ratios for the transistors of the CUT. To determine the upper and lower limits for Comparator1 and Comparator2, one should analyze the adder circuit for all cases of short circuit faults.

The upper (lower) limit can be calculated by analyzing all short circuit states in the PMOS (NMOS) network and find the maximum (minimum) value of the internal node voltages. The selected upper and lower limits are 2.6V and 160mV respectively taking into consideration 10% variations in the power supply and temperature. The structures of the six comparators used in the BIS are shown in Fig. 9. Also, the aspect ratios for the MOS transistors used in the comparators are given in Table III.

	0V		Lower Limit		Upper Limit	3V	Volts
		Range of logic Low				Range of logic High	
Type of Fault	O.C in PMOS network		O.C in NMOS network	S.C in PMOS or NMOS networks	O.C in PMOS network		O.C in NMOS network
Realized by:	Comp 4		(Comp 6) AND (the INV of Comp 2)	Comp 1 AND Comp 2	(Comp 5 AND (the INV of Comp 1)		Comp3

Fig. 7 The available ranges for the internal node voltage

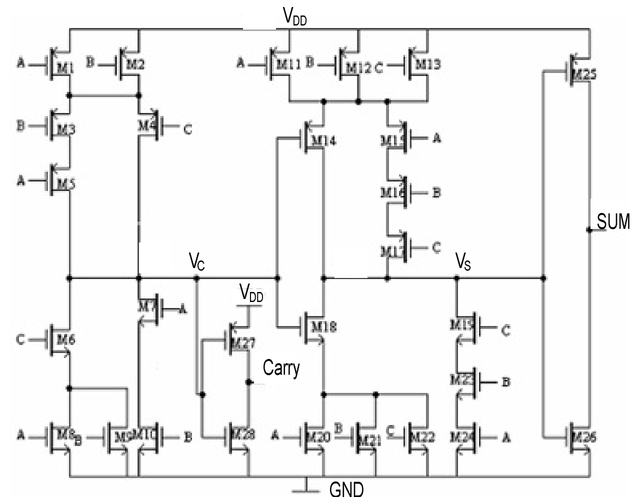


Fig. 8 A CMOS adder circuit used as the CUT [24].

To detect all faults, the three inputs of the CUT; A, B and C should be traced for all cases. The input configurations used are shown in Table IV. Fig. 10 shows the two output signals Pass/Fail1 and Pass/Fail2 along with the two internal node voltages V_C and V_S in case of fault free CUT. However, Fig. 11 shows the case of a short circuit fault in the PMOS network between the source and drain of M11. This fault causes the voltage V_S to drop to 2.16V in the period from 210nsec to 240nsec and hence, the Pass/Fail1 signal can detect the short circuit fault after 1.2nsec. Fig. 12 shows the case of open circuit fault in the NMOS network at the drain of M8. This fault appears in the periods; from 150nsec to 160nsec, from 200nsec to 210nsec and from 280nsec to 300nsec.

TABLE II
THE ASPECT RATIOS FOR TRANSISTORS IN THE CUT

The MOS transistor	The aspect ratio W/L
All PMOS transistors	2/0.25
All NMOS transistors	1/0.25

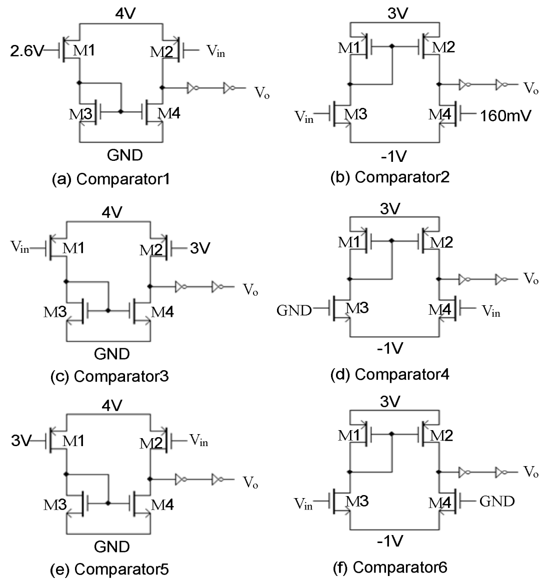


Fig. 9 The CMOS realization of the comparators used in the BIS

TABLE III

THE ASPECT RATIOS FOR TRANSISTORS IN THE COMPARATORS

The Comparator	The MOS transistor	The aspect ratio W/L
Comparator1	M1, M2	2/0.5
	M3,M4	1.25/0.25
Comparator2	M1, M2	1.75/0.25
	M3,M4	1.75/0.25
Comparator3	M1, M2	2/0.25
	M3,M4	1/0.5
Comparator4	M1, M2	1.5/0.5
	M3,M4	1/0.25
Comparator5	M1, M2	2.5/0.25
	M3,M4	1.25/0.25
Comparator6	M1, M2	1.75/0.5
	M3,M4	1.5/0.25

TABLE IV

ALL INPUT CONFIGURATIONS TO TEST THE CUT

Input Configuration	Time Duration (nsec)	Interval Number
000	0-40	1
100	40-70	2
110	70-80	3
010	80-120	4
110	120-140	5
100	140-150	6
101	150-160	7
001	160-200	8
101	200-210	9
111	210-240	10
011	240-280	11
101	280-300	12
100	300-320	13
000	320-360	14

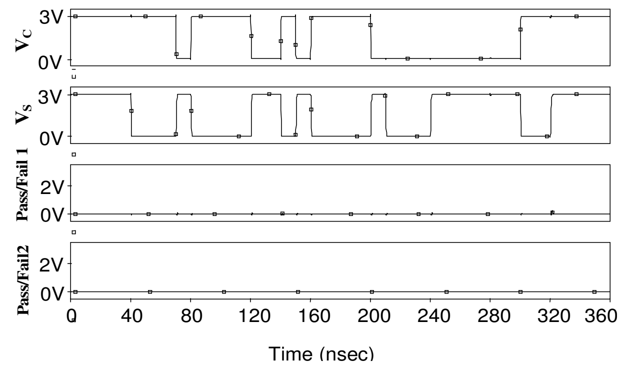


Fig. 10 The internal voltages V_C and V_S along with the signals Pass/Fail1 and Pass/Fail2 in case of fault-free CUT

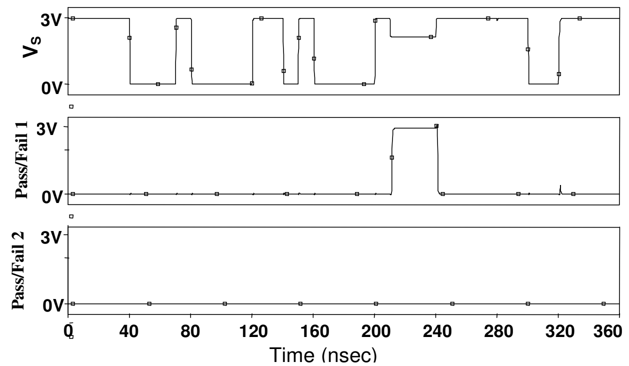


Fig. 11 The internal voltage V_S along with the two signals Pass/Fail1 and 2 in case of short circuit fault on M11 in the CUT

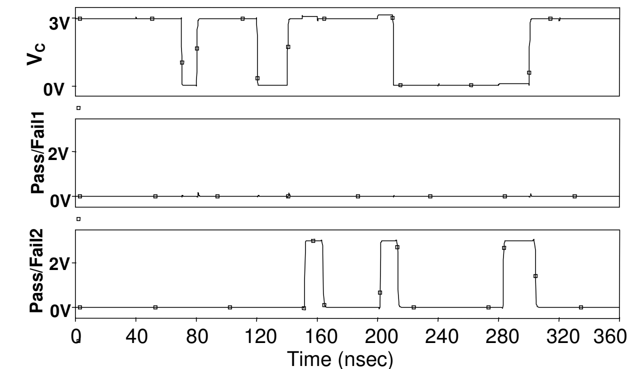


Fig. 12 The internal voltage V_C along with the two signals Pass/Fail1 and 2 in case of open circuit fault at the drain of M8 in the CUT.

The voltage V_C goes above the supply voltage by 115mV in the first period and goes above the supply voltage by 171mV in the second period. In the third period, it goes above the zero by 61mV. Hence, the Pass/Fail2, can detect the open circuit fault in the three periods. It is worth noting that the BIS has nearly no impact on the CUT voltages.

Fig. 13 simulates the difference between the internal node voltages V_C and V_S with and without connecting the BIS. It is clear that no DC difference value of both cases. In Fig. 13(a), the difference between the values of V_C with and without the BIS has a max delay of 1.5nsec. The difference between the values of V_S with and without the BIS is shown in Fig. 13(b) with a max delay of 1nsec.

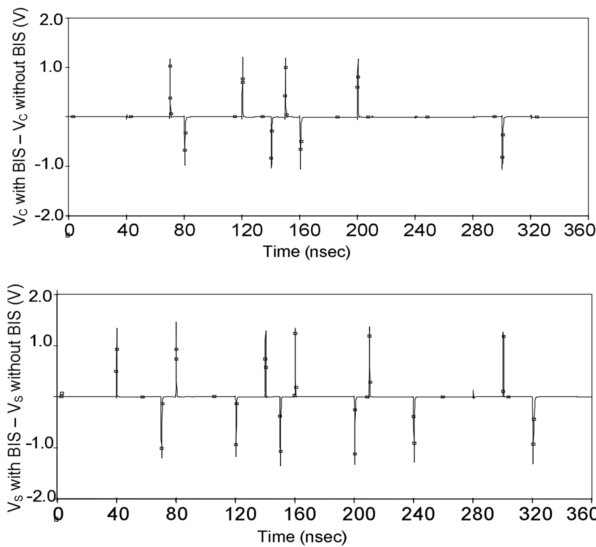


Fig. 13 The difference between internal node voltages V_C and V_S with and without the BIS

All possible short and open circuit fault cases in the full adder circuit are traced in Tables V, VI, VII and VIII. Tables V and VI show the values of node voltages; V_C and V_S at all cases of drain-source short circuit. The number of tested cases is 53. It is worth noting that the values of the internal node voltages in these tables are the same for the absence or presence of the BIS which prove that the proposed BIS has no impact on the CUT. It is worth noting also that all cases of short circuit faults can be detected by the proposed BIS. Another observation is that the value of the faulty voltage, in case of short circuit is ranged between 170mV to 2.48V. This value depends on the supply voltage of the CUT, the transistors exist in the faulty path, and the model used for the MOS transistors. A problem extracted from Table V is that when there is a short circuit fault in the PMOS network connected to V_C node, it affects the value of the node voltage V_S. This is what we know by "fault propagation". This may cause a problem in the diagnostic of error (open or short circuit), and in localizing the error (connected to V_C node or V_S node). So, the nodes should be tested in sequential order not simultaneously. And then, one should find the first stage that has a fault to diagnose and locate the fault correctly. This problem does not appear in testing the node voltage; V_S, as it is clear in Table VI, because there is no feedback from the second stage, connected to V_S node, and the first stage, connected to V_C node. And so, any fault exists in the second stage does not affect the first one. Note that only the abnormal values of node voltages are written in the tables and the symbol “-” means that this value is normal (0 or 3V).

TABLE V
VALUES OF V_C AND V_S FOR ALL CASES OF DRAIN-SOURCE SHORT CIRCUIT IN THE NETWORK CONNECTED TO V_C

Shorted MOS Transist-or	Case No.	Interval No.	V_C (V)	Detection		V_S (V)	Detection	
				Pass/ Fail1	Pass/ Fail2		Pass/ Fail1	Pass/ Fail2
M1	1	3	1.8	1	0	107m	0	1
	2	5	1.8	1	0	107m	0	1
M2	3	3	1.8	1	0	107m	0	1
	4	5	1.8	1	0	107m	0	1
M3	5	11	747m	1	0	2.85	0	1
M4	6	7	1.8	1	0	106m	0	1
	7	9	1.8	1	0	106m	0	1
	8	11	1.8	1	0	106m	0	1
M5	9	7	750m	1	0	2.85	0	1
	10	9	750m	1	0	2.85	0	1
	11	11	750m	1	0	2.85	0	1
	12	12	750m	1	0	2.85	0	1
M6	13	2	363m	1	0	-	0	0
	14	4	363m	1	0	-	0	0
	15	6	363m	1	0	-	0	0
	16	13	363m	1	0	-	0	0
M7	17	4	363m	1	0	-	0	0
M8	18	8	282.7 m	1	0	-	0	0
M9	19	8	282.7 m	1	0	-	0	0
M10	20	2	363m	1	0	-	0	0
	21	6	363m	1	0	-	0	0
	22	13	363m	1	0	-	0	0

TABLE VI
VALUES OF V_S FOR ALL CASES OF DRAIN-SOURCE SHORT CIRCUIT IN THE NETWORK CONNECTED TO V_S

Shorted MOS Transistor	Case No.	Interval No.	V_S(V)	Detection	
				Pass/Fail1	Pass/Fail2
M11	23	10	2.16	1	0
M12	24	10	2.16	1	0
M13	25	10	2.16	1	0
M14	26	2	2.48	1	0
	27	4	2.48	1	0
	28	6	2.48	1	0
	29	8	2.48	1	0
	30	13	2.48	1	0
M15	31	2	575m	1	0
	32	6	575m	1	0
	33	13	575m	1	0
M16	34	4	575m	1	0
M17	35	8	575m	1	0
M18	36	3	170m	1	0
	37	5	170m	1	0
	38	7	170m	1	0
	39	9	170m	1	0

	40	11	170m	**1**	0
	41	12	170m	**1**	0
M19	42	3	753m	**1**	0
	43	5	753m	**1**	0
M20	44	1	205m	**1**	0
	45	14	205m	**1**	0
M21	46	1	205m	**1**	0
	47	14	205m	**1**	0
M22	48	1	205m	**1**	0
	49	14	205m	**1**	0
M23	50	7	753m	**1**	0
	51	9	753m	**1**	0
	52	12	753m	**1**	0
M24	53	11	753m	**1**	0

All open drain and source cases are studied in Tables VII and VIII. The number of studied cases is the 93 case. It is obvious from those tables that the values of the internal voltages in case of open circuit fault varies depend on whether the BIS is connected to the CUT or not. The reason of this varying is that the value of the internal node voltage, in case of open circuit fault, depends on the parasitic capacitance connected to this node. Generally, when the open circuit fault occurs in the PMOS network, the internal node voltage decreases below its previous value and when the open circuit occurs in the NMOS network, the internal node voltage increases over its previous value.

TABLE VII
VALUES OF V_C FOR ALL CASES OF DRAIN AND SOURCE OPEN CIRCUIT WITH AND WITHOUT CONNECTING THE BIS

Place of O.C	Case No.	Interval No.	V_C without BIS (V)	V_C with BIS (V)	Pass/ Fail1	Pass/ Fail2
Source of M1	1	4	-17m	-37m	**0**	**1**
Source of M2	2	2	3.09m	3.07	**0**	**1**
	3	6	-50m	-22m	**0**	**1**
	4	13	525m	103m	**0**	**1**
Source of M3	5	8	-218m	-130m	**0**	**1**
Source of M4	6	2	2.87	2.99	**0**	**0**
	7	4	-15m	-44m	**0**	**1**
	8	6	-28m	-17m	**0**	**1**
	9	13	-119m	-80m	**0**	**1**
Source of M5	10	8	-222m	-130m	**0**	**1**
Drain of M5	11	8	-130m	-84m	**0**	**1**
Drain of M4	12	2	2.8	2.99	**0**	**0**
	13	4	-25m	-41m	**0**	**1**
	14	6	-25m	-16m	**0**	**1**
	15	13	-34m	-35m	**0**	**1**
Drain of	16	7	3.23	3.1	**0**	**1**
M6	17	9	3.33	3.17	**0**	**1**
	18	11	600m	160m	**0**	**1**
	19	12	462m	202m	**1**	**0**
Source of M6	20	7	3.3	3.13	**0**	**1**
	21	9	3.3	3.17	**0**	**1**
	22	11	512m	156m	**0**	**1**
	23	12	382m	200m	**1**	**0**
Drain of M7	24	3	3.23	3.17	**0**	**1**
	25	5	3.23	3.22	**0**	**1**
Source of M7	26	3	3.33	3.17	**0**	**1**
	27	5	3.32	3.24	**0**	**1**
Drain of M8	28	7	3.24	3.11	**0**	**1**
	29	9	3.31	3.16	**0**	**1**
	30	12	161m	64m	**0**	**1**
Source of M8	31	7	2.91	3.01	**0**	**1**
	32	9	3.33	3.16	**0**	**1**
	33	12	244m	104m	**0**	**1**
Drain of M9	34	11	481m	138m	**0**	**1**
Source of M9	35	11	402m	129m	**0**	**1**
Source of M10	36	3	3.34	3.17	**0**	**1**
	37	5	3.34	3.24	**0**	**1**

The above note can be applied for all cases except for cases (2, 4, 40, 41, 43, 46, 47, 48 and 49) in the PMOS network and cases (74, 79, 83, 84, 86, 87, 89 and 91) in the NMOS network.

There are only five cases of ninety three one that can not be detected by the proposed BIS. Those cases are (6, 12, 50, 72 and 77). This is because in those cases, the node voltage varies from the normal voltage (0 or 3V) by very small value; less than 15mV which is much closed to the accuracy of the comparators used in the BIS. So, the comparators can not catch these small differences. But fortunately, the first two cases are open source and drain of M4 which can be detected in the other three periods. Also, the third case belongs to open circuit fault at the drain of M14 which also can be detected in the other five periods.

TABLE VIII
VALUES OF V_S FOR ALL CASES OF DRAIN AND SOURCE OPEN CIRCUIT WITH AND WITHOUT CONNECTING THE BIS

Place of O.C	Case No.	Interval No.	V_S without BIS (V)	V_S with BIS2(V)	Pass /Fail1	Pass /Fail2
Drain of M11	38	11	-58m	-18m	0	1
Source of M11	39	11	55m	-23m	0	1
Drain of M12	40	7	493m	165m	0	1
	41	9	517m	140m	0	1
	42	12	2.74	2.93	0	1
Source of M12	43	7	1	375m	1	0
	44	9	1	368m	1	0
	45	12	2.46	2.8	0	1
Drain of M13	46	3	535m	107m	0	1
	47	5	513m	111m	0	1
Source of M13	48	3	1	326m	1	0
	49	5	1	350m	1	0
Drain of M14	50	3	19m	1.74m	0	0
	51	5	-50m	-29m	0	1
	52	7	-24m	-6m	0	1
	53	9	-65m	-29m	0	1
	54	11	-55m	-24m	0	1
	55	12	-97m	-60m	0	1
Source of M14	56	3	-80m	-40m	0	1
	57	5	-190m	-71m	0	1
	58	7	-125m	-7m	0	1
	59	9	-156m	-80m	0	1
	60	11	-58m	-24m	0	1
	61	12	-99m	-58m	0	1
Source of M15	62	1	2.93	2.93	0	1
	63	14	-53m	-17m	0	1
Source 0f M16	64	1	2.93	2.93	0	1
	65	14	-26m	-17m	0	1
Drain of M17	66	1	2.93	2.93	0	1
	67	14	-28m	-21m	0	1
Source of M17	68	1	2.93	2.93	0	1
	69	14	-26m	-19m	0	1
Drain of M18	70	2	3.16	3.06	0	1
	71	4	3.14	3.04	0	1
	72	6	3.07	2.99	0	0
	73	8	3.16	3.04	0	1
	74	13	3.03	2.94	0	1
Source of M18	75	2	3.17	3.07	0	1
	76	4	3.18	3.06	0	1
	77	6	3.1	3.003	0	0
	78	8	3.2	3.06	0	1
	79	13	3.06	2.97	0	1
Drain of M19	80	10	3.24	3.1	0	1
Source of M19	81	10	3.25	3.1	0	1
Drain of M20	82	2	3.16	3.07	0	1
	83	6	3.007	2.96	0	1
	84	13	2.95	2.92	0	1
Source of M20	85	2	3.16	3.06	0	1
	86	6	2.8	2.89	0	1
	87	13	2.7	2.84	0	1
Drain of M21	88	4	3.07	3.01	0	1
Source of M21	89	4	2.8	2.93	0	1
Drain of M22	90	8	3.08	3.007	0	1
Source of M22	91	8	2.7	2.92	0	1
Source of M23	92	10	3.24	3.1	0	1
Source of M24	93	10	3.24	3.1	0	1

The last two cases appear when there is open circuit fault at the drain and source of M18, respectively. This fault also can be detected in the other four periods.

Another note extracted from Table VII and Table VIII is that there are six cases which are wrongly diagnosed by the BIS as short circuit faults whereas they are open circuit ones. Those cases are (19, 23, 43, 44, 48 and 49). Case 19 and 23 represent open circuit at the drain and source of M6 respectively. Fortunately, these two faults can be detected correctly in the other three input configurations. So, the detection percentage in those cases is 75%. The next two cases; 43 and 44, belong to open circuit fault at the source of M12. The detection percentage in this case is 33%. The last two cases are for open circuit fault at the source of M13, unfortunately, this fault cannot be detected as open circuit fault.

Note that for the adder configuration used here, there are eighteen short circuit cases which represent number of parallel branches in this circuit. Also, there are eighteen open circuit case that represent number of series branches in the adder circuit.

All those cases are tested by the proposed BIS and they are all detected. The simulation results for all the short and open circuit cases are summed up in Tables IX and X respectively. From those tables, we can conclude that each open or short circuit case is happen at a specific input configuration or on a specific input transition. Thus, using the look-up tables IX and X, the proposed technique has the ability to detect the location of the maximum possible number of equivalent faulty groups which are 36 for both the short and open circuit cases in a specific adder circuit, if we know the tested node and the input configuration at the fault case.

TABLE IX
ALL INPUT CONFIGURATIONS ALONG WITH SHORTED TRANSISTORS

Input Configuration ABC	BIS connected to V_C	BIS connected to V_S
000	-	M20, M21 OR M22
001	M8 OR M9	M17
010	M7	M16
011	M3	M24
100	M10	M15
101	M5	M23
110	M1 OR M2	M19
111	-	M11, M12 OR M13
010, 100	M6	-
011, 101	M4	-
001, 010, 100	-	M14
011, 101, 110	-	M18

IV. CASE STUDY

One of the famous digital testing circuits is the multiplier circuit. Here, the proposed BIS is used to test a 4x4 multiplier circuit, shown in Fig. 14 [30]. This circuit consists of 12 adder circuit. The CMOS realization of the adder circuit used is the same which was tested before and is shown in Fig. 8. The CUT operates with supply voltage of 3V. Simulations are done using Cadence PSpice program with 0.25µm MOS model.

TABLE X
ALL INPUT CONFIGURATION TRANSITIONS ALONG WITH FAULTY TRANSISTORS FOR ALL OPEN CIRCUIT CASES

Input Transition	BIS connected to V_C	BIS connected to V_S
110→010	M1	M21
101→001	M3 OR M5	M22
111→011	M9	M11
100→000	-	M15, M16 OR M17
101→111	-	M19, M23 OR M24
100→110, 010→110	M7 OR M10	M13
000→100, 110→100 101→100	M2	M20
100→101, 001→101 011→101	M8	M12
000→100, 110→010 110→100, 101→100	M4	-
100→101, 001→101 111→011, 011→101	M6	-
000→100, 110→010, 101→100 101→001	-	M18
100→101, 001→101 111→011, 011→101 100→110, 010→001	-	M14

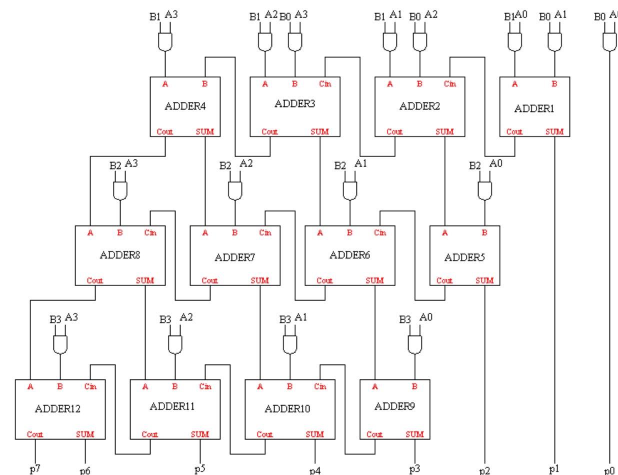
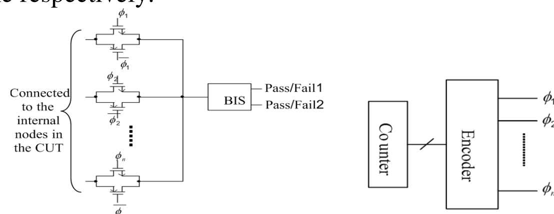


Fig. 14 The 4x4 multiplier circuit used as CUT [30]

In the selected CUT, there are 24 nodes to be tested using the BIS; two nodes for each adder circuit. The configuration of connecting the CUT with the BIS is shown in Fig. 15. In this configuration, each internal node is connected to the BIS through a transmission gate which is controlled by an encoder circuit. A counter is connected to the input of the encoder to decide which internal node to be connected to the BIS and so, to be tested. So, all internal nodes of the CUT can be tested on-line respectively.



(a) (b)

Fig. 15 The configuration used to connect all internal nodes in the CUT to the BIS; (a) connecting to the internal nodes, and (b) generating control signals for the transmission gates

The clock frequency of the CUT is 20MHz and the selected clock frequency of the testing scheme is 5MHz. This means that the testing phase for each internal node is 0.2µ seconds. The testing time is illustrated in Table XI. Fig. 16 shows the two output signals Pass/Fail1 and Pass/Fail2 along with the input of the BIS in case of fault free CUT. Two independent faults are injected to the CUT: a short circuit fault on M20 in the sixth adder circuit and an open drain in M18 in the seventh adder circuit. Fig. 17 shows the case where Pass/Fail1 detects the short circuit fault whereas the open circuit fault is detected by Pass/Fail2 and shown in Fig. 18.

TABLE XI
THE TIMING SCHEDULE FOR TESTING THE 4X4 MULTIPLIER CIRCUIT

The tested ADDER	Time period for testing V_C (µsec)	Time period for testing V_S (µsec)
ADDER1	0.0:0.2	0.2:0.4
ADDER2	0.4:0.6	0.6:0.8
ADDER3	0.8:1.0	1.0:1.2
ADDER4	1.2:1.4	1.4:1.6
ADDER5	1.6:1.8	1.8:2.0
ADDER6	2.0:2.2	2.2:2.4
ADDER7	2.4:2.6	2.6:2.8
ADDER8	2.8:3.0	3.0:3.2
ADDER9	3.2:3.4	3.4:3.6
ADDER10	3.6:3.8	3.8:4.0
ADDER11	4.0:4.2	4.2:4.4
ADDER12	4.4:4.6	4.6:4.8

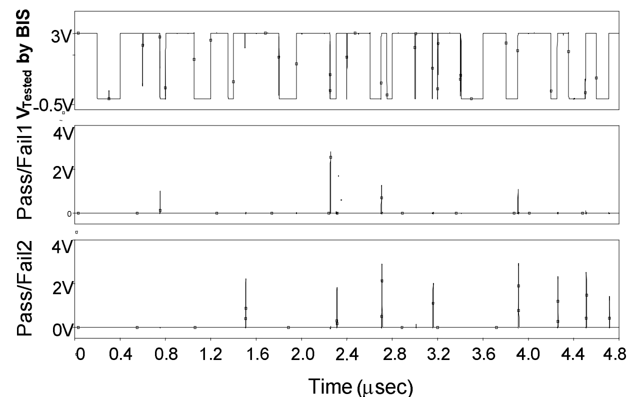


Fig. 16 The input voltage of the BIS along with the signals Pass/Fail1 and Pass/Fail2 in case of fault-free CUT

To localize the fault, this can be done through two levels; first, determine the defected adder. Second, localize the defected transistor in this adder. The first level is easily achieved by knowing the period in which the fault is detected. (make sure that there is no other defected adders before this period). Then, use Table XI to localize the defected adder circuit and the defected part in it (by knowing the tested node; V_C or V_S). The second level is achieved by the following steps; for the defected adder, disconnect its inputs from the CUT and use a shift register to trace all possible input configurations. Then, use the look-up tables: Tables IX and X to locate the fault in this adder circuit. The localization scheme is illustrated in Fig. 19.

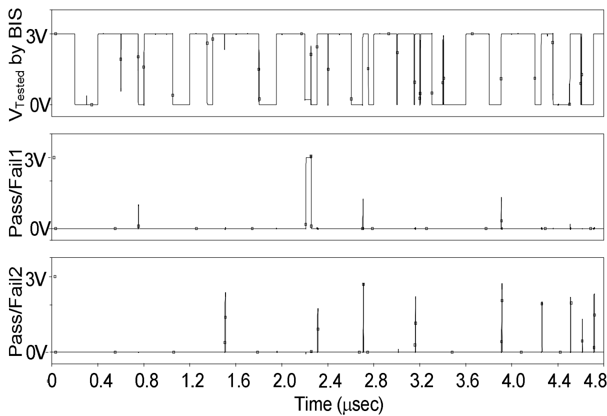


Fig. 17 The input voltage of the BIS along with the two signals Pass/Fail1 and 2 in case of short circuit fault between source and drain of M20 in ADDER6

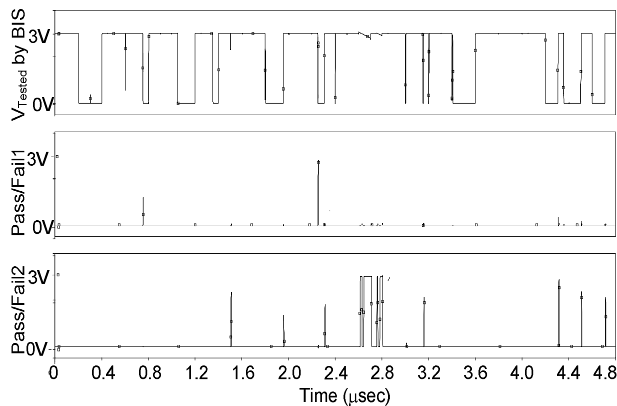


Fig. 18 The input voltage of the BIS along with the two signals Pass/Fail1 and 2 in case of open circuit fault at the drain of M18 in ADDER7

To localize the short circuit fault of Fig. 17, it is clear that this fault is detected in the period from 2.2:2.4 μsec. So, with the aid of Table XI, one can know that this fault exists in the network connected to node V_S in ADDER6. Then, the shift register is connected to the inputs of this adder circuit and all input configurations are traced to localize the fault. The traced inputs along with the signal Pass/Fail1 are shown in Fig. 20. It is obvious that the short circuit fault appears at the input configuration 000. Then, using Table IX, one can find that this fault represents a short circuit on M20, M21 or M22. Using the same methodology explained above, the detected open circuit fault shown in Fig. 18 can be localized. First, this fault is detected in the period 2.6:2.8 μsec which means that the defected transistor exists in the network connected to node V_S in the ADDER7 circuit. Second, the input of this adder is disconnected and a shift register is connected, instead of it, to trace all possible input configurations. Fig. 21 shows the applied input configuration along with the Pass/Fail2 signal. With the aid of this Figure and Table X, one can locate the open circuit fault at source or drain of M18.

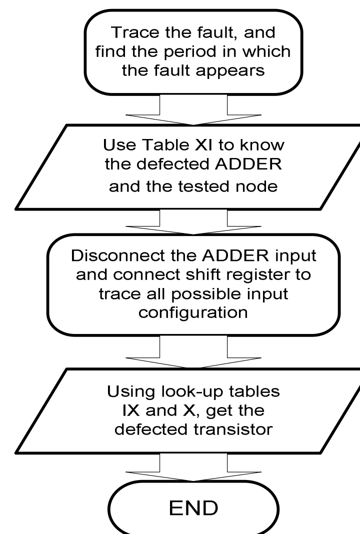


Fig. 19 The fault localization flowchart

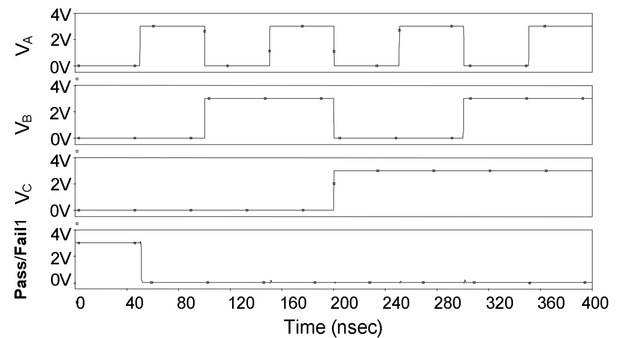


Fig. 20 The applied input configuration; ABC along with the signal Pass/Fail1 in case of short circuit on M20

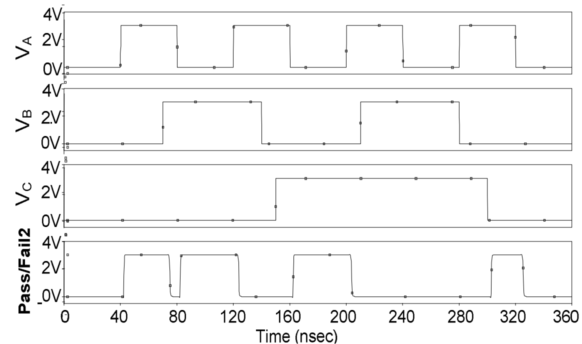


Fig. 21 The applied input configuration; ABC along with the signal Pass/Fail2 in case of open drain of M18

From the above simulations, it is clear that the proposed BIS can detect the injected short and open circuit faults, define the type of the fault using the two signals; Pass/Fail1 and Pass/Fail2 and locate it. It is worth noting that the BIS has nearly no impact on the CUT voltages. Fig. 22 simulates the difference between the last three outputs of the multiplier circuit with and without connecting the BIS. It is clear that no DC difference value in the three cases and the testing scheme cause only a little delay of max 3nsec.

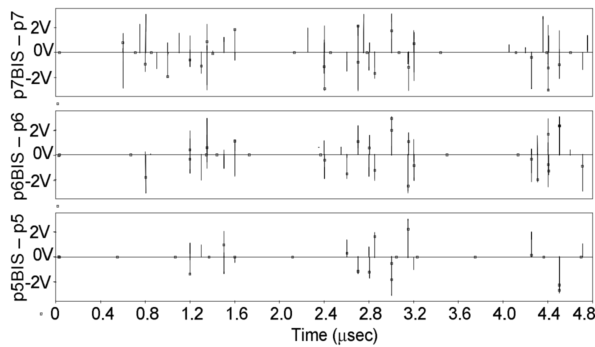


Fig. 22 The difference between the last three outputs of the multiplier with and without the BIS

V. COMPARISON AMONG THE PROPOSED BIS AND PREVIOUS WORK

A comparison of the proposed BIS with the previously published designs is shown in Tables XII and XIII, where Table XII shows the BIS properties with respect to the same aspects considered in the comparison presented in Table I among the previous BICS.

TABLE XII
BIS PROPERTIES CONSIDERING THE SAME ASPECTS AS IN TABLE I

	Sensing Element	Voltage Degradation	Using Ref. current	Type of detected fault		Using clock scheme
				Short circuit	Open circuit	
Proposed BIS	No sensing	Zero voltage degradation	No	Yes	Yes	No

	element					

And Table XIII compares between the proposed BIS and the previous published BICS according to the number of elements used, using mode select, the reaction time, the area and the power dissipation. Although a direct comparison cannot be made because the sensors are designed in different technologies, some important conclusions can be drawn from the two tables. First and foremost, the proposed BIS has zero voltage degradation, because it has no sensing element. This feature is not achieved by any other published design. Second, the proposed BIS can detect both short and open circuit faults and define the type of the fault. It is worth noting that all of the compared previous sensors detect only short circuit faults except for the sensor in [22] which is designed to detect open circuit faults only and the sensors proposed in [8] and [10], which can detect both short and open circuit faults but not all. Also, they cannot define the type of the fault. Moreover, the proposed sensor can localize the fault using the look-up tables constructed in this work. In addition, since the proposed sensor does not require a mode selection, on-line testing is possible. All of the above advantages can be achieved with a very small area, small reaction time and reasonable power dissipation.

Table XIII
COMPARISON BETWEEN THE PROPOSED BIS AND THE PREVIOUS PUBLISHED BICS

Comparison Factor / Reference	Technology μm	No. of elements	Using mode select	Reaction time in nsec	Area in μm^2	Power Dissipation in mWatt
[5], [6] and [7]	3 and 2	20MOS+1BJT +1 latch	No	-	-	-
[8]	2	13MOS+1Diode	No	2	-	-
[12]	2	35MOS+2Diode+2BJT	No	-	-	-
[9]	0.8	24MOS +1Resistor	No	2.73	246	2.132
[10]	-	7MOS	No	1	-	-
[11]	0.8	7MOS	Yes	-	28	-
[13]	0.18	BICSI:20MOS, BICSII:12MOS BICSIII:15MOS	No	-	-	-
[14]	-	18MOS +1Doide	Yes	-	-	-
[15]	0.35	41MOS+ 2Resistor	Yes	-	0.4%of the die area	-
[16]	0.6	11MOS	Yes	215	20%of the die area	-
[20]	0.25	16MOS	No	-	11.5	-
[21]	0.18	-	No	0.5	-	-
[22]	-	-	No	-	-	-
[23]	0.18	8MOS	Yes	0.51	-	27.5
[24]	0.35	15MOS	Yes	2.4	17	-
Proposed BIS	**0.25**	**48MOS**	**No**	**1.6**	**18**	**9.31**

VI. CONCLUSION AND FUTURE WORK

Simple, on-line and fast BIS, for CMOS digital circuit applications, were proposed. The BIS has nearly no voltage degradation on the supply voltage of the CUT. It can also detect both short and open circuit faults and identify the fault type using to output signals; Pass/Fail1 for short circuit fault detection and Pass/Fail2 for open circuit fault detection. Moreover, the proposed BIS can locate the fault by knowing which node it is branched from, in which MOS network (P or N), and the value of the internal node voltage at the fault case. This is done with the aid of the look up tables presented. Moreover, the proposed BIS has a small reaction time (max of 1.6nsec), and a high sensitivity. It is worth noting that the proposed BIS can be adjusted to test any other CMOS circuits by adjusting the biasing and reference voltages of the comparators used. PSpice simulations were done to verify the good response of the proposed BIS and it is proved that it detects all short and open circuit faults in the given CUT. Also, a 4x4 multiplier circuit was tested by the proposed BIS and all injected faults are well detected and defined. Also, a proposed scheme for localizing the faulty transistor in the multiplier circuit was presented. Finally, a comparison between the proposed BIS and the other BICS exist in the literature was presented. The drawback in the design of the proposed BIS is that it utilizes different supply voltage that the CUT uses. The future study tends to modify the design so that it can use the same supply voltage as the CUT.

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