Built-In Current Sensor for Testing Analog Blocks

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Abstract— This paper presents novel testing scheme for detecting catastrophic faults in analog circuits. Here, the proposed scheme is applied to test the terminal characteristics of two well-known analog building blocks; the Current Feedback Operational Amplifier (CFOA) and the Operational Trans-Resistance Amplifier (OTRA). It produces on-line testing and it has no voltage degradation. Moreover, it has a simple design, very small area and can detect both short and open circuit faults. Also, simulations are made to test two universal analog filters to prove that the proposed method can detect and localize the defected analog block in the filter. Finally, the proposed scheme is compared with the conventional I_{DDQ} testing scheme and it proves that the proposed method has a superior performance.

Key Words — Analog testing – Built in Sensors – Fault detection – Catastrophic faults

I. INTRODUCTION

The increase of mixed signal applications with ICs containing analog and digital parts, along with technology scaling, motivates the development of several approaches for testing analog sections embedded in digital systems [1-20]. So, detecting and diagnosis a fault is an integral part of integrated circuit manufacturing because a single circuit critical fault can lead to unexpected system performance, and often complete system failure. As the systems become more complex and more highly automated, the need for efficient and effective methods for fault detection provides the pre-requisites for increased reliability, minimization of maintenance activities and costs [2].

In this introduction, a brief note about analog testing methodologies is produced. But first, let us define and categorize the faults in the following subsection.

A. Fault Definition and Fault Categories

In the context of fault diagnosis, a fault is understood as any kind of malfunction in the system that leads to an unacceptable anomaly in the overall system performance [1]. A fault in a system can be very costly in terms of loss of production, equipment damage and economic setback. Faults are developed in a system due to normal wear and tear, design or manufacturing defects or improper operation leading to stress beyond endurable limits and also is subject to blemishes and imperfections. These imperfections may cause either catastrophic failure in the operation of any individual IC or minor variations in the performance from one IC to the next. The faults causing catastrophic failures are called catastrophic faults or hard faults such as open nodes, shorts between nodes, and other topological changes in a circuit caused due to dust particles, over etching or extra metal extensions which join the lines [2]. On the other hand parametric faults or soft faults refer to any change in the value of an element with respect to its nominal value outside the tolerance limits, without affecting its connectivity. These faults cause minor variation in performance. According to the number of faults, faults in analog circuits are often categorized into two types: single fault and multiple faults. The number of single faults in electronic devices accounts for 70 − 80 percent of total faults [16]. The classification of faults is shown in Fig. 1.

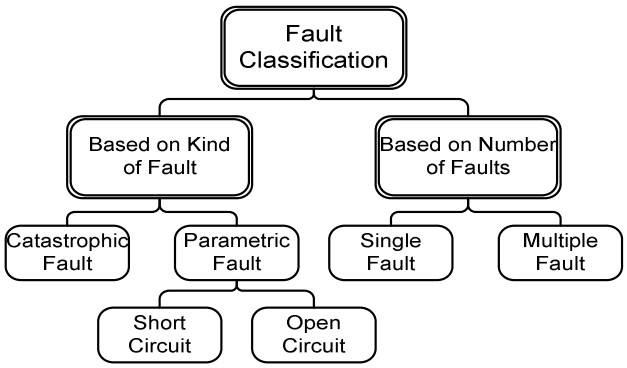


Fig. 1 The Fault Classification

In analog circuits, both kinds of faults; hard and soft, exist. Therefore the taxonomy of analog faults can be represented as shown in Fig. 2 [1]. There is a region of acceptable behavior around nominal range. Beyond this region, there is circuit performance that does not meet design specification, but does not cause complete circuit failure. Finally there are faults that render the circuit inoperable. Since both hard and soft faults can take on infinitely many varieties, there are infinitely many analog faults. Consequently, we must choose a subset of faults, which will lead to the best possible fault list. Since 80-to-90 percent of analog faults involve short and open circuit faults, in this study we have chosen the fault models of various

devices as in [17]. Open faults are hard faults in which the component terminals are out of contact with the rest of the circuit creating a high resistance at the incidence of fault in the circuit. Addition of a combination of high resistance in parallel with a small capacitor, in series (e.g., R_{open}=1MΩ and C_{open}=1fF) with the component can simulate the open faults. Short faults, on the other hand, are a short between terminals of the component (effectively shorting out the component from the circuit). A small resistor in parallel (e.g., R_{short} =100 Ω) with the component can simulate this type of fault. It is worth noting that the catastrophic fault model considered in this study does not include shorts between the gate and the source or drain of the transistors, or opens in the gate contacts. Also, it has been considered that all the faults have the same probability of occurrence.

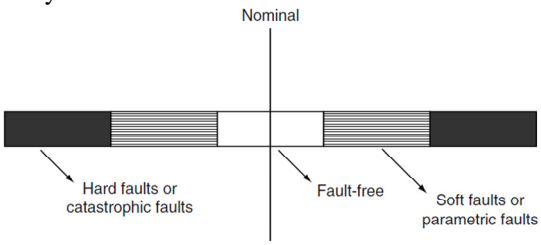


Fig. 2 The Taxonomy of analog faults

B. Analog Testing Classification

The classification of analog testing is illustrated in Fig. 3. The most famous methodologies in testing analog circuits are Built In Current Sensors (BICS), Simulation After Test (SAT) and Simulation Before Test (SBT). The SAT methods focus on parameter identification and fault verification and they are very efficient for soft fault diagnosis because they are based on linear network models. However, the major problem in parameter identification is the ability to access test points. Very often, there are not enough test points to test all components or each added test point is too expensive to accept. As an alternative, the fault verification method addresses the problem with limited number of measurements, by which not all parameters of the circuit can be identified at a time. The method assumes that only a few components are faulty and the rest of the network components are within design tolerances. Checking the consistency of certain network equations identifies faulty components. The ability to test multiple faults is limited by large number of choices of faulty components, which result in combinatorial explosion for large design. The SAT approaches have the disadvantage of high on-line computational complexity, inability to deal with catastrophic faults, error proneness to component tolerances, and high numerical sensitivity. To compromise test coverage and test simulation, SBT methods emphasize on building a fault dictionary in which the nominal circuit behaviors in DC, frequency or time domain are stored. In the test stage, the measured circuit behavior is compared with the nominal case and the faults are diagnosed. In manufacturing testing, a DC test is reliable and effective. However, when higher test coverage is needed, a frequency test or time domain test provides more information about the circuit under test without adding test nodes.

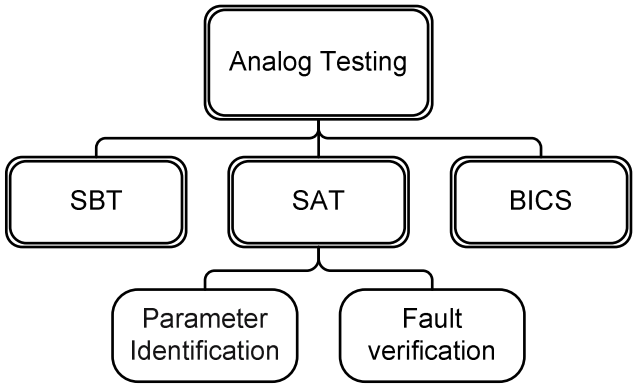


Fig. 3 The classification of the analog testing

The third testing method is the I_{DDQ} testing [3]. I_{DDQ} stands for quiescent I_{DD}, or quiescent power-supply current. I_{DDQ} testing of CMOS ICs is shown very efficient for improving test quality. The test methodology based on the observation of quiescent current on power supply lines allows a good coverage of physical defects such as gate oxide shorts, floating gates and bridging faults, which are not very well modeled by the classic fault models, or undetectable by conventional logic tests. It is recognized as the single most sensitive test method to detect CMOS IC defects. Fig. 4 shows the block diagram of the I_{DDQ} testing with BICS. Essentially, I_{DDQ} testing technique adds a BIC sensor in series with V_{DD} or GND lines of the Circuit Under Test (CUT). A series of input stimuli is applied to the device under test while monitoring the current of the power supply (V_{DD}) or ground (GND) terminals in the quiescent state conditions.

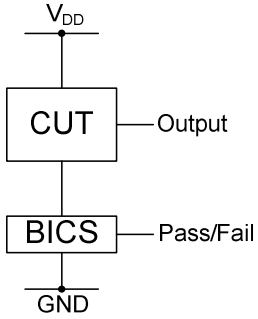


Fig. 4 Block diagram of BICS testing

Most of BICS detect the current by sensing a voltage drop across a sensing element and then, comparing this current with a reference one which represents the nominal current of the CUT. As shown in the structure of Fig. 4, the BICS is connected in series with the CUT and the supply current; I_{DDQ} is transformed to voltage using a resistance sensing element causing undesired degradation of the CUT supply voltage. Thus, for low voltage circuits, it is very important to minimize the voltage degradation.

To reduce the voltage degradation, it is better to have two modes of operation; normal and test modes. Unfortunately, these require more external pins and controlling signals and the BICS cannot operate on-line [15]. Another disadvantage in the BICS is that it uses reference current or voltage. And this reference should be adjusted for each CUT.

The objective of this paper is to present a simple Built In Sensor (BIS) which tests on the voltage terminal characteristics of the CUT and so, it does not utilize a sensing element to overcome the voltage degradation problem exist in most of the BICS. In this work, the proposed BIS is employed to test two famous analog building blocks; the current feedback operational amplifier (CFOA) and the Operational Transresistance Amplifier (OTRA) which have a great interest devoted to the analysis and design of them. This is due to the fact that they provide higher signal bandwidth, greater linearity, and larger dynamic range than conventional op-amps [62], [63].

It is worth noting that most of the previous BICS were designed to test the conventional op-amp whereas the CFOA and OTRA have not been tested before. The Paper is organized as follows: the following section give a fast survey on the previous work in the design of BICS for testing analog circuits. Section III explains the design of the proposed BIS and applies it to test the CFOA circuit. Also, a second order CFOA-based filter is tested using the proposed sensor. Testing of OTRA circuit with the proposed BIS is introduced in Section IV and a case study of testing an OTRA-based second order filter is introduced. At last, Section V concludes the overall contribution of the work.

II. A FAST SURVEY ON THE DESIGN OF BICS:

The traditional BICS consists of a sensing element which transforms the I_{DDQ} to a tested voltage then this sensor is followed by a comparator to compare the tested voltage with a reference one. The key feature in the design of the BICS is selecting the sensor to minimize the voltage degradation. Another criteria of the design of BICS is as follows:

1- designing the comparator to be sensitive to small variations.
2- Detecting faults that cause up-normal and down-normal I_{DDQ} not only up-normal I_{DDQ}.
3- Reducing the number of control bins used in the BICS.

A comparison table; Table I, is constructed to compare among the previous designs for BICS. The BICS proposed in [4] overcome the supply voltage degradation by using a Current Signature Compressor (CSC) circuit. This circuit uses transistors of the CUT as the referential transistors to mirror the current of the different branches composes the CUT. Whereas the sensing element used in the BICS of [6] is a Thin-Film Transistor (TFT) with input terminals which are capacitive coupled to the TFT gate. The voltage drop across this sensing element can be reduced to almost zero, while preserving transistor operation in the saturation region.

But the disadvantage in this method is using different and quite cost technology in the implementation. The same author uses a Floating Gate MOS (FGMOS) transistor operating in linear region in [13] to reduce the voltage drop. But this requires a sensitive comparator to detect little variations in the sensing element. In [7], the sensor is based upon a sharp use of the parasitic resistor attached to the IC interconnection layers. It takes advantage of a ratio-metric measurement of current, which allows a linear transfer function whatever the technology dispersion. But this design is quit complicated which uses a clocking scheme. A 40Ω resistor is used as the sensing element in [10].

TABLE I
COMPARISON AMONG THE PREVIOUS DESIGNS OF BICS

ref	The sensing element	Voltage degradation	Design complexity	No. of controlling pins	Limits of the comparator	
					UL	LL
[4]	CSC circuit	-	Rather simple	1	√	-
[5]	Diode connected NMOS	exist	simple	2	√	√
[6]	TFT	Almost zero	Rather complex	0	√	-
[7]	Parasitic resistance	Very small	-	0	√	√
[9]	Parasitic resistance	Very small	Rather complex	0	√	-
[10]	40Ω resistor	Very small	Simple but utilize 4 resistor	2	√	-
[11]	MOS transistor biased with forward bias technique	small	Rather simple	1	√	√
[12]	Diode connected MOS transistor	exist	Rather simple	1	√	-
[13]	FGMOS transistor	Very small	Rather complex	0	√	-
[14]	Diode connected NMOS	exist	simple	2	√	-

The mean feature in this BICS design is maintaining performance in a process and temperature varying operating environment. The sensor in [11] is designed using forward bias technique to limit the supply voltage degradation to 2% of the supply voltage. The parasitic resistance is also utilized as the sensing element in [9] where the sensing of the supply current is based on the measurement of the voltage drop across a parasitic resistance of the supply voltage metal wire. Then auto-zero technique for voltage comparator offset cancellation, which provides very accurate and sensitive low voltage measurement is used to compare the voltage drop on the sensor with a reference one. Unfortunately, this affects the sensitivity of the designed BICS. The sensing element exploited in [5], [12] and [14] is a simple diode connected MOS transistor. The key feature of the BICS designed in [12] is its programmability and ability to test many CUT simultaneously.

III. Testing the Current Feedback Op-Amps with the Proposed BIS

The proposed BIS bypass most of the drawbacks exist in the other topologies. It tests on node voltage, so, there is no need for a sensing element. Thus, it has nearly zero voltage degradation. The testing can be made on-line and does not need separate phase for testing. No excitation or read out circuitry are needed. The output is represented by testing pin which give low for proper operation and high for faulty operation. In addition, the proposed BIS does not need reference current or voltage and its design is very simple and compact. Moreover, both open and short circuit faults can be detected using the proposed BIS. The following subsections explain the design and simulation results for the proposed BIS.

A. The proposed BIS structure

The BIS is based on testing some terminal characteristics of the CFOA to check that it works correctly. The symbol of the CFOA is shown in Fig. 5; it is a four port network which has a describing matrix of the following form [21]:

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \\ V_O \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \\ I_O \end{bmatrix} \quad (1)$$

From Equation (1), two of the important characteristics of the CFOA are that the voltage is conveyed from terminal Y to terminal X and from terminal Z to terminal O. The objective of the proposed BIS is to be added to the circuitry of the CFOA to check on this voltage conveying property. The block diagram of the BIS is shown in Fig. 6(a). It consists of two comparators with their outputs goes as inputs to an OR gate. The output pin: Test_Pin, is high if the voltage at terminal (2) is less or greater than the voltage at terminal (1) by an amount; x, where x is an acceptable percentage resolution designed for the BIS. Fig. 6(b) shows how to connect the CFOA to the proposed BIS. One sensor is connected between the Y and X terminals of the CFOA and the other sensor is connected between the two other terminals; Z and O. There are two testing pins: Test_Pin1 and Test_pin2 which represent the existence of the fault in the CFOA.

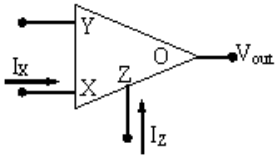


Fig. 5 Current Feedback Op-Amp symbol

B. Simulation results of testing CFOA

Fig. 7 shows the circuit diagram of the CMOS CFOA [21] used for testing. The CFOA and the BIS have been designed using 0.25μm CMOS process. Note that the faults considered here are drain-source shorts, open drain and open source faults. The circuit under test and the BIS operate with supply voltages of ±1.5V. The tolerance of the BIS is adjusted to 5% form the maximum linear range of the input voltage.

All possible faults for the given CFOA are tested by the proposed BIS and most of them are detected. It is worth noting that the BIS does not need special input for the circuit, i.e. the input here is a sinusoidal function. Fig. 8 shows the case where there is a short circuit on transistor M12. This figure shows the terminal voltages; V_Y, V_X, V_Z and V_O along with the two testing output pins;Test_Pin1 and 2. It is seen that the voltage V_X does not match the voltage V_Y. So, Test_Pin1 is high, detecting this fault.

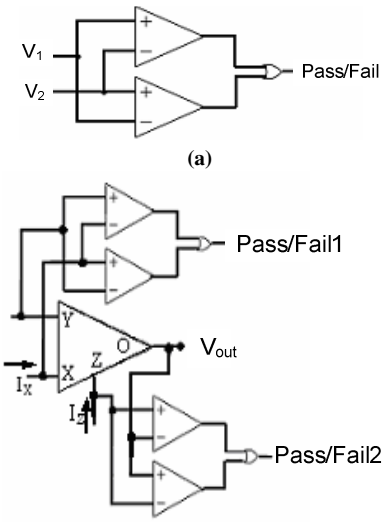


Fig. 6 (a) Structure of the proposed BIS, (b) Structure of the testable CFOA

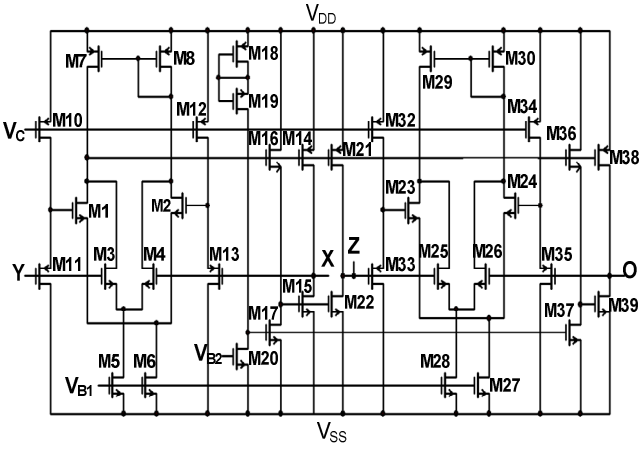


Fig. 7 CMOS realization of the tested CFOA[21]

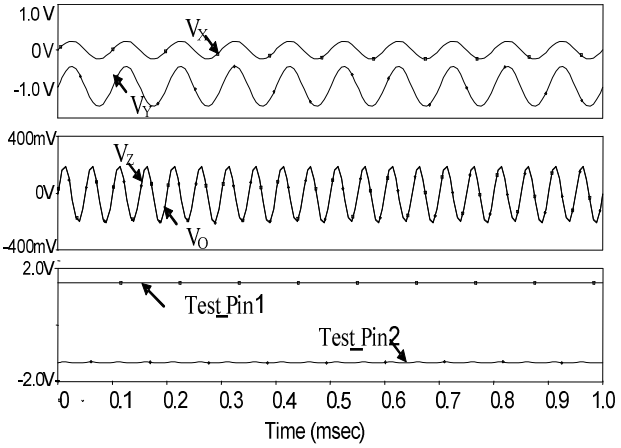


Fig. 8 The trminal voltages for the tested CFOA along with Test_Pin1 and 2 in case of M12 is shorted.

Fig. 9 shows the case where an open circuit fault is injected in the drain of M32. This fault affects the conveying function between the Z and O terminals. As seen from the figure, the voltage V_O deviate far from the voltage V_Z, and so, the signal: Test_Pin2 detects this fault. To ensure that the proposed BIS has nearly no impact on the performance of the CFOA, Fig. 10 shows the DC sweeping output voltage of a CFOA-based amplifier along with DC input voltage swept from -100mV to 100mV, with and without connecting the BIS. Also, the magnitude response of the amplifier with and without connecting the BIS is shown in Fig. 11.

C. Comparison between the proposed BIS and the conventional IDDQ testing method

To show the superior performance of the proposed BIS, it is compared with the I_{DDQ} testing method. Here, there is no specific BICS, instead, the supply current: I_{DDQ} is measured directly, which represents the best result that any BICS can have. Table II shows the simulation results for testing the CFOA using the I_{DDQ} measurement and the proposed BIS, for all possible short circuit faults. The nominal I_{DDQ} is measured to be 410.99μA.

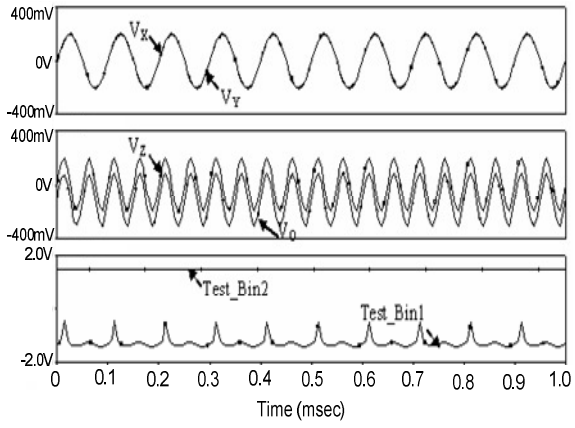


Fig. 9 The terminal voltages of the tested CFOA along with Test_Pin 1 and 2 in case of open drain fault at M32

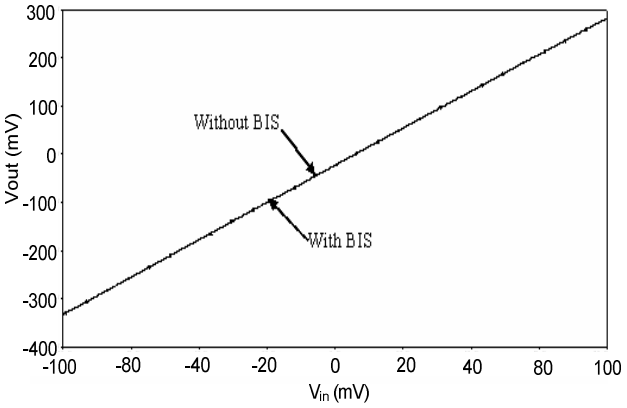


Fig. 10 CFOA-based amplifier output voltage with and without BIS

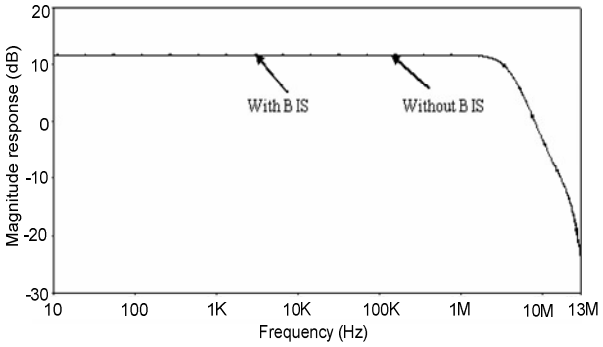


Fig. 11 The magnitude response of the CFOA-based amplifier with and without BIS

If we assume a percentage of 3% due to process variations, this means that the nominal range for the I_{DDQ} is from 398.67μA to 423.33μA. It is found that there are some faults that do not affect the performance specifications of the circuit. Those faults can be dropped from the fault list [18].

It is worth noting that the proposed BIS does not detect those faults whereas the I_{DDQ} measuring technique detects those cases as faults. From Table II, the proposed BIS can not detect six short circuit faults. Five of them can be dropped because they do not affect the performance of the CFOA. Thus, there is only one short circuit fault that can not be detected by the proposed BIS. On the other hand, there are ten faults that can not be detected by the conventional I_{DDQ} testing and five fictitious faults that are detected as faults where they do not affect the performance of the CFOA block.

Table III shows the simulation results for all open drain faults using I_{DDQ} measuring and the proposed BIS. There are only three faults that can not be detected by the proposed BIS. And there are thirteen faults that can not be detected by the I_{DDQ} measuring method. Moreover, there are six faults that are detected by the I_{DDQ} measuring method whereas they do not affect the normal operation of the CFOA, those faults are not detected by the proposed BIS. The CMOS realization of the CFOA tested here consists of 39 MOS transistor. So, there are 117 possible short and open faults. The BIS cannot detect

only seven faults which mean that the efficiency of it is 94%, where the efficiency of measuring I_{DDQ} technique is 67.5%.

A. *Application Of The Proposed Testing Sensor to a second order CFOA-based filter*

A second order CFOA-based voltage mode universal filter, shown in Fig. 12, is taken as an example to test the proposed BIS. This filter has five CFOA blocks. To reduce the overhead due to the testing equipment, only one block of the proposed BIS, which is shown in Fig. 6(a), is used to test the five CFOA blocks. Here, there are ten pairs of tested nodes; two pairs for each CFOA block. The configuration of connecting the tested nodes to the BIS is shown in Fig. 13. In this configuration, each tested pair is connected to the two inputs of the BIS through two transmission gates which are controlled by an encoder circuit. The encoder output is controlled by a counter circuit to decide which pair is to be tested by the BIS. So, all pairs can be tested on-line respectively. Table IV indicates the timing sequence of the testing operation. Note that the testing frequency is equal to $1/\sum_i T_i$, where i=1 to 10. In this example, T_i is selected to be 200nsec. Note also that testing is done on-line, and this frequency does not affect the performance of the filter. The second order filter is designed to have a Band-Pass (BP) response with center frequency; f_o= 50kHz and quality factor; Q=10. For the Low-Pass (LP) and High-Pass (HP) responses, the cutoff frequency; f_c= 50 kHz and the quality factor; Q=1. To show the efficiency of the BIS proposed, two faults are injected in different CFOAs blocks.

Fault1; An open circuit at the drain of M8 in CFOA (4): the HP magnitude and phase response, for the fault-free filter and the filter with injected fault, are shown in Fig. 14 (a) and (b) respectively. It is seen that this fault cause unwanted spick in both the magnitude and phase responses around 200kHz. Fig. 14(c) shows the output of the BIS. It is clear

TABLE II
ALL SHORT CIRCUIT FAULTS DETECTION WITH MEASURING I_{DDQ} AND THE PROPOSED BIS FOR TESTING CFOA BLOCK

Transistor	Measured IDDQ in µA	Detection by I_{DDQ}	Detection by proposed BIS	Effect on normal operation
M1	411.59	NO	YES	YES
M2	613.54	YES	YES	YES
M3	410.73	NO	YES	YES
M4	613.63	YES	YES	YES
M5	808.33	YES	NO	NO
M6	1400	YES	YES	YES
M7	616	YES	YES	YES
M8	409.18	NO	YES	YES
M10	2200	YES	YES	YES
M11	411.66	NO	YES	YES
M12	5460	YES	YES	YES
M13	412.3	NO	YES	YES
M14	1540	YES	YES	YES
M15	908.6	YES	YES	YES
M16	1810	YES	YES	YES
M17	609.64	YES	YES	YES
M18	431.2	YES	NO	NO
M19	426.66	YES	NO	NO
M20	986.26	YES	YES	YES
M21	391.36	YES	YES	YES
M22	726.98	YES	NO	YES
M23	411.89	NO	YES	YES
M24	362.38	YES	YES	YES
M25	411.37	NO	YES	YES
M26	363.31	YES	YES	YES
M27	1400	YES	YES	YES
M28	810	YES	NO	NO
M29	361.3	YES	YES	YES
M30	409.87	NO	YES	YES
M32	2200	YES	YES	YES
M33	410.88	NO	YES	YES
M34	5470	YES	YES	YES
M35	412.92	NO	YES	YES
M36	980.86	YES	YES	YES
M37	661.2	YES	NO	NO
M38	1290	YES	YES	YES
M39	979.47	YES	YES	YES

TABLE III
ALL OPEN DRAIN CIRCUIT FAULTS SIMULATION WITH MEASURING I_{DDQ} AND THE PROPOSED BIS FOR TESTING CFOA BLOCK

Transistor	Measured IDDQ in µA	Detection by I_{DDQ}	Detection by proposed BIS	Effect on normal operation
M1	410.67	NO	YES	YES
M2	410.64	NO	YES	YES
M3	410.66	NO	YES	YES
M4	410.77	NO	YES	YES
M5	394.77	YES	NO	NO
M6	393.89	YES	NO	NO
M7	411.2	NO	YES	YES
M8	411.14	NO	YES	YES
M10	390.82	YES	YES	YES
M11	391.61	YES	YES	YES
M12	390.9	YES	YES	YES
M13	592.36	YES	YES	YES
M14	292.72	YES	YES	YES
M15	586.02	YES	NO	YES
M16	259.39	YES	YES	YES
M17	618.46	YES	YES	YES
M18	922.68	YES	YES	YES
M19	922.82	YES	YES	YES
M20	404.02	NO	NO	NO
M21	410.44	NO	NO	YES
M22	359	YES	NO	YES
M23	410.09	NO	YES	YES
M24	411.12	NO	YES	YES
M25	410.46	NO	YES	YES
M26	410.98	NO	YES	YES
M27	393.89	YES	NO	NO
M28	394.77	YES	NO	NO
M29	411.5	NO	YES	YES
M30	410.85	NO	YES	YES
M32	390.74	YES	YES	YES
M33	391.87	YES	YES	YES
M34	390.98	YES	YES	YES
M35	341.43	YES	YES	YES
M36	312.19	YES	NO	NO
M37	491.18	YES	YES	YES

Transistor	Measured IDDQ in μA	Detection by I_{DDQ}	Detection by proposed BIS	Effect on normal operation
M38	345.99	YES	YES	YES
M39	360.38	YES	NO	NO

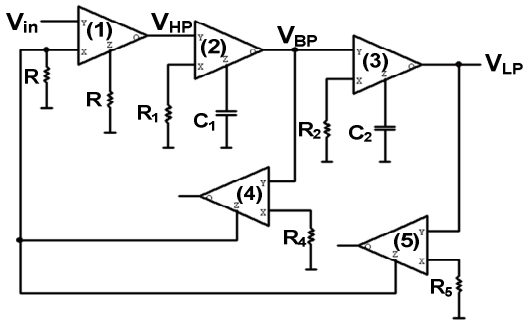
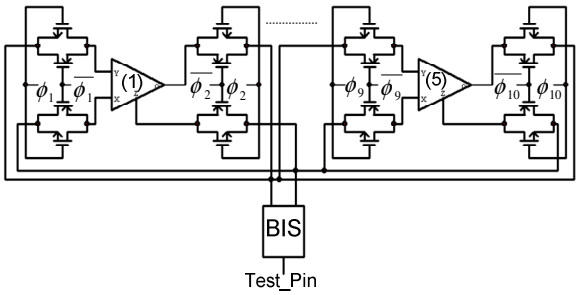
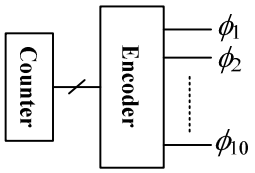


Fig. 12 Second order CFOA universal filter

that this fault is detected by the proposed BIS in the period from 1.2μsec to 1.4μsec. Using Table IV, this fault is detected in the period T_7, which is dedicated to test the Y-X conveying property of the fourth CFOA. So, using this testing scheme, one can localize the faulty CFOA and also the faulty part on it.

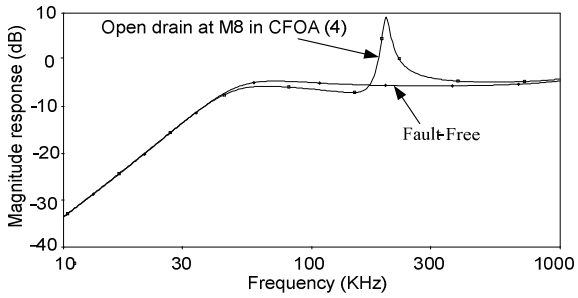


(a) connecting to the internal nodes,

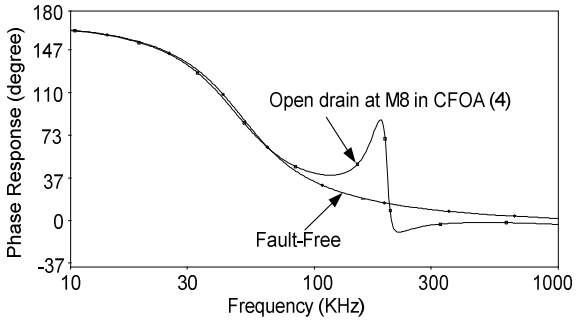


(b) generating control signals for the transmission gates

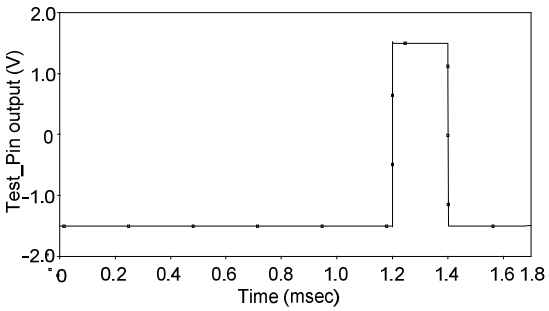
Fig. 13 The configuration used to connect all internal nodes in the CUT to the BIS



(a) The HP magnitude response of the fault-free and faulty filter,



(b) The HP phase response of the fault-free and faulty filter and



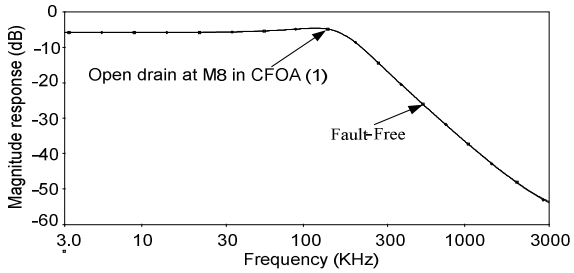
(c) the output of the BIS

Fig. 14 Fault1 case: open drain at M8 in CFOA (4)

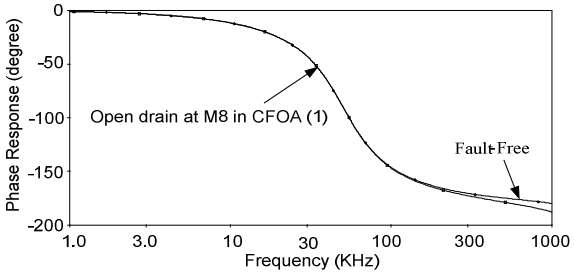
TABLE IV
THE TIMING SEQUENCE FOR TESTING THE CFOA-BASED FILTER

The period	The tested pairs
T_1: 0→0.2μsec	The X-Y terminal in CFOA(1)
T_2: 0.2μsec→0.4μsec	The O-Z terminal in CFOA(1)
T_3: 0.4μsec→0.6μsec	The X-Y terminal in CFOA(2)
T_4: 0.6μsec→0.8μsec	The O-Z terminal in CFOA(2)
T_5: 0.8μsec→1μsec	The X-Y terminal in CFOA(3)
T_6: 1μsec→1.2μsec	The O-Z terminal in CFOA(3)
T_7: 1.2μsec→1.4μsec	The X-Y terminal in CFOA(4)
T_8: 1.4μsec→1.6μsec	The O-Z terminal in CFOA(4)
T_9: 1.6μsec→1.8μsec	The X-Y terminal in CFOA(5)
T_{10}: 1.8μsec→2μsec	The O-Z terminal in CFOA(5)

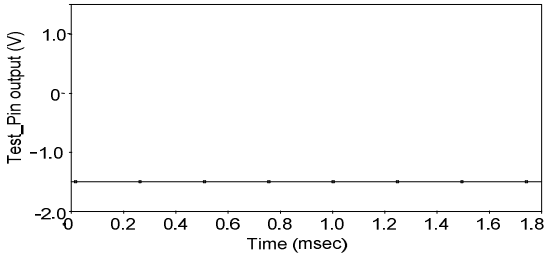
Fault2; short circuit on the transistor M18 in CFOA (1): this fault does not have any effect on the three responses of the filter under test and this is expected because this fault is classified in Table II to have no effect on the operation of the CFOA and so, it is not be detected by the proposed BIS. The LP magnitude and phase responses are shown here along with the output of the BIS in Fig. 15. Note that this fictitious fault is detected by the conventional I_{DDQ} method. The total power dissipation of the filter under test with and without connecting the testing scheme are 3.59 mWatt and 3.55 mWatt respectively, which means that the testing adds only 50μwatt.



(a) The LP magnitude response of the fault-free and faulty filter



(b) The LP phase response of the fault-free and faulty filter



(c) The output of the BIS

Fig. 15 Fault2 case: short circuit on the transistor M18 in CFOA (1)

IV. TESTING THE OPERATIONAL TRANSRESISTANCE AMPLIFIER WITH THE PROPOSED BIS

The proposed BIS is employed to test the OTRA block. The following subsections provide the design of the BIS and how it can be connected to the OTRA circuit. It provides also PSpice simulations to examine the performance of the proposed BIS. In addition, a second order OTRA-based filter is tested with the BIS.

A. The proposed BIS structure

The proposed BIS designed for testing the OTRA block, is based on the same concept of the one used to test the CFOA block and has the same advantages of it. The BIS is based on testing some terminal characteristics of the OTRA to check that it works correctly. The symbol of the OTRA is shown in Fig. 16; it is a three terminal analog building block with a describing matrix in the form [22]:

$$\begin{bmatrix} V^+ \\ V^- \\ V_o \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ R_m & R_m & 0 \end{bmatrix} \begin{bmatrix} I^+ \\ I^- \\ I_o \end{bmatrix} \qquad (2)$$

From Eqn. (2), one of the important characteristics of the OTRA is that the voltage at the positive and negative terminals of the OTRA should be zero. The objective of the proposed BIS is to be added to the circuitry of the OTRA to check on those zero voltages.

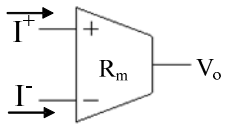
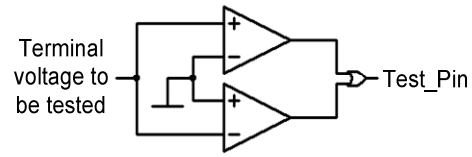
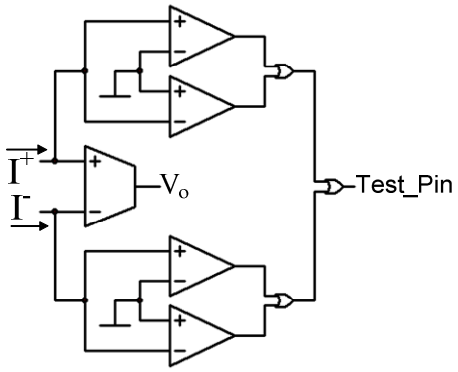


Fig. 16 Operational Transresistance Amplifier symbol



(a)



(b)

Fig. 17 (a) Structure of the proposed BIS, (b) Structure of the testable OTRA

The block diagram of the BIS is shown in Fig. 17(a). It consists of two comparators with their outputs goes as inputs to an OR gate. The output pin: Test_Pin, is high if the terminal voltages is less or greater than the ground reference voltage by an amount; x, where x is an acceptable resolution designed for the BIS. Fig. 17(b) shows how to connect the OTRA to the proposed BIS. One sensor is connected to test the positive terminal of the OTRA and the other one is connected to the negative terminal. The outputs of the two sensors are connected to OR gate to get the Test_Pin which represent the existence of the fault in the OTRA.

B. Simulation results of testing OTRA

Fig. 18 shows the circuit diagram of the CMOS OTRA used in the simulations[22]. The analog CMOS transistor fault model, simulating the possible defects is introduced using the same model used in testing the CFOA. The circuit under test and the BIS operate with supply voltages of ±1.5V. The biasing voltages; V_{B1} and V_{B2} for the OTRA, are -0.5V and 0.7V respectively.

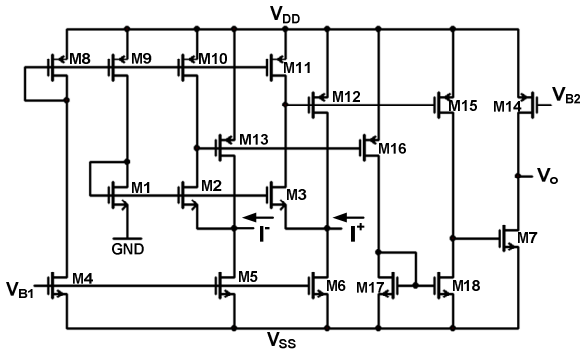


Fig. 18 CMOS realization of the OTRA under test [22]

To decide the tolerance of the BIS, the OTRA circuit is simulated with no fault taking into consideration 10% variations in the power supply and temperature. The tolerance selected here is ±13.5mV. This means that the output of the sensor is high, if the input is greater or less than the zero voltage by 13.5mV. An OTRA-based Voltage Controlled Voltage Source (VCVS), which is shown in Fig. 19, is used as the CUT to test all possible faults by the proposed BIS and most of them are detected. The VCVS is designed to have a unity gain. It is worth noting that the BIS does not need special input for the circuit. Thus, the input selected in this simulation is a sinusoidal function with frequency 10kHz. Fig. 20 shows the case where there is a short circuit on transistor M2. In this figure, the terminal voltages; V^+ and V^- along with the testing output pin are traced. It is seen that the voltage V^+ equals -11mV, which means that it is in the normal range, whereas the negative terminal voltage; V^- equals 828mV, which means that it is out of nominal range. So, Test_Pin is high, detecting this fault.

Fig. 21 shows the case where an open circuit fault is injected to the source of M8. In this case, the mean value of the terminal voltage: V^+= 73mV and V^-= 75mV. This fault is detected by Test_Pin signal.

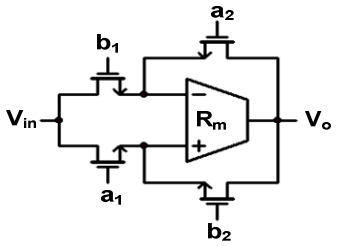


Fig. 19 The OTRA-based VCVS used as CUT [22]

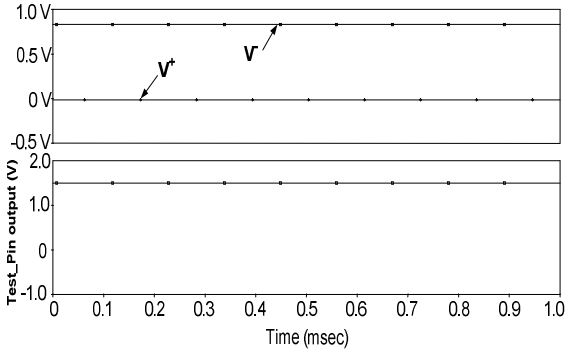


Fig. 20 The terminal voltages of OTRA along with the output of the BIS in case of short circuit on transistor M2

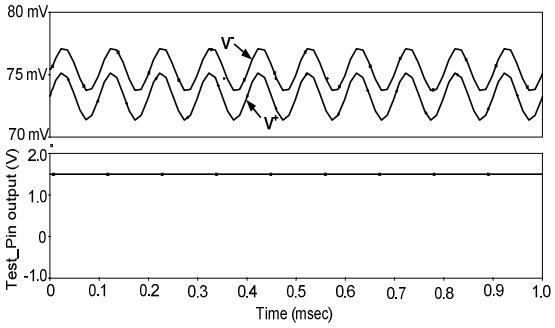


Fig. 21 The terminal voltages of OTRA along with the output of the BIS in case of open drain at transistor M8

To ensure that the proposed BIS has nearly no impact on the performance of the OTRA-based VCVS, Fig. 22 shows the magnitude and phase responses of the VCVS with and without connecting the BIS. It is clear that the proposed BIS has no impact on the performance of the OTRA.

C. Comparison between the proposed BIS and the conventional I_{DDQ} testing method

To show the effectiveness of the proposed BIS, the OTRA-based VCVS considered here is tested using the I_{DDQ} topology. Here, there is no specific BICS, instead, the supply current I_{DDQ} is measured directly, which represents the best result that any BICS can have.

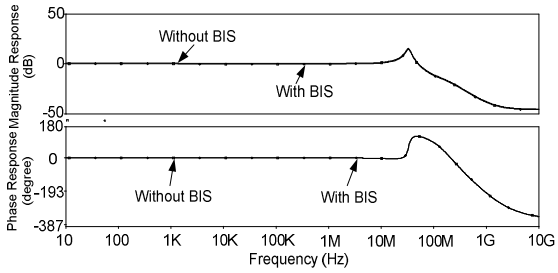


Fig. 22 The magnitude and phase response of the OTRA-based VCVS with and without connecting the BIS

Table V shows the simulation results for testing using the I_{DDQ} measurement and the proposed BIS, for all possible short circuit faults. The nominal I_{DDQ} is measured to be 2.8233mA. If we assume a percentage of 3% due to process variations,

this means that the normal range for the I_{DDQ} is from 2.74mA to 2.908mA. So, from Table V, the short circuit on transistor M11 cannot be detected by the I_{DDQ} method and the short circuit on transistor M8 cannot be detected by the proposed BIS.

TABLE V
ALL SHORT CIRCUIT FAULTS DETECTION WITH MEASURING I_{DDQ} AND THE PROPOSED BIS FOR TESTING OTRA BLOCK

Transistor	Measured IDDQ in mA	Detection by I_{DDQ}	Detection by proposed BIS
M1	2.1259	YES	YES
M2	3.3477	YES	YES
M3	3.4956	YES	YES
M4	5.7126	YES	YES
M5	11.59	YES	YES
M6	8.6175	YES	YES
M7	5.1839	YES	YES
M8	3.5581	YES	NO
M9	4.7623	YES	YES
M10	3.5608	YES	YES
M11	2.9072	NO	YES
M12	4.0068	YES	YES
M13	3.179	YES	YES
M14	5.2426	YES	YES
M15	8.8452	YES	YES
M16	5.5334	YES	YES
M17	4.5885	YES	YES
M18	3.0977	YES	YES

Table VI shows the simulation results for all open drain faults cases using I_{DDQ} measuring and the proposed BIS. There are two faults that neither detected by the proposed BIS nor by the I_{DDQ} method. The CMOS realization of the CFOA tested here consists of 18 MOS transistor. So, there are 54 possible short and open faults. The BIS can not detect five faults which mean that the efficiency of it is 90.7%. Note that it is the same efficiency for measuring I_{DDQ} technique. But the I_{DDQ} method has the drawback of voltage degradation which may affect the performance of the CUT.

TABLE VI
ALL OPEN DRAIN FAULT CASES WITH MEASURING I_{DDQ} AND THE PROPOSED BIS FOR TESTING OTRA BLOCK

Transistor	Measured IDDQ in mA	Detection by I_{DDQ}	Detection by proposed BIS
M1	2.6905	YES	YES
M2	2.0307	YES	YES
M3	2.1109	YES	YES
M4	2.8533	NO	NO
M5	2.8073	NO	NO
M6	2.273	YES	YES
M7	2.9912	YES	YES
M8	2.5847	YES	YES
M9	2.5784	YES	YES
M10	3.8471	YES	YES
M11	5.1832	YES	YES
M12	6.3596	YES	YES
M13	3.6182	YES	YES
M14	3.77	YES	YES
M15	3.6348	YES	YES
M16	2.919	YES	YES
M17	3.0314	YES	YES
M18	4.5756	YES	YES

D. *Application Of The Proposed Testing Sensor to a second order OTRA-based filter*

The OTRA-based KHN biquad filter [22], shown in Fig. 23, is taken as a CUT to be tested by the proposed BIS. This filter has three OTRA blocks. To reduce the overhead of the testing elements, only one block of the proposed BIS, which is shown in Fig. 17(a), is used to test on the three OTRA blocks.

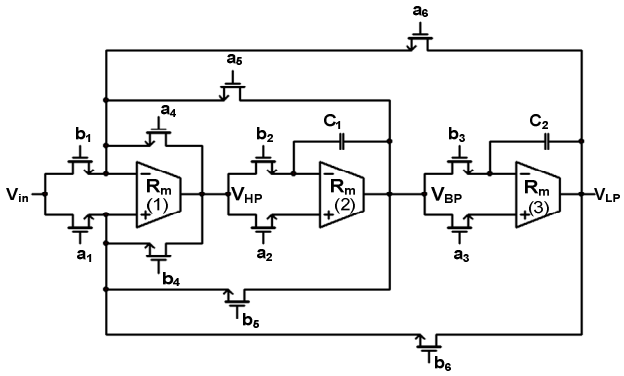


Fig. 23 The OTRA-based KHN biquad circuit used as CUT [22]

The configuration of connecting the tested OTRA blocks to the BIS is shown in Fig. 24. In this configuration, each tested OTRA is connected to the two inputs of the BIS through two transmission gates which are controlled by an encoder circuit. The encoder output is controlled by a counter circuit to decide which OTRA is to be tested by the BIS. So, all OTRA blocks can be tested on-line respectively. The testing frequency is equal to $1/\sum_i T_i$ where i=1 to 3. In this example, T_i is selected to be 200nsec. Note that testing is done on-line, and this frequency does not affect the performance of the filter. Table VII indicates the timing sequence of the testing operation. The second order filter under test is designed to have a BP response with center frequency; f_o= 100kHz and quality factor; Q=10. For the LP and HP responses, the cutoff frequency; f_c is equal to 100 kHz and the quality factor; Q is equal to 1. To show the efficiency of the BIS proposed, two faults have been injected in different OTRA blocks.

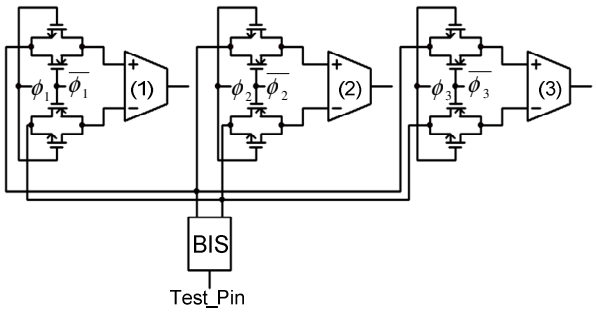


Fig. 24 The configuration of connecting OTRAs in the KHN filter example to the BIS

TABLE VII
THE TIMING SEQUENCE FOR TESTING THE OTRA-BASED FILTER

The period	The tested OTRA
T_1: 0→0.2μsec	OTRA(1)
T_2: 0.2μsec→0.4μsec	OTRA(1)
T_3: 0.4μsec→0.6μsec	OTRA(2)

Fualt1; short circuit on the transistor M8 in OTRA (2): this fault cause a large error in the cutoff frequency and a considering deviation on the quality factor in the LP response of the filter under test, as shown in Fig. 25(a). And also, the short circuit fault cause large deviation of the phase response, as seen in Fig. 25(b). The nominal cutoff frequency and quality factor are; f_c= 113.12 kHz and Q= 0.94. Whereas the measured cutoff frequency and quality factor, in case of injecting fault1, are; f_c= 51.62 kHz and Q= 1.3. The proposed BIS can detect this fault as shown in Fig. 25(c). The detected fault is in the period T_2, which means that this fault is in the second OTRA.

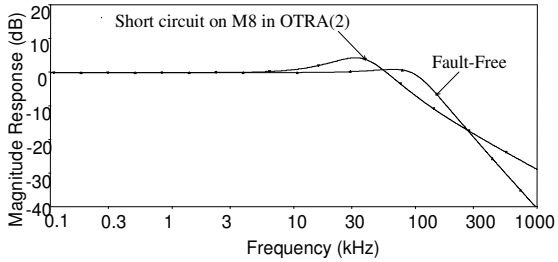
Fault2; open drain of the transistor M6 in OTRA (3): this fault causes the response of the filter under test to deviate away from the nominal response. Here, the BP magnitude and phase responses are shown in Fig. 26(a) and (b). The output of the BIS is shown in Fig. 26(c). Here, this fault is detected in the third period, which means that it is in the third OTRA block.

The total power dissipation of the filter under test with and without connecting the testing schemes are 2.33 mWatt and 2.29 mWatt respectively, which means that the testing adds only 40 μWatt.

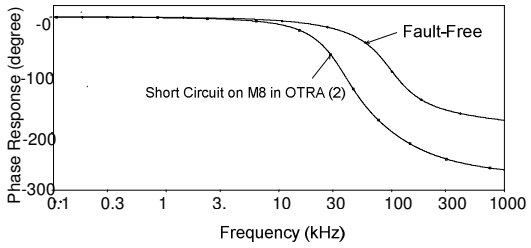
V. CONCLUSION

Smart BIS designed for testing analog blocks was presented. It is applied to test the CFOA and the OTRA analog blocks. The major contributions of the proposed sensor can be summed up as follows: a) ignored impact on the CUT, b) no reference current or voltage source used, c) detecting both short and open circuit faults, f) simple design and small area, g) reasonable power dissipation.

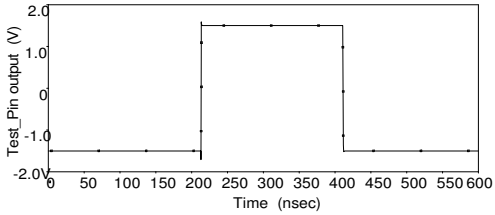
Note that the proposed sensor can also be adjusted to test any other analog CMOS block. Also, the proposed BIS was



(a) the LP magnitude response of the fault-free and faulty filter

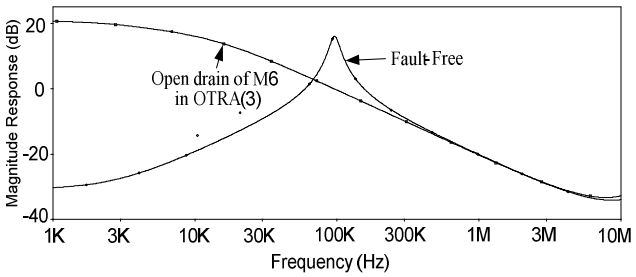


(b) the LP phase response of the fault-free and faulty filter

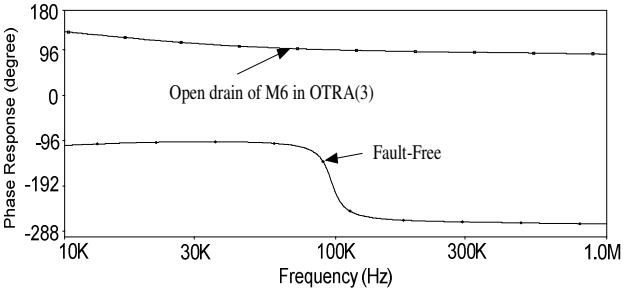


(c) the output of the BIS

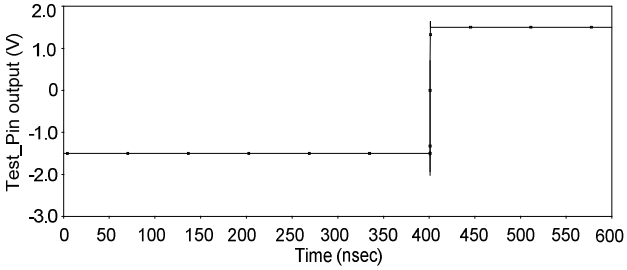
Fig. 25 Fault1 Case: short circuit on the transistor M8 in OTRA (2)



(a) the BP magnitude response of the fault-free and faulty filter



(b) the BP phase response of the fault-free and faulty filter



(c) the output of the BIS

Fig. 26 Fault2 Case: open drain of the transistor M6 in OTRA (3)

compared with the conventional I_{DDQ} testing scheme by simulations, and it is shown that the proposed BIS has a superior performance than the conventional I_{DDQ} testing scheme in case of the CFOA analog building block and it has the same efficiency in case of the OTRA. The efficiency of the proposed BIS on testing the CFOA was 94% and on testing the OTRA was 90.7%. Finally, two biquad universal filters were tested with the proposed testing scheme, and all the injected faults were detected and localized.

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