Digitally Programmable Lossless Floating Inductor Realization using Current Differential Amplifier (CDA)

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***Abstract*— A digitally programmable lossless floating inductor realization circuit is proposed. The proposed block uses current differential amplifier as an active block and the programmability is achieved through array of capacitors each one is connected to a switch, according to the logic 1 or 0 applied to the switch gate; the array size change and the programmability is achieved. The presented circuit realizes a tunable floating inductor tuned from L=26.624µH to 38.088mH. To show the reliability of the proposed block, Programmable resonant circuit has been implemented using the proposed circuit from frequency 51 kHz to 86 kHz. Also, Programmable low pass filter have been realized using the digital programmable block from frequency 6MHz to 17MHz.The simulation results has been demonstrated and discussed using PSPICE simulation for 0.18 µ m CMOS technology provided by TSMC. The proposed circuit uses ±1.5 V dual supply voltages.**

I. INTRODUCTION

The trend in IC fabrication is to have inductive less filters; that's why lots of active realizations are introduced for floating and grounded inductor using various high performance active building blocks, such as, current conveyor, current-controlled differential current voltage conveyors, current feedback op-amp, operational transconductance amplifier and many others active blocks. The most famous active inductor realization was proposed in [1] and utilizes two op-amps and five passive elements. In [2–9], circuit implementations performing equivalent floating or grounded inductances, which are based on current conveyors (CCIIs) [10–12], have been proposed. In [13-16] inductor simulator based on operational transconductance amplifier (OTA) has been proposed.

Current amplifiers are useful active devices for analogue signal processing in the current domain. They provide better operation at higher frequencies compared to conventional voltage amplifiers and wider bandwidth. Current amplifiers operate as low gain devices. For low-current gains the obtained bandwidth remains almost constant, unaffected by the current gain. In applications where noise rejection is of importance, differential input current amplifiers (CDAs) are preferable. On the other hand, the differential input provides increased flexibility in obtaining new applications.

In this paper, digitally programmable lossless floating inductor realization will be introduced. The realization uses the current differential amplifier (CDA) [17-18] as an active block and the programmability is achieved through array of capacitors which could be adapted to cover any range of frequencies; in this paper the range of operating frequency is the mid band range for signal processing applications. PSPICE simulation results are introduced and discussed. As an application to show the reliability of the proposed realization; it is applied on a series RLC resonance circuit and a 3rd order Chebyshev low pass filter which can be used in various applications.

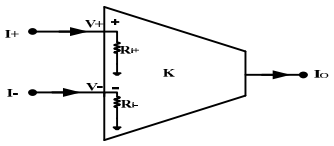

Figure 1. Current differential amplifier (CDA) [17-18] symbol diagram.

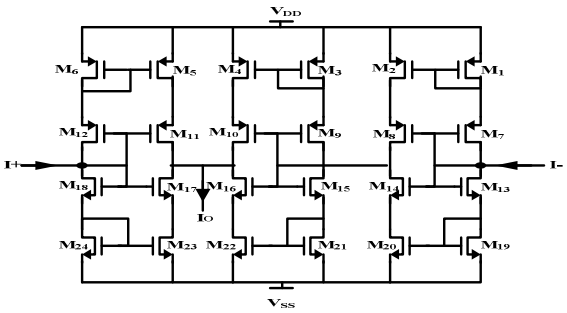

Figure 2. CMOS implementation of the CDA [17]

The paper is organized as follows Section II presents the CMOS current differential amplifier (CDA), Section III presents the CMOS implementation of CDA, Section IV Illustrates the circuit realization of the digitally programmable floating inductor, Section V discuss the implementation of a resonator circuit and a 3rd order low pass filter using the proposed realization and finally section VI drawn the conclusion.

II. CURRENT DIFFERENTIAL AMPLIFIER (CDA)[17-18]

The Current differential amplifier (CDA) is a three port network with terminal characteristics described by eqn. (1).

$$I_O = K(I_+ - I_-) \tag{1}$$

Where I_+ and I_- are the input currents of the network and I_O is the output current. The current gain equals to K for CDA and it is determined by setting aspect ratios of some transistors as explained in the next section. The symbol diagram of CDA is shown in Fig.1.

Taking into consideration the input resistance of each input terminal; the input currents could be obtained as follows:

$$I_+ = \frac{V_+}{R_i} \ , \ I_- = \frac{V_-}{R_i} \tag{2}$$

From eqn. (2), the output current equation can be written as in eqn. (3).

$$I_O = \frac{K}{R_i}(V_+ - V_-) \tag{3}$$

III. CMOS REALIZATION OF CDA

Fig.2 shows the CMOS realization of CDA [17]. It consists of three similar current mirror stages properly connected, which are two amplifying stages and one a unity gain current inverter one .

The current gain K of the amplifier in Fig.2 is calculated by the size ratio of the mirror transistors, in the two amplifying stages.

$$K = \frac{(W/L)_{MNi}}{(W/L)_{MNj}} = \frac{(W/L)_{MPi}}{(W/L)_{MPj}} \tag{4}$$

Where MN_i are the transistors M16, M22, M17, MN23; MN_j are the transistors M15, M21, M18, M24, MP_i are the transistors M10, M4, M11, MN5 and MP_j are the transistors M9, M3 , M12 , M6.

IV. FLOATING INDUCTOR CIRCUIT REALIZATION

The circuit as shown in Fig.3 [17] uses two CDA, capacitor and two floating resistors to realize floating inductor. From Fig.3 the impedance between A and B can be written as in eqn. (5).

$$L_{equ} = \frac{\left(2R_i^2 + 3R_iR + R^2\right)}{R + R_i} RC \tag{5}$$

The active inductor realization shown in Fig.3 is digitally tuned by replacing capacitor C by array of capacitors. Each capacitor is connected to NMOS switch which is responsible for connecting the capacitor branch to the circuit or not as shown in Fig.4. The capacitor array values may be different or similar according to the desired design.

The capacitor array values could be controlled through logical bits applied on the gates of MOS transistors logic‘0’ for off and logic ‘1’for on. The digital word ‘ $b_4b_3b_2b_1b_0$ ’ control the capacitor array.

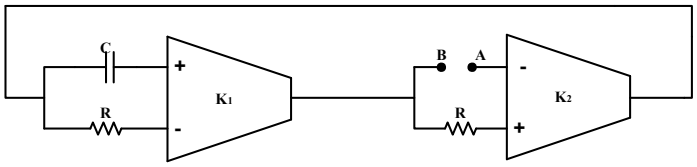

Figure 3. Floating inductor realization [17].

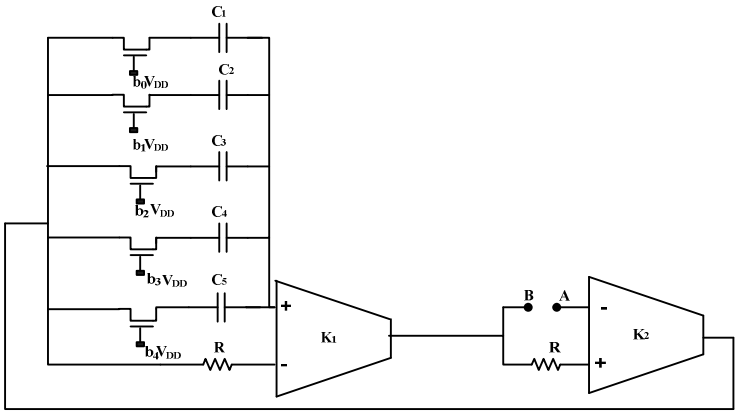

Figure 4. Digitally programmable Inductor realization.

V. APPLICATIONS

In this section the proposed programmable inductor realization is used in the implementation of a programmable resonator circuit and a programmable low pass filter.

A. Programmable resonator

The RLC series resonance circuit shown in Fig.5 with center frequency=159 kHz has been simulated using floating inductor realization shown in Fig.3. The floating inductor circuit is realized with the following values R=23 kΩ , C = 43.478 pF, K_1=1 and K_2=3.Fig.7 shows the actual inductor response relative to ideal.

The resonator's center frequency and its quality factor depend on inductor value as shown in equations (6), (7).

$$\omega = \frac{1}{\sqrt{LC}} \tag{6}$$

$$Q = \frac{1}{R}\sqrt{\frac{L}{C}} \tag{7}$$

Varying the resonator frequencies and quality factors by using tunable inductor realization shown in Fig.4 with array of capacitors and values equal to C_1=120pF, C_2 =60pF, C_3=30pF, C_4 =15pF and C_5=7.5pF to be suitable for mid band range for signal processing applications. Table I contain the different values of simulated inductance and its corresponding capacitor array values.

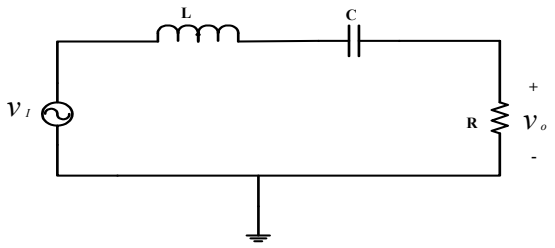

Figure 5. Passive circuit for a resonator.

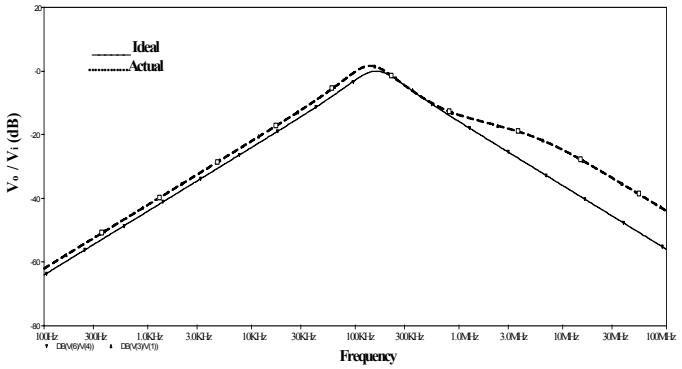

Figure 6. Ideal and actual frequency response of output voltage for the resonator circuit.

Fig.7 shows the response of resonator due to the center frequency changes. It can be used as a tunable band pass filter. The active inductor realization is simulated using SPICE based on 0.18 µm TSMC CMOS technology parameters at room temperature. The aspect ratios of transistors are given in Table II with K=1. The current differential amplifier (CDA) realization is simulated by using the schematic implementation shown in Fig.2. The DC simulation for CDA gives power consumption 53.9µw.

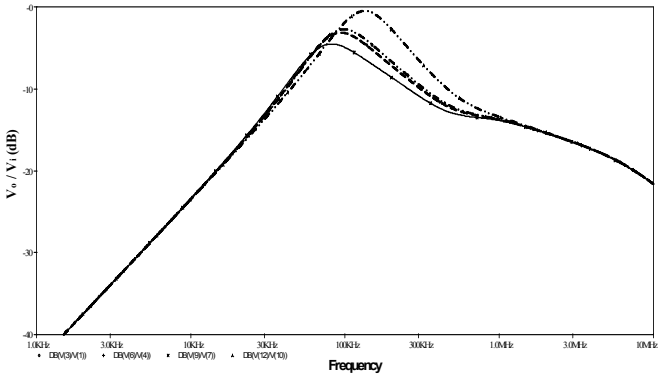

Figure 7. Frequency response of output voltage gain for different center frequency of the resonator circuit F_{center} =51 kHz, 61 kHz, 65 kHz, 86 kHz.

TABLE I. THE TUNABLE INDUCTOR VALUES USED IN RESONATOR CIRCUIT.

Inductance value (mH)	Frequency (KHz)	Logical Control word configurations				
		b_0	b_1	b_2	b_3	b_4
38.088	61	1	1	0	0	0
21.16	65	1	0	1	0	0
27.205	51	1	1	1	0	0
10.58	86	0	1	0	0	1

TABLE II. ASPECT RATIOS OF TRANSISTORS FOR K=1

Transistor	W (µm)	L (µm)
M1- M12	0.405	0.18
M13- M24	0.27	0.405
M Switch	36	0.18

B. Programmable low pass filter

A 3rd order current mode low pass filter with cutoff frequency 10 MHz and the pass-band ripple is 1dB is shown in Fig.8 .It has been simulated using the floating inductor realization shown in Fig.2. The floating inductor circuit is realized with the following values R=6 kΩ , C = 1.75425pF, K_1=3 and K_2=3.Fig.9 shows the actual inductor response relative to ideal response.

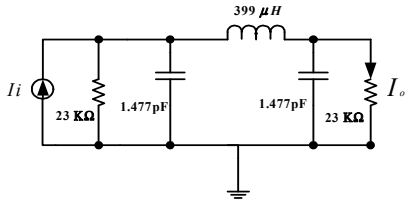

Figure 8. 3rd order low pass Ladder filter.

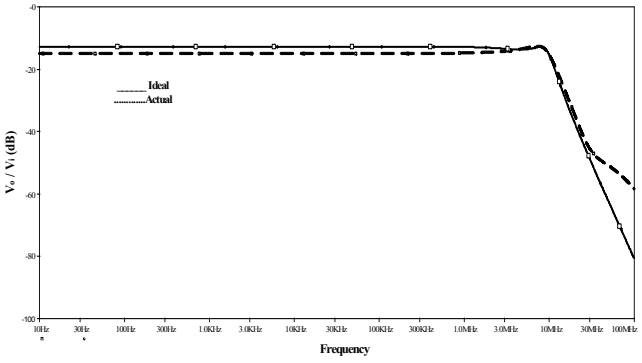

Figure 9. Ideal and actual frequency response of output voltage gain for the filter circuit.

Varying the filter frequencies by using tunable inductor realization shown in Fig.3 with array of capacitors equal to C_1=0.128pF, C_2=0.256pF, C_3 =0.512pF, C_4=1.024pF and C_5=2.048pF. Table III contains the different values of simulated inductance and its corresponding capacitor array values. Fig.10 shows the response of the low pass filter due to the cut off frequency changes.

TABLE III. INDUCTOR VALUES USED IN LADDER LOW PASS FILTER

Inductance value (µH)	Frequency (MHz)	Logical Control word configurations				
		b_0	b_1	b_2	b_3	b_4
64.33	7	0	1	0	1	0
26.624	17	1	1	0	0	0
32.16	13	1	0	1	0	0
53.8577	6	0	0	1	1	0

VI. CONCLUSION

Using the concept of CDA, NMOS switch and capacitor array a digitally tunable floating inductor realization has been proposed. It has been applied on two applications; it is useful in applications that need variability in frequency range. PSPICE simulation has been done verifying the usefulness of the proposed tunable floating inductor realization in the building active filter implementations

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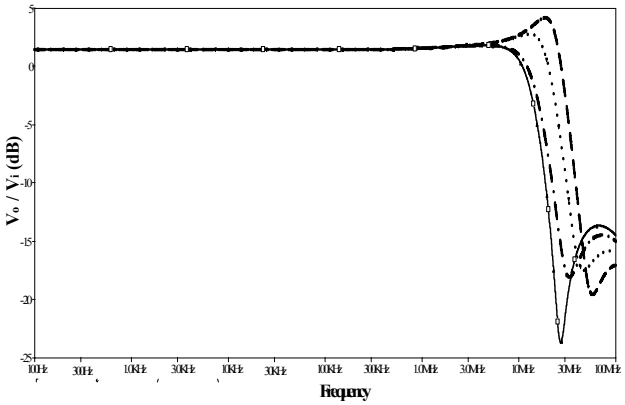

Figure 10. Frequency response of output voltage gain for different cut off frequency of the low pass filter circuit F_{cutoff} =6MHz, 7MHz, 13MHz and17MHz.

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