A Low Start-Up Voltage Charge Pump for Energy Harvesting Applications

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***Abstract*— Threshold voltage cancellation (V_t cancellation) scheme is applied to cancel the threshold drop associated with the diode-connected device and improve charge pump performance. Applying this scheme depends on generating control signals from the next stage so it cannot be applied on the output stage. In this paper V_t cancellation is applied for the output stage of modified Pelliconi pump. This is done by adding an extra circuit that establishes the controlling signals necessary for the auxiliary circuit of the output stage. This modification in the output stage leads to increasing the whole pump power efficiency and voltage gain. Also the pump output equivalent resistance is improved. The proposed charge pump is more suitable for energy harvesting applications due to its ability to give more gain at low voltage levels.**

***Keywords*—Charge pump, Energy harvesting, Power efficiency, Low voltage**

I. INTRODUCTION

Most of the current portable devices are powered by rechargeable batteries. But the battery based systems have many problems such as the need to recharge or replace these batteries with time. Due to these reasons battery based devices are not suitable for all applications. Another alternative for batteries is to utilize environmental sources of energy such as thermal energy [1]. Thermoelectric generators are the devices that convert the thermal energy harvested from the human body into electrical power. The output voltage of thermal-electrical generator is very low, usually less than 1V [2], so it cannot be used directly to power any electronic circuit. Step-up converters are used after the TEG to generate a higher voltage from the available low voltage. Two main techniques are used to implement a step-up DC-DC converter: boost converter with external LC and switched-capacitor charge pump. The charge pump (CP) simply consists of some capacitors and switches [3]. The boost converter needs external components such as inductors and capacitors to be implemented. To achieve a fully integrated system, the switched capacitor CP is chosen for harvesting systems. A CP with V_t cancellation scheme applied in output stage is presented in this paper. Section II describes conventional CP architectures. The proposed work is presented in section III. Simulation results are presented in section IV.

II. CONVENTIONAL CHARGE PUMPS

The operation of the CP simply depends on the concept of charge conservation. In Dickson CP diode connected-NMOS works as the charge transfer device [4] as shown in Fig. 1. The gain of Dickson CP is as follows:

$$Gain = \Delta V - V_{tn} \quad (1)$$

Although Dickson CP has very simple architecture, it has two main problems which influence its performance at low voltage input levels. These problems are threshold voltage drop per stage and body effect. According to (1), to obtain a positive voltage step in each stage, the following condition should be applied:

$$\Delta V > V_{tn} \quad (2)$$

Equation (2) sets a minimum limitation on the value of ΔV and hence a minimum input supply V_{DD}. Body effect problem appears due to increasing the source terminal voltage of NMOS from a stage to the next. As a result the threshold voltage of diode connected-NMOS increases with each stage.

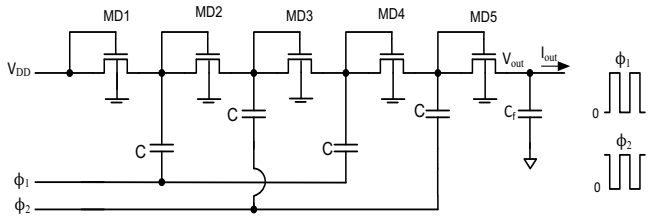

Figure 1. Five-stage Dickson CP

According to (1), as the output voltage of each stage increases, the voltage gain per stage decreases due to increasing threshold voltage. When the threshold voltage of the last stage's transistor becomes equal to ΔV the output voltage will not increase even with the addition of subsequent stages. Therefore, Dickson CP is not suitable for low-voltage applications.

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In charge transfer switch (CTS) scheme [5], threshold voltage drop associated with each diode-connected device is cancelled by adding Pass transistors in parallel with each diode connected device. Two techniques are used to control the CTS, static and dynamic controls [5]. Static CTS uses the next stage higher voltage as a static control for the CTS's as shown in Fig. 2. Although static CTS achieves higher gain than Dickson, it suffers from incomplete turning OFF of CTS in the desired period [5] and hence inefficient operation. The problem of static CTS is solved by using dynamic control of the CTS's such that CTS's can be turned off completely in the required period. As shown in Fig. 3, each CTS is accompanied by an auxiliary circuit that consists of NMOS and PMOS transistors. The auxiliary circuit works under the following condition:

$$2V_{DD} > \left|V_{tp}\right| \,\&\, 2V_{DD} > V_{tn}(n) \qquad (3)$$

Where V_{tp} is PMOS threshold voltage and $V_{tn}(n)$ is the NMOS threshold voltage modified by the source voltage at node n. But dynamic CTS is not effective at low voltage applications because CTS's are difficult to turn ON in low voltage environment, especially with increasing threshold voltage in later stages. The architecture of Pelliconi [6] is shown in Fig. 4. Pelliconi CP has many advantages. First, its gain is larger than Dickson since no threshold drop is obtained in Pelliconi stage. Second, body effect is eliminated by using triple-well technology. In addition, it has completely symmetrical stages and uses very simple clocking scheme.

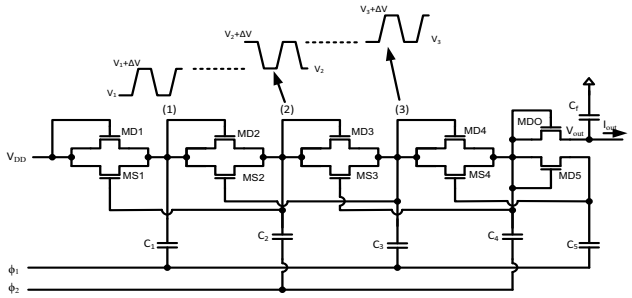

Figure 2. Static CTS CP

The problems of Pelliconi CP appear at very low voltage levels. At very low voltage levels, cascading a large number of stages is necessary to obtain the desired output voltage. But increasing the number of stages will lead to increasing the pump output equivalent resistance [7]. Thus Pelliconi CP has a poor performance at very low voltage levels. For the modified Pelliconi pump [7] shown in Fig. 5, PMOS transistors are replaced with diode-connected NMOS transistors due to their low threshold voltage in TSMC 0.25µm technology. An auxiliary circuit is added to each diode-connected device to cancel its threshold drop. The auxiliary circuit works properly under the following condition:

$$4V_{DD} > \left|V_{tp}\right| \,\&\, 2V_{DD} > V_{tn} \qquad (4)$$

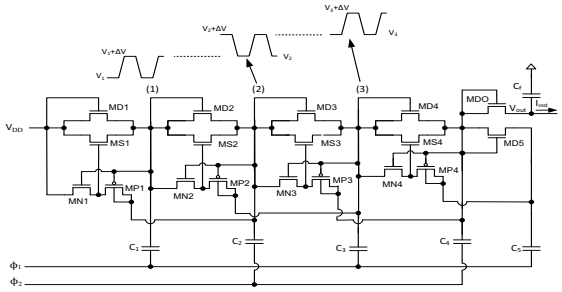

Figure 3. Dynamic CTS CP

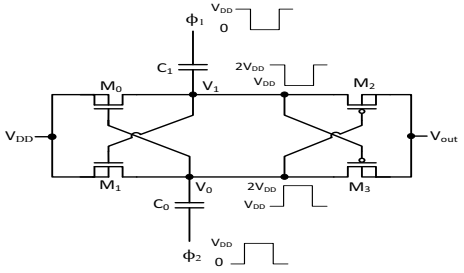

Figure 4. Pelliconi CP

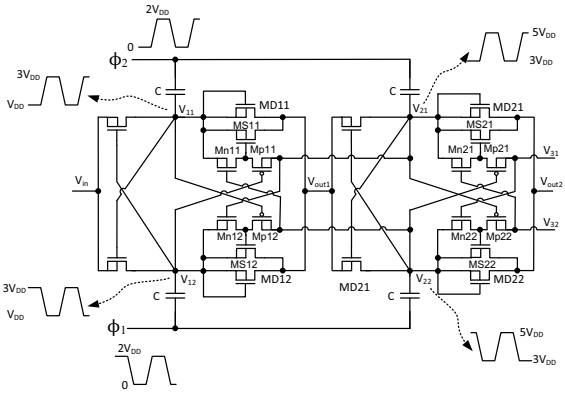

Figure 5. Modified Pelliconi CP

Comparing (4) with (3), the modified Pelliconi CP is more suitable for low voltage applications. Also the condition in (4) is the same for all stages because body effect is eliminated due to using triple-well technology and all transistors have the same threshold voltage. The output stage of this CP is shown in Fig. 6. It has no auxiliary circuit since no signal is available to control it. The controlling signals for the previous stage already exist at the nodes V_{n1} and V_{n2}.

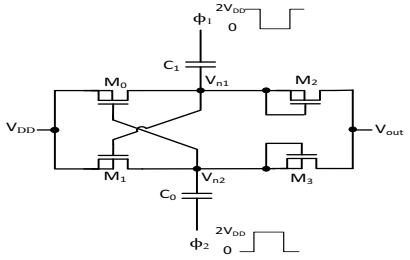

Figure 6. Output stage of modified Pelliconi CP

III. PROPOSED WORK

In the previous CP, V_t cancellation scheme cannot be applied in the output stage since no controlling signal is available for the auxiliary circuit. In this paper an extra circuit is added to establish the controlling signal necessary for applying V_t cancellation in output stage. The extra circuit consists of two diode-connected MO_1 and MO_2 and two capacitors CO_1 and CO_2 as shown in Fig. 7. The source of Mp_{11} is connected to V_{O1} while the source of Mp_{12} is connected to V_{O2}.

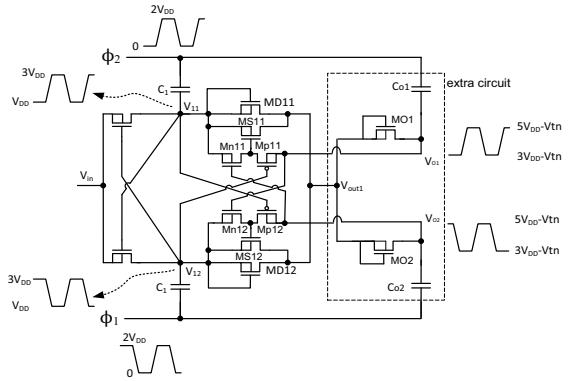

Figure7. Proposed output stage of modified Pelliconi pump

To discuss the operation of the proposed output stage, assume its input is V_{DD}. When Φ_1 is low and Φ_2 is high ($2V_{DD}$), the voltage at the nodes V_{11}, V_{12}, V_{o1}, V_{o2} and V_{out1} are $3V_{DD}$, V_{DD}, $5V_{DD}$-V_{tn}, $3V_{DD}$-V_{tn} and $3V_{DD}$ respectively. The source-to-gate voltage of Mp_{11} is $4V_{DD}$-V_{tn}. So if:

$$4V_{DD} - V_{tn} > \left|V_{tp}\right| \tag{5}$$

then Mp_{11} is turned ON. The gate-to-source voltage of MS_{11} is equal to the voltage difference between the nodes V_{o1} and V_{11}. So if

$$V_{DD} > V_{tn} \tag{6}$$

then MS_{11} will be turned ON also. For Mn_{11}, it will be OFF. When Φ_1 is high and Φ_2 is low, the voltage at the nodes V_{11}, V_{12}, V_{o1}, V_{o2} and V_{out1} are V_{DD}, $3V_{DD}$, $3V_{DD}$-V_{tn}, $5V_{DD}$-V_{tn}, and $3V_{DD}$ respectively. Mp_{11} will be turned OFF and the gate-to-source voltage of Mn_{11} is $2V_{DD}$. So if

$$2V_{DD} > V_{tn} \tag{7}$$

then Mn_{11} will be turned ON causing MS_{11} to turn OFF. It is useful to mention that the function of the capacitors CO_1 and CO_2 is only to transfer clock variations to the nodes V_{o1}, V_{o2} respectively. So the values of these capacitors are not large compared to boosting capacitors. The output voltage after N stages can be expressed as:

$$V_{out} = V_{DD} + N\left(2V_{DD}\frac{C}{C+Cs} - I_{out}r_{out}\right) \tag{8}$$

where r_{out} is the pump output resistance, I_{out} is the output load current, C is the boosting capacitors. The pump output resistance r_{out} can be approximated as:

$$r_{out} = \frac{1}{2(C+Cs)f} \tag{9}$$

Note that the factor (½) in the previous equation appears due to the existence of two pumping nodes per stage and the charge pumped by each stage per clock cycle is doubled.

IV. SIMULATIONS RESULTS

The simulations in this section are performed for two purposes. The first purpose is to test the performance of the modified Pelliconi CP with the proposed output stage and to compare between the analytical expectations and simulation results. The second purpose is to compare between the modified Pelliconi CP (Proposed-I), modified Pelliconi CP with proposed output stage (Proposed-II), and Pelliconi CP. Simulations were performed using TSMC 0.25µm CMOS technology in Spectre® .

A. Proposed-II Testing

The output voltage for six-stage at input voltage of 0.3V and frequency of 1MHz is shown in Fig. 8. From (8), at no load current, the ideal output voltage after six stages is expected to be 3.9V, but due to parasitic capacitances the output voltage is reduced to 3.7V. By substituting by V_{out}=3.7 in (8), the ratio (C/Cs) is be equal to 0.059.

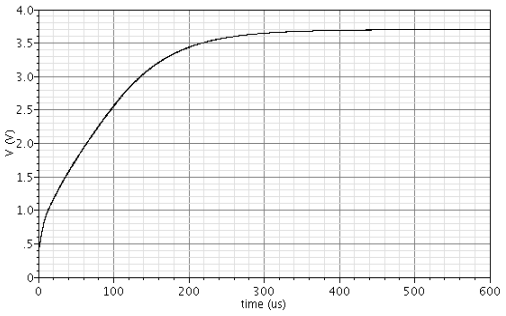

Figure 8. Initial transient (six-stage, V_{DD} =0.3V, f=1MHz, C_{load}=25pF, I_{out}=0)

Fig. 9 shows the output voltage for six-stage pump versus frequency. As expected from (8) as the frequency increases the loss in the output voltage will decrease and hence the output voltage value will increase. The analytical expectations from (8) are compared with the simulation results in Fig. 9.

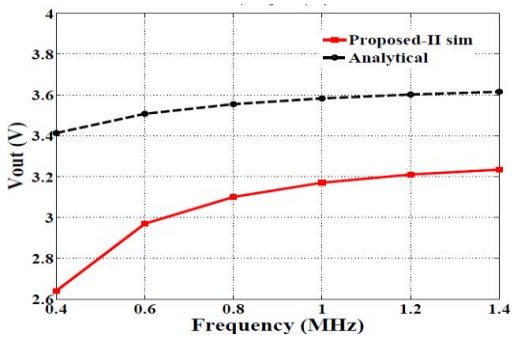

Figure 9. Output voltage versus frequency (six-stage, V_{DD} =0.3V, I_{out}=1µA)

Fig. 10 shows the output voltage of six-stage pump versus the input voltage. Both the analytical values and the simulation results are compared in this figure. The output voltage ripple is plotted versus frequency and load capacitance and the results are shown in Fig. 11 and Fig. 12 respectively. Fig. 13 (a & b) shows the power efficiency versus load current. Fig. 14 (a & b) shows the load analysis at different supply voltages and different frequencies respectively. A summary of simulation results is presented in Table I.

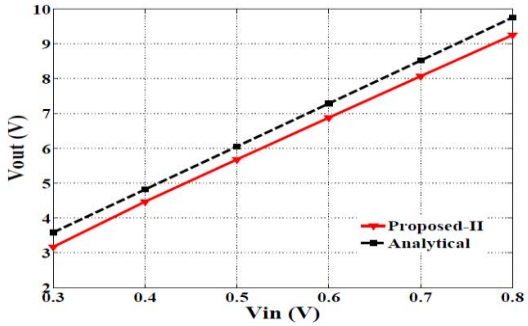

Figure 10. Output voltage versus input voltage (six-stage, Iout=1µA, f=1MHz)

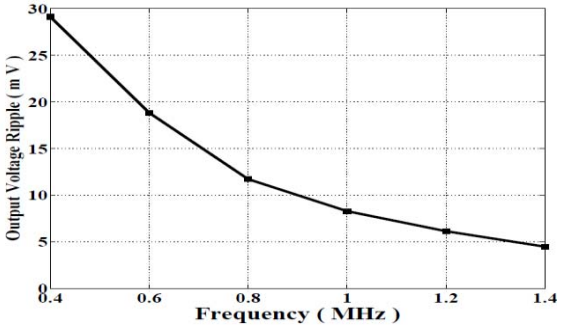

Figure 11. Output voltage ripple versus frequency (six-stage, V_{DD}=0.3V, I_{out}=1µA, C_{load}=25pF)

Table I. Summary of main simulation results

N	Main simulations results		
	Frequency (MHz)	*Max. Power efficiency (%)*	*Rout (KΩ)*
N = 3	1	68.15	150
N = 6	0.5	67.9	982.1
	1	66.39	528.5
	1.5	64.73	437.5

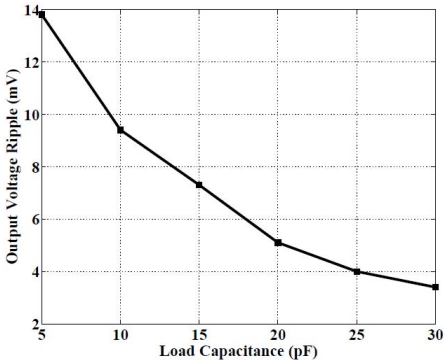

Figure 12. Output voltage ripple versus load capacitance (six-stage, V_{DD}=0.3V, I_{out}=0.5µA, f=1MHz)

(a)

(b)

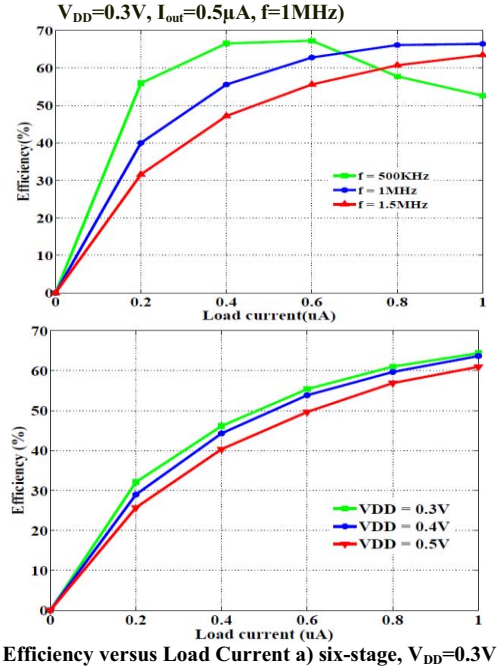

Figure 13. Efficiency versus Load Current a) six-stage, V_{DD}=0.3V b) Three-Stage, f=1MHz

(a)

(b)

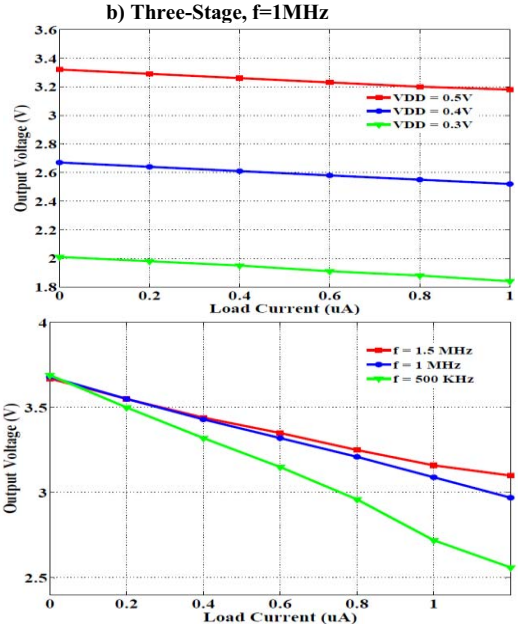

Figure 14. Output Voltage versus Load Current a) Three-stage, f=1MHz b) Six-Stage, V_{DD}=0.3V

B. Comparison

To have a fair comparison, all simulations are done for six-stage pumps at 1MHz frequency. The same clock boosting scheme has been used for all circuits and all circuits have the same value (25pF) of pumping capacitors. The power efficiency versus load current comparison is shown in Fig. 15. The proposed-I CP has a maximum power efficiency of 60.39% while the efficiency reaches 66.39% when the output proposed-II is used. The maximum power efficiency is about 53.98% in boosted Pelliconi CP.

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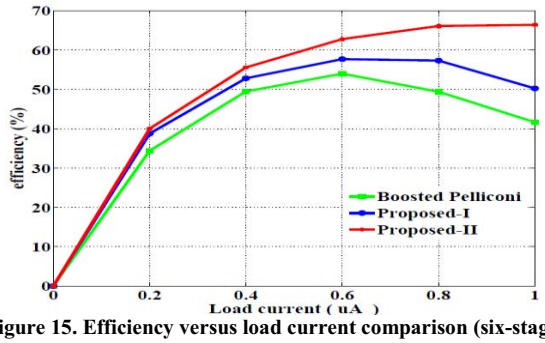

Figure 15. Efficiency versus load current comparison (six-stage, V_{DD}=0.3V, f =1MHz)

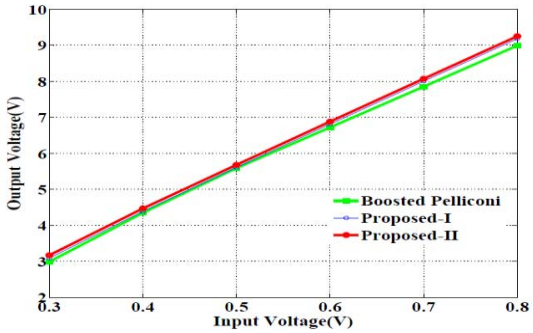

Figure 16. Gain comparison (six-stage, I_{out}=1µA, f=1MHz)

As shown in Fig. 16 the gain of the three pumps is compared. The proposed-II CP has the highest gain (e.g. at input voltage of 0.7V, the output voltage of the proposed-II is 8.07V while it is 8V for proposed-I and 7.85V for the boosted Pelliconi). The output resistance at 1MHZ frequency is compared in Fig. 17. The output resistance of the boosted Pelliconi is about 977KΩ while it is about 589.8 KΩ in the proposed-I. When proposed-II is used the output equivalent resistance is decreased to 528.5KΩ due to the improvement done in output stage. Fig. 18 shows the comparison of the output voltage versus number of stages. When a few number of stages are used (2 to 4), the boosted Pelliconi CP has higher output voltage than proposed-I and this is due to the diode-connected device in last stage of the proposed-I CP which is more significant when low output voltage is obtained. As the number of stages increases above four, the diode-connected threshold drop is less significant and the proposed-I CP achieves higher output voltage than boosted Pelliconi. Since the problem of diode-connected is eliminated in the proposed-II CP, it always has the highest output voltage at any N.

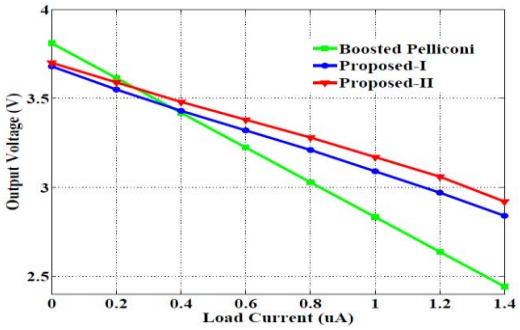

Figure 17. Output voltage versus output current comparison (six-stage, V_{DD}=0.3V, f =1MHz)

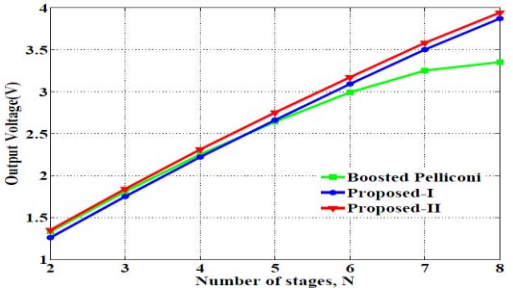

Figure18. Output voltage versus number of stages comparison (V_{DD}=0.3V, f =1MHz, I_{out}=1µA)

V. CONCLUSION

In this paper, the output stage of modified Pelliconi CP is optimized by employing V_t cancelation. Eliminating the threshold voltage drop associated with each diode-connected device in output stage improves the whole performance of the pump. The proposed solution is analyzed and simulated against modified Pelliconi CP. The power efficiency is shown to be about 6% higher than modified Pelliconi CP. Furthermore, the improvement in output resistance value is about 10%. The proposed pump also achieves higher gain at low voltage levels which makes it more suitable for energy harvesting applications.

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