High Speed Fully Differential Second Generation Current Conveyor

Soliman A. Mahmoud[(1)], Eman A. Soliman[(2)], Maurits Ortmanns[(3)] and Ahmed M. Soliman[(4)]
(1) Electrical and Computer Engineering Department, Faculty of Engineering, Sharjah University, Sharjah, UAE, solimanm@sharjah.ac.ae
(2) Electrical and Electronics Engineering Department, Faculty of Information Engineering and Technology German University in Cairo, Cairo, Egypt
(3) Institute of Microelectronics, University of Ulm, Ulm, Germany
(4) Electronics and Communication Engineering Department, Faculty of Engineering, Cairo University, Cairo, Egypt

***Abstract*—In this paper, a high speed fully differential second generation current conveyor (FDCCII+) is presented. The proposed FDCCII+ is based on using fully differential buffer [1] and class AB push-pull output stage with a new standby current control circuitry. The circuit is realized using 90nm CMOS TSMC technology model under 1.2V single supply voltage. The proposed realization of FDCCII+ input differential voltage dynamic range is from -0.45V to 0.45V. The total power dissipation of the circuit is 1.7mW. The simulated bandwidth of the FDCCII+ is 254MHz under 10KΩ load at X and Z terminals. All the circuit simulations are done using Cadence Virtuoso SPECTRE circuit simulator.**

I. INTRODUCTION

Fully differential circuit configurations have been widely used. They have higher rejection capabilities to clock-feed-through, charge injection errors and power supply noises, larger output dynamic range, higher design flexibility, and reduced harmonic distortion in high-frequency analog signal applications [2]. For these reasons, many conventional single ended active blocks such as voltage op-amps and current conveyors was modified to handle differential signals [3], [4],[5].

The fully differential second generation current conveyor (FDCCII+) is also suitable for high frequency applications. The FDCCII+ surpasses conventional voltage op-amps frequency response because it doesn't have constant gain bandwidth product. Most of the analog signal processing applications can be realized using current conveyors. The circuit symbol of FDCCII+ is presented in Fig.1. The Y terminal is a high impedance port while the X terminal has considerably lower impedance than Y terminal. The Z terminal has large impedance to make the block suitable for current mode applications. The differential voltage applied to the Y terminal is conveyed to the X terminal and the X terminal differential current is conveyed to the Z terminal. The IV-characteristics of FDCCII+ are given as follows:

$$\begin{bmatrix} I_{Yd} \\ V_{Xd} \\ I_{Zd} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} V_{Yd} \\ I_{Xd} \\ V_{Zd} \end{bmatrix} \quad (1)$$

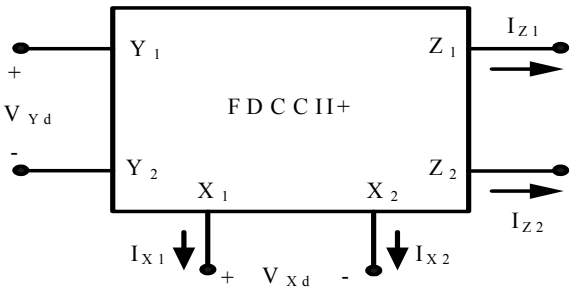

Figure 1 FDCCII+ circuit symbol

In this paper, a proposed high frequency FDCCII+ is realized using 90 nm CMOS TSMC technology model. The paper is organized as follows; section II contains the CMOS realization of FDCCII+ and a summary of the circuit specifications. Section III contains the simulation results of the FDCCII+. The simulations investigate the FDCCII+ Y terminal differential voltage dynamic range, X terminal differential current dynamic range, the 3-dB bandwidth of the FDCCII+ at X and Z terminals, the finite output resistance at the X terminal (ideally equals to zero) and the X terminal offset voltage. Finally section IV concludes the paper.

II. PROPOSED CMOS REALIZATION OF THE FDCCII+

The proposed CMOS realization for the FDCCII+ is shown in Fig.2. The circuit is based on the use of fully differential buffer (FDB) [1].

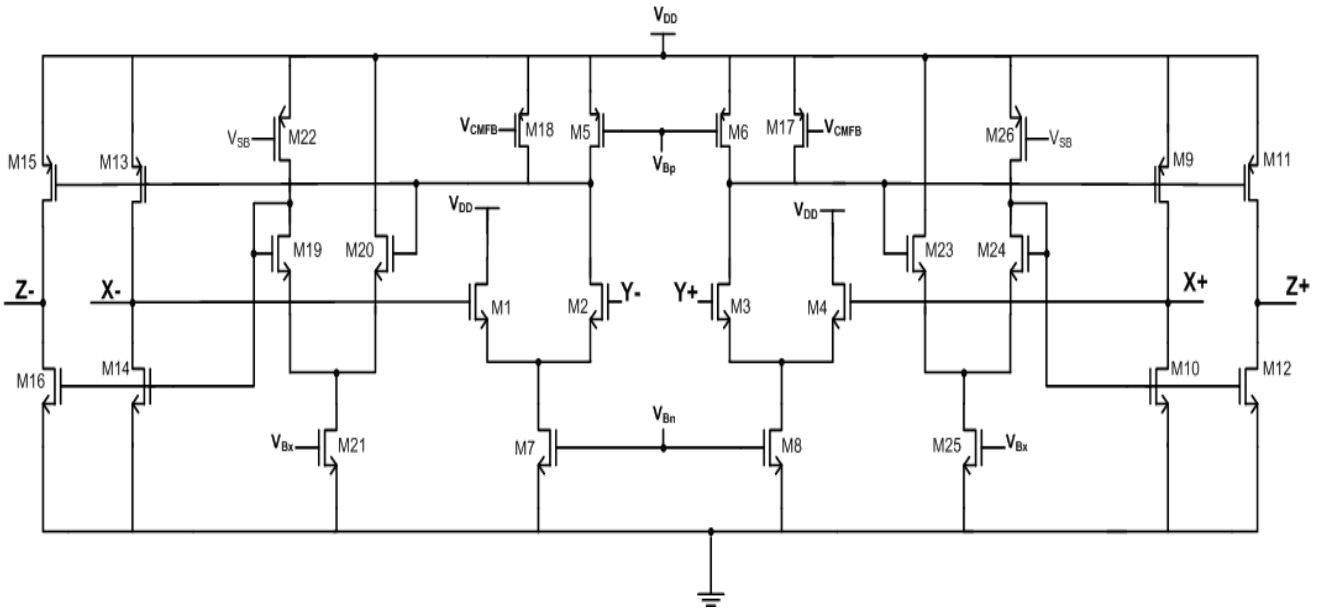

Figure 2 Circuit Diagram of the FDCCII+

The FDB conveys the differential voltage of Y terminal to the X terminal. The FDB consists of two matched DPs formed with transistors M1-M2 and M3-M4. The two DPs are biased with two identical tail current sources formed from transistors M7 and M8. The drains of M2 and M3 are connected to the constant current sources M5-M6; this will force the currents of the DPs to have the same common mode and differential values and consequently the gate voltages of the DPs are equal.

The current conveying action is obtained using two class AB push-pull output stages formed with M9-M16. The output stages DC operating point are controlled using two identical circuits formed with M19-M22 and M23-M26. The control circuit is formed with NMOS native transistor DP (M19-M20 and M23-M24) biased using tail current source realized with transistor M21 and M25. Transistors M22 and M26 act as a constant current source controlled using V_{SB}. According to the ratio between the drain currents of M21- M22 and M25-M26 the gate voltages of M10, M12 and M14, M16 are adjusted to control the output stage DC operating point.

The control voltage V_{SB} is generated from extra circuitry shown in Fig.3. The biasing circuit consists of native transistor [6] DP formed with M27-M28 with their gate voltage connected to the drains of two self biased transistors M31 and M32 respectively. The gate voltages of the DPs are controlled using the biasing current I_{SB}.

Finally; a common mode feedback (CMFB) circuit is used to adjust the output voltage common mode value. The CMFB circuit generates V_{CMFB}. The circuit is shown in Fig.4. The CMFB circuit compares the output common mode value Vo_{av} with the desired value V_{CM} and generates V_{CMFB} which adjusts the output common mode value using M17 and M18. The common mode estimator circuit [7] used is shown in Fig.5.

The common mode estimator circuit is illustrated as follows: M39-M42 are matched transistors and operate in saturation region together they form two DPs, M43-M46 are matched and used as current mirrors to force the currents flowing in the two DPs to be the same. Transistors M51 and M52 are used to bias the two DPs M39-M42. Transistors M47-M50 compose a negative feedback loop to generate a proper biasing voltage for M52.

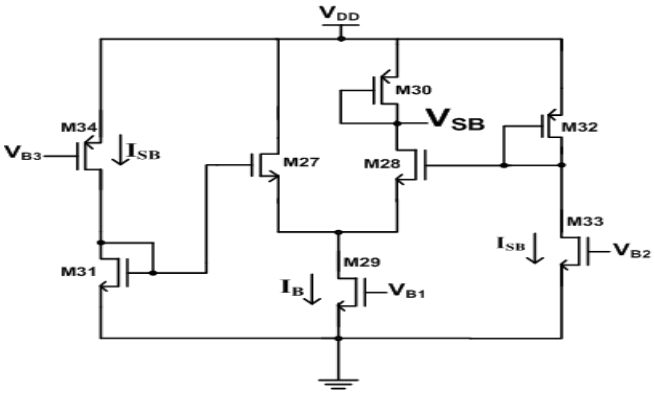

Figure 3 Biasing Circuit used to Generate V_{SB}

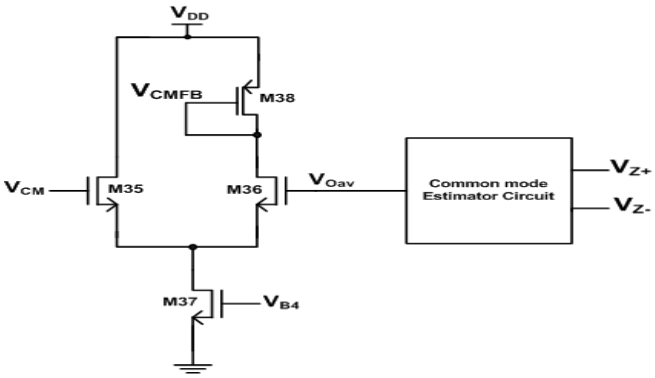

Figure 4 CMOS Realization of the Common Mode Feedback Circuit

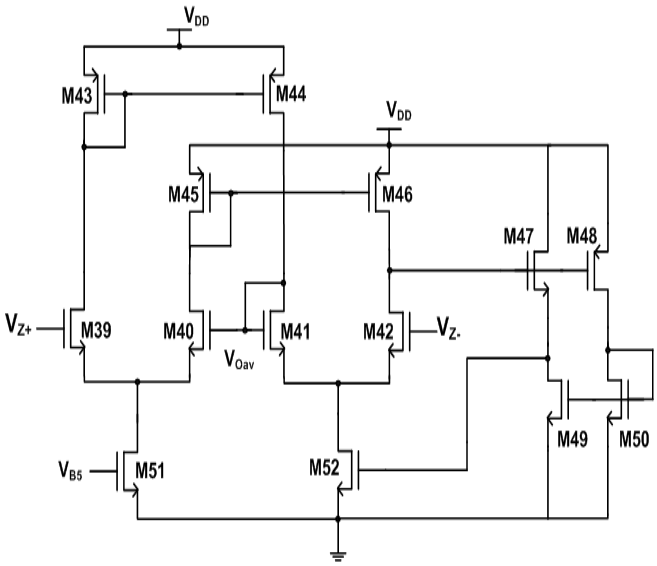

Figure 5 CMOS Realization of the Common Mode Estimator Circuit [7]

III. Simulation Results

The FDCCII+ in Fig.2 is simulated using 90nm CMOS TSMC technology model under 1.2V single supply. The circuit is simulated using Cadence Virtuoso SPECTRE circuit simulator. The FDCCII+ is simulated while loaded with 10kΩ resistors at X and Z terminals. The voltage following action and their difference are shown in Fig.6 and 7 respectively. The current following action is tested with terminal Y voltage fixed at 0.6V (common mode value of the voltage supplies). The current at Z terminal follow the X terminal current from -0.5mA to 0.5mA under short circuit loading condition at Z terminals as shown in Fig.8. The FDCCII+ voltage following action frequency response is shown in Fig.9. The output resistance at X terminals is shown in Fig.10. The offset voltage at the X terminal is shown in Fig.11. Table I contains a summary of the FDCCII+ parameters obtained from the simulations in addition to a comparison with previous work given in [1].

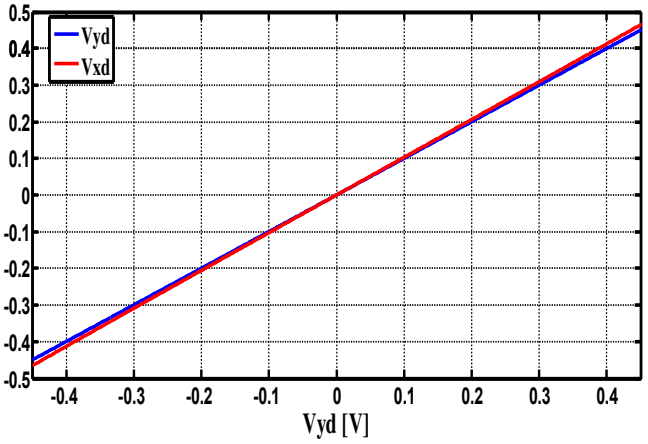

Figure 6 Differential Voltage Following Action between X and Y Terminals of the FDCCII+

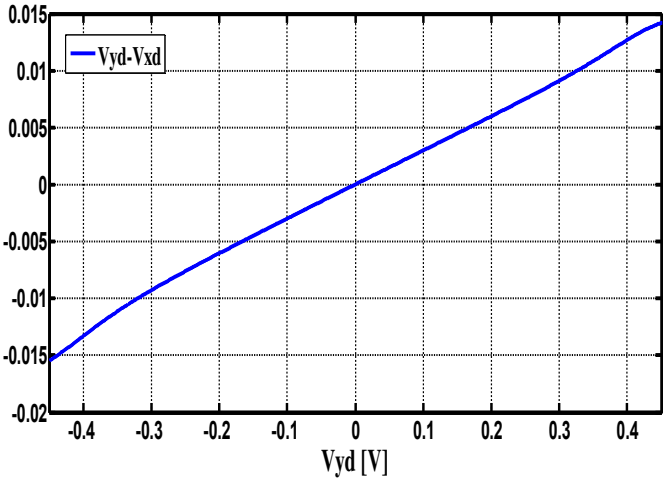

Figure 7 The Difference Voltage between X and Y Differential Voltages

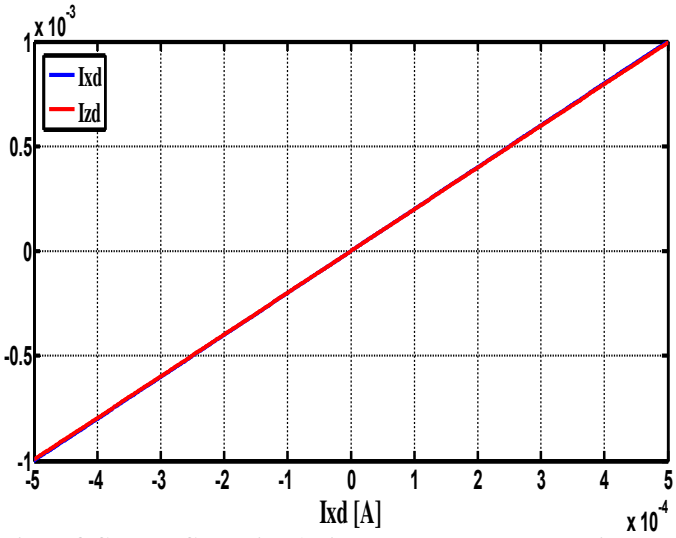

Figure 8 Current Conveying Action between X and Z Terminals

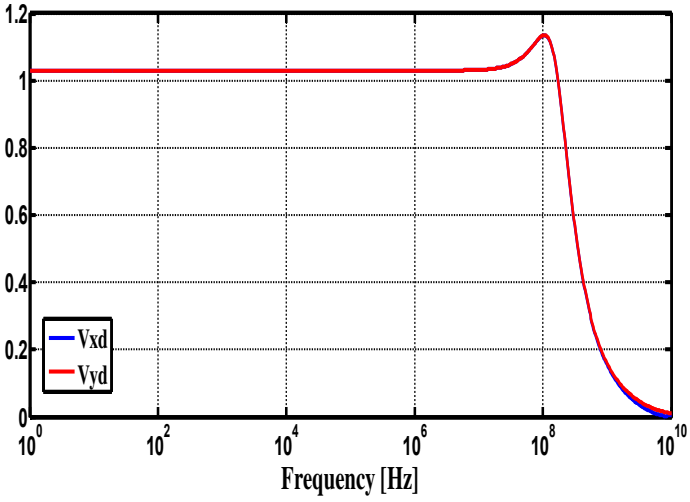

Figure 9 Magnitudes of the X and Z Terminals Voltages vs. Frequency

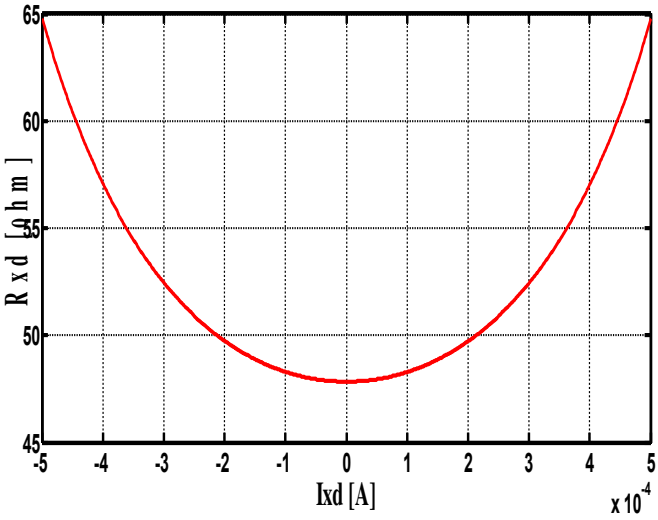

Figure 10 Finite Output Resistance of X Terminals

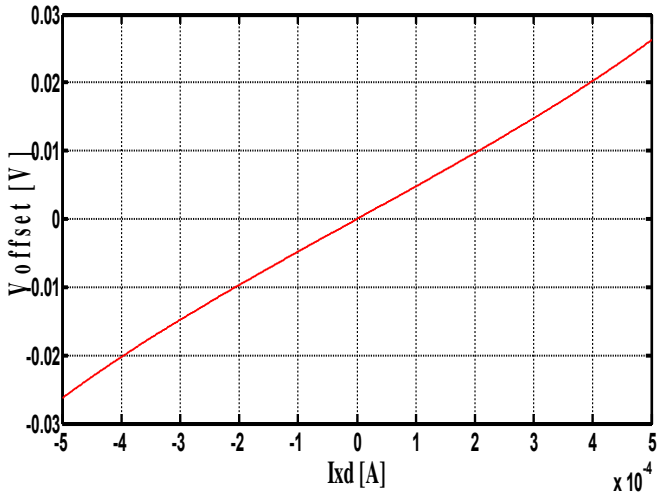

Figure 11 Offset Voltage at the X terminal

IV. Conclusion

A proposed realization for high speed FDCCII+ is presented. The FDCCII+ is realized using 90nm CMOS technology model under single supply voltage of 1.2V. The FDCCII+ is realized using fully differential buffers. A common mode feedback circuit is used for proper operation. The total standby power dissipation of the FDCCII+ is 1.7mW. The FDCCII+ input voltage dynamic range is from -0.45V to 0.45V with maximum error of 15mV and input current dynamic range from -0.5mA to 0.5mA. The maximum values of the output resistance and the offset voltage at the X terminal throughout the input current dynamic range are 65Ω and 26.17mV respectively. The circuit shows higher 3-dB frequency and higher voltage dynamic range compared to previous work done in [1].

TABLE I
FDCCII+ Simulation Results Summary

Parameter	Proposed Realization	Realization in [1]
Supply Voltage	1.2V	±1.5
CMOS Technology	90nm	0.35µm
Voltage Conveying Range	±0.45V	±0.75V
Current Conveying Range	±0.5mA	±0.5mA
Standby Power	1.7mW	1.2mW
X port 3-dB Frequency at 10KΩ	254MHz	NA
Z port 3-dB Frequency at 10KΩ	254MHz	20MHz
offset Voltage	< 26.17mV	<7mV
output resistance at X port	< 65Ω	<20Ω
THD @ f=10MHz Vyp-p=0.4sin(2πft)	1.059%	NA

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