Digitally Controlled Fully Differential Current Conveyor: CMOS Realization and Applications

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Abstract—**Design and simulation of a digitally controlled CMOS fully differential current conveyor (DCFDCC) is presented. A novel current division network (CDN) is used to provide the digital control of the current gain between terminals X and Z of this DCFDCC. The proposed DCFDCC operates under low supply voltage of ±1.5V. Application of the DCFDCC in realizing second order universal active filter is also given. PSPICE simulation confirms the performance of the proposed blocks and its application.**

I. INTRODUCTION

Programmable characteristic of an analog cell is a key feature that is used in so many useful applications. Analog or digital tuning can be employed to control the parameters of the analog cell. However, in low voltage applications, there is a limitation on the allowable range of the analog tuning voltage. Hence, in these applications, the digital control is more attractive [1-3]. Another example utilizing digital control is the interface with the digital signal processing unit (DSP) in the modern digital systems. For example, in modern wireless systems, all of the baseband signal processing is implemented digitally by DSP unit. There are baseband analog blocks required in the integrated wireless receiver such as highly linear filter section for out-of band blockers attenuation, tunable filter section for channel selection, and variable gain amplifier (VGA) for providing programmable gain setting. Hence, a primary requirement of those baseband analog blocks is to be digitally controlled.

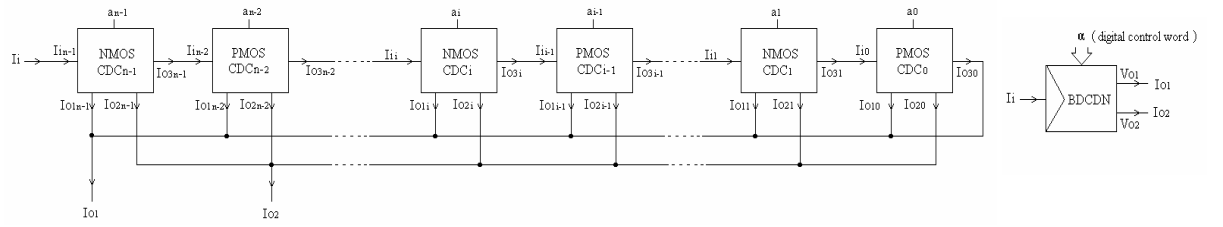
Recently, the analog circuit design using current-mode approach has gained considerable attention. This stems from its inherent advantages of wide bandwidth, high slow rate, low power consumption, and simple circuitry [4], [5]. The second generation current conveyor (CCII) proposed by Sedra and Smith [6] is one of the most versatile current-mode building blocks. Since its introduction, it has been used in wide range of applications and several circuit realizations have been proposed for its implementation (e.g., [7-9]). The CCII is a single ended device, however, fully differential circuit configuration recently have been widely used in high frequency analog signal applications. As compared to their single-ended counterparts, they have higher rejection capabilities to clock-feed-through, charge rejection errors and power supply noises, larger output
dynamic range, higher design flexibility, and reduced harmonic distortion [5].

In this paper, a digitally controlled fully differential second generation current conveyor (DCFDCC) is presented, the DCFDCC is based on using fully differential buffer [5] with its output current sensed and copied to the current ports with a current gain where this current gain is digitally controlled. Precise gain control is achieved using a novel current division technique as will be discussed on the following section. CMOS realization of the DCFDCC will be given in section III. Application of the DCFDCC in realizing digitally tuned universal filter with linearly proportional tuned frequency to the digitally controlled parameter will be given in section IV.

II. THE PROPOSED CURRENT DIVISION NETWORK (CDN)

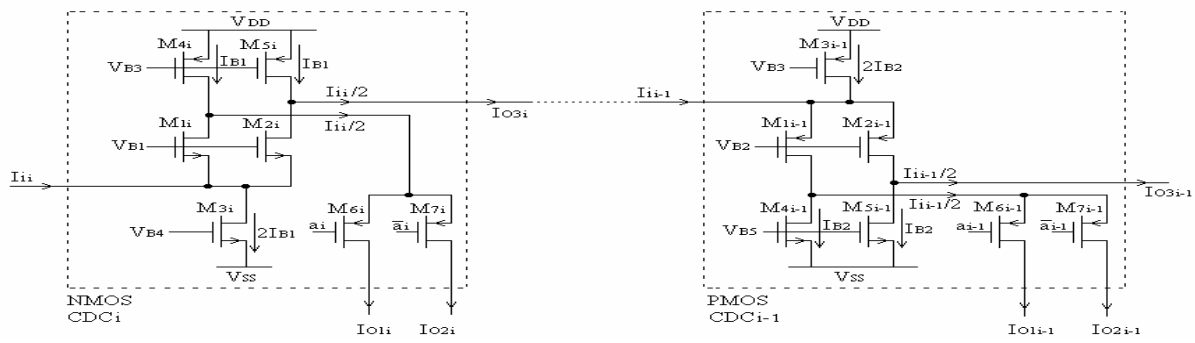
The MOS ladder circuit [10] to implement the CDN has similar structure to the classical resistor based R-2R ladder circuit. For proper operation, all transistors in the ladder must be matched. This may be very difficult to achieve in practice especially when number of bits increases. Also, the output nodes (I_{O1} and I_{O2}) of this CDN should be at virtual ground voltages. Both CDNs given in [2] and [3] have high output resistance since the output currents are drown from the drain of the transistors. Hence, no need for virtual ground nodes. Besides, only the transistors inside each CDC are required to be matched rather than matching all the transistors in the entire CDN. Hence, the matching-requirements are relaxed. However, both [2] and [3] circuits suffer from the drawback of operating in only single direction of the input current.

The block diagram of the proposed CDN is shown in Fig. 1(a). It consists of n current division cells (CDCs). Using NMOS-CDC followed by PMOS-CDC shown in Fig. 2 gives the CDN the advantage of unlimited number of bits due to the supply voltage limitation where the voltage levels are regenerated from one cell to another. The proposed CDN also has advantages based on the structure of the CDC itself such as low input impedance, and high output impedance. Hence, no need for virtual ground nodes. Also, only the transistors inside each CDC are required to be matched rather than matching all the transistors in the entire CDN. Moreover, the proposed CDN has the ability of driven by bidirectional input current. According to the current division principle, each CDC of this network has three output currents. The output currents of the current division cell number i (CDC_i) are I_{O1i}, I_{O2i}, and I_{O3i}



(a) (b)

Fig.1: (a) Block Diagram of the Proposed CDN. (b) Symbol of the CDN.



(a) (b)

Fig.2: (a) Proposed NMOS-CDC. (b) Proposed NMOS-CDC.

whose relations to the input current of this cell (Ii_i) are expressed as follow:

$$I_{O1i} = a_i \frac{Ii_i}{2} \quad (1)$$

$$I_{O2i} = \overline{a}_i \frac{Ii_i}{2} \quad (2)$$

$$I_{O3i} = \frac{Ii_i}{2} \quad (3)$$

Where a_i is the digital control bit of this cell. As shown from Fig. 1(a), I_{O3i} of the CDC_i is used as the input current of the next stage Ii_{i-1} and I_{O30} is added to I_{O1}. Therefore, I_{O1} and I_{O2} of the CDN are given by:

$$I_{O1} = I_{O30} + \sum_{i=0}^{i=n-1} I_{O1i} = \frac{1}{2^n}\left(1 + \sum_{i=0}^{i=n-1} 2^i a_i\right) Ii \quad (4)$$

$$I_{O2} = \sum_{i=0}^{i=n-1} I_{O2i} = \frac{1}{2^n}\left(\sum_{i=0}^{i=n-1} 2^i \overline{a}_i\right) Ii \quad (5)$$

$$\alpha = \frac{I_{O1}}{Ii} = \frac{1}{2^n}\left(1 + \sum_{i=0}^{i=n-1} 2^i a_i\right) \quad (6)$$

Hence, the current gain (α) of the proposed CDN is digitally controlled where α is less than, or equal to, one.

The proposed NMOS-CDC is shown in Fig. 2(a). M_{1i} and M_{2i} are matched and assumed to be operated in saturation region. M_{4i} and M_{5i} are matched and operate as current sources with drain current equal to I_{B1}. Also, M_{3i} operates as current source with drain current equal to $2I_{B1}$. Using the drain current equation of MOS transistor in saturation region, the input current of the CDC_i (Ii_i) is divided equally between the matched transistors M_{1i} and M_{2i} as shown in equation (7).

$$I_{M1i} = I_{M2i} = I_{B1} - \frac{Ii_i}{2} \quad (7)$$

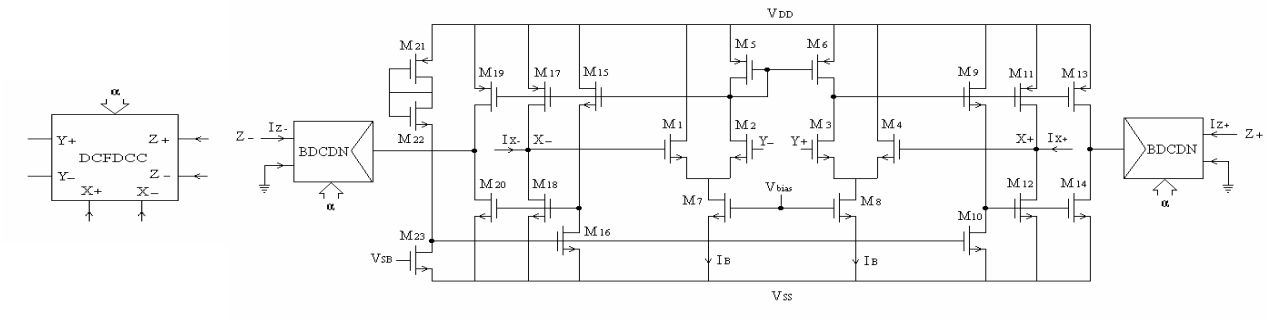
Hence, a current equals $Ii_i/2$ is transferred to I_{O3i} as stated in equation (3). Only one transistor of M_{6i} or M_{7i} is on at a time due the value the digital control bit a_i. Hence, the current of $Ii_i/2$ is either switched to I_{O1i} or I_{O2i} as given in equations (1) and (2). The operation of the PMOS-CDC shown in Fig. 2(b) is typically as its NMOS counterpart.

III. CMOS REALIZATIONS OF THE DCFDCC

The DCFDCC, represented symbolically as in Fig. 3(a), can be realized using class AB fully differential buffer (FDB) presented in [5] with its output current is sensed and copied to the current port and followed by the proposed bidirectional CDN as shown in Fig. 3(b). The DCFDCC is represented mathematically by the following matrix equation:

$$\begin{pmatrix} V_{Xd} \\ I_{Zd} \\ I_{Yd} \end{pmatrix} = \begin{pmatrix} 0 & 0 & 1 \\ \alpha & 0 & 0 \\ 0 & 0 & 0 \end{pmatrix} \begin{pmatrix} I_{Xd} \\ V_{Zd} \\ V_{Yd} \end{pmatrix} \quad (8)$$

Where, $V_{Xd} = (V_{X+})-(V_{X-})$, $V_{Yd} = (V_{Y+})-(V_{Y-})$, $I_{Zd} = (I_{Z+})-(I_{Z-})$, $I_{Xd} = (I_{X+})-(I_{X-})$, and $(I_{Y+}) = (I_{Y-}) = 0$. The FDB is consisting of two matched differential pairs (M_1-M_2) and (M_3, M_4), matched biasing currents sources transistors (M_7, M_8), matched active load transistors (M_5-M_6), and two class AB output stages (M_9-M_{12}, and M_{15}-M_{18}, and the biasing of the output stage M_{21}-M_{23}). The differential input is applied to the two high impedance terminals of the NMOS transistors M_2 and M_3. The tail current transistors M_7 and M_8 carry equal bias current I_B and $I_{M2}=I_{M3}$ by the current mirror action



(a) (b)

Fig. 3: (a) Symbol of the DCFDCC (b) CMOS Realization of the DCFDCC

of transistors M_5 and M_6. Hence, the two matched differential pairs carry equal differential and common mode current values. Therefore:

$$(V_{X+})-(V_{X-})=(V_{Y+})-(V_{Y-}) \quad (9)$$

Transistors M_{13}-M_{14} and M_{19}-M_{20} are used to copy the current of the class AB output stages of the FDB and transfer it to the proposed bidirectional CDCs. Hence, the current gain, between X and Z terminals, is linearly proportional to the digitally controlled parameter α as given in equation (8).

The DCFDCC circuit in Fig 3(b) has been simulated using PSPICE with 0.5μm CMOS parameters. The power supply voltages V_{DD} and V_{SS} are balanced (1.5V and -1.5V) respectively. n = 6 bits. In Fig. 4, the differential Z-terminals current of the DCFDCC is shown when the differential Y-terminals voltage is swept from -1 to 1V for different values of the digitally controlled parameter α ranging from 0.125 to 1 with step of 0.125. Z-terminals are loaded by R_{Z+}=R_{Z-}=1KΩ while X-terminals are loaded by R_{X+}=R_{X-}=10KΩ. Fig. 5 shows the AC response of the Z-terminals current for the same α setting of Fig. 4

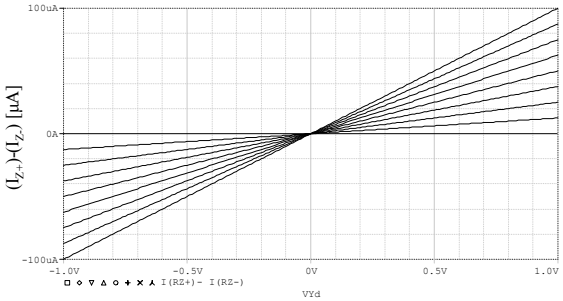


Fig. 4: DC Response of the Z-Terminals Current of the DCFDCC.

As seen in Fig. 5, the bandwidth is approximately constant and equal to 64.6 MHz. The DC response of the X-terminals voltage is shown in Fig. 6.

IV. Digitally Programmable Universal Active Filter

The Single-ended universal-filter presented in [11] can be implemented using DCFDCC in fully differential configuration as shown in Fig. 7. This filter employs five DCFDCC and all-grounded passive elements. This configuration provides several advantages.

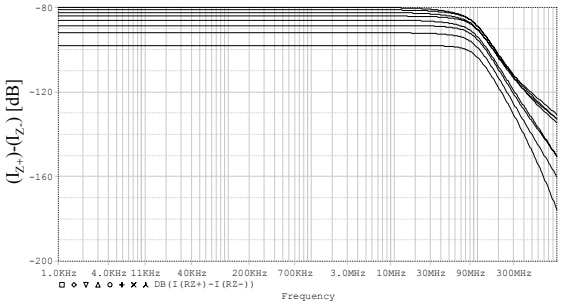


Fig. 5: AC Response of the Z-Terminals Current of the DCFDCC.

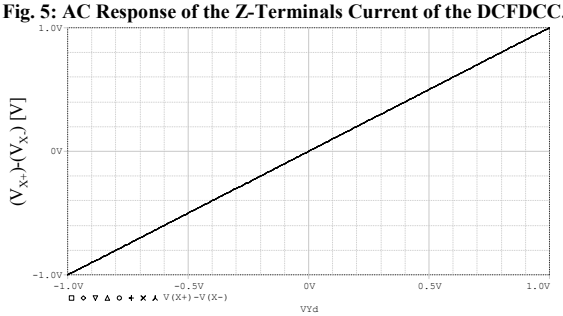


Fig. 6: DC Response of the X-Terminals Voltage of the DCFDCC.

It has infinite input impedance. All elements are grounded. It realizes highpass, bandpass, and lowpass differential voltage responses. Also, ω_0 and Q of the filter can be adjusted independently. By direct analysis, the following transfer functions are obtained:

$$\frac{V_1}{V_i}=\frac{\left(\frac{\alpha_1 R}{R_i}\right)s^2}{D(s)},\quad \frac{V_2}{V_i}=\frac{\left(\frac{\alpha_1\alpha_2 R}{C_1R_1R_i}\right)s}{D(s)},\quad \frac{V_3}{V_i}=\frac{\left(\frac{\alpha_1\alpha_2\alpha_3 R}{C_1C_2R_1R_2R_i}\right)}{D(s)} \quad (10)$$

$$D(s)=s^2+\frac{\alpha_1\alpha_2\alpha_4 R}{C_1R_1R_4}s+\frac{\alpha_1\alpha_2\alpha_3\alpha_5 R}{C_1C_2R_1R_2R_3} \quad (11)$$

Using the following set of the design equation,

$$R_i=R_1=R_2=R_3=R,\quad C_1=C_2=C,\quad \alpha_1=\alpha_5=1,\quad \alpha_2=\alpha_3=\alpha_\omega,\quad \alpha_4=\alpha_Q \quad (12)$$

The ω_0 and Q of the filter will be given by:

$$\omega_0 = \frac{\alpha_\omega}{CR}, \qquad Q = \frac{1}{\alpha_Q}\frac{R_4}{R} \tag{13}$$

As seen from equation (13), the ω_0 and Q of the filter can be independently programmed digitally using α_ω and α_Q respectively without distorting each others.

The circuit of Fig. 7 has been simulated using PSPICE with C=16pF, and R4=0.707R=5KΩ to obtain a maximally flat low pass response for a DC gain of 1 and with digitally tunable f_o. The frequency response of that filter is shown Fig. 8 for different values of the digitally controlled parameter α_ω. Fig. 9 shows the simulated bandpass response for the same circuit for different values of the digitally controlled parameter α_ω while Q is constant at approximately 20.

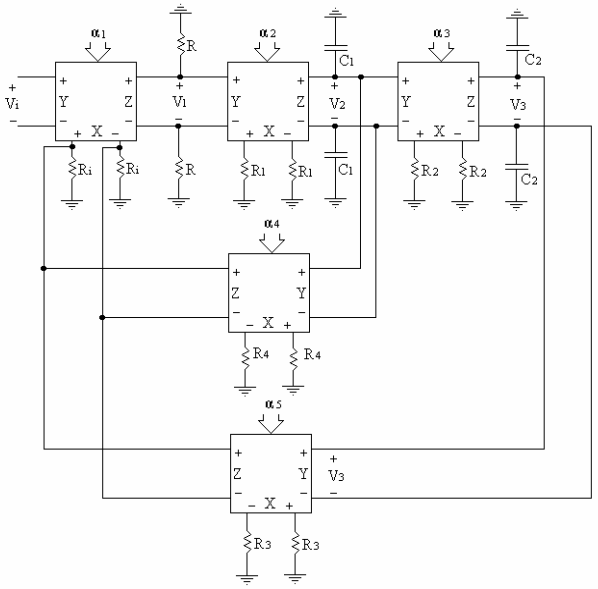


Fig. 7: DCFDCC-Based Universal Active Filter

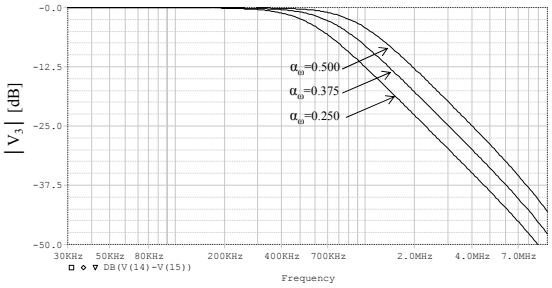


Fig. 8: Magnitude Response of the Differential Voltage Lowpass Output.

V. Conclusion

In this paper, a digitally controlled fully differential current conveyor (DCFDCC) has been presented. A novel current division network (CDN) has been proposed to provide a current gain of the DCFDCC. The DCFDCC provides linearly proportional current gain with the digitally controlled parameter of the CDN. Application of the DCFDCC in realizing second order universal active filter has been given. The proposed blocks and its applications have been confirmed using PSPICE simulation.

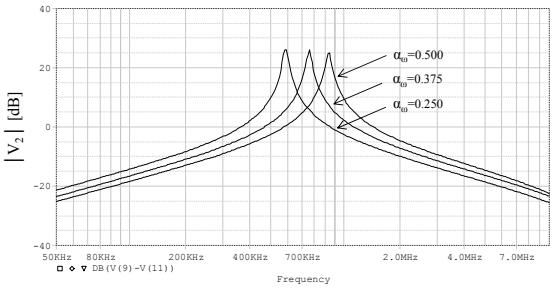


Fig. 9: Magnitude Response of the Differential Voltage Bandpass Output.

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