New Current-Mode and Voltage-Mode CMOS Analog Multipliers

Mohammed A. Hashiesh[1], Soliman A. Mahmoud[1], and Ahmed M. Soliman[2]

1. Electrical Engineering Dept., Cairo University, Fayoum Branch, Egypt.
2. Electronics and Communication Eng. Dept., Cairo University, Cairo, Egypt.

Abstract. In this paper, a four-quadrant current-mode multiplier based on a new squarer cell is proposed. The multiplier has a simple core, wide input current range with low power consumption, and it can easily be converted to a voltage-mode by using a balanced output transconductor (BOTA) [1]. The proposed four-quadrant current-mode and voltage-mode multipliers were confirmed by using PSPICE simulation and found to have good linearity with wide input dynamic range.

Key Words : CMOS Multiplier, Current-mode, Voltage-mode, Transconductance.

I. INTRODUCTION

A multiplication of two signals is one of the most important operations in analog signal processing. The multiplier is used not only as computation building block but also as a programming element in systems such as filters, neural networks, mixers, and modulators in communication systems [2]. Several MOS four-quadrant multipliers have been reported but all can be categorized into two groups based on its MOS operating region, linear and saturation [3]. The operation of the multiplier only in linear or saturation region limits the input-voltage range, so the multiplier presented in [2] has wider input-voltage range as a result of operation in linear and saturation regions complementally.

The analog circuit design using the current-mode approach has recently gained considerable attention. This stems from its inherent advantages of wide bandwidth, high slow rate, low power consumption, and simple circuitry [4-5]. This is clearly obvious in the four-quadrant current-mode multipliers presented in [6-7] which based on current squarer cells.

In this paper a novel four-quadrant current-mode multiplier that has simple core circuit based on a simple novel squarer cell will be proposed. Although this circuit has design trade off among the input current range, the output current dynamic range, and the power consumption, it can be designed to operate with low supply voltage (±1.5V) under low power consumed with acceptable dynamic ranges for both input and output currents. The proposed current-mode multiplier circuit is presented in section II. In section III, balanced output transconductor (BOTA) circuit given in [1] is used to drive the proposed four-quadrant current-mode multiplier. The four-quadrant voltage-mode multiplier has attractive performance that it has very good linearity with wide differential-input voltage range.

The proposed circuits of four-quadrant current-mode and voltage-mode multipliers are simulated using CMOS 0.5 μm technology.

II. CMOS CURRENT-MODE MULTIPLIER

The proposed four-quadrant current mode multiplier is based on a novel squarer cell. The design of the squarer cell and the complete circuit of the multiplier will be given in the following sub-sections.

A. PROPOSED CURRENT-MODE SQUARER CELL

The proposed current-mode squarer cell is shown in Fig. 1. The symbol of the squarer cell is shown in Fig. 1(b) and its CMOS realization is shown in Fig. 1(a). The circuit consists of four transistors; M_1 and M_2 are operated in the saturation region and assumed to be matched, and M_3 and M_4 are operated in the linear region and assumed to be matched also. M_3 and M_4 are equivalently representing grounded resistors with resistance value approximately given by:

$$R = \frac{1}{K_3(V_G - V_T)} \quad (1)$$

Where K_3 is the transconductance parameter of transistors M_3 and M_4, $K_3=\mu C_{ox}(W/L)_3$, μ is the mobility of the carrier, C_{ox} is the gate capacitance per unit area, W is the channel width, L is the channel length, V_G is the gate voltage, and V_T is the threshold voltage.

From Fig. 1(a), assuming that both I_i and $-I_i$ are available, the output current of the squarer I_o is given by:

$$I_O = I_{D1} + I_{D2} \quad (2)$$

Where I_{D1} and I_{D2} are the drain currents of the saturated transistors M_1 and M_2. I_O can be written as follow:

$$I_O = I_{OFF} + KsI_i^2 \quad (3)$$

Where I_{OFF} is the output offset current (at Ii=0A) and is given by:

$$I_{OFF} = K_1(V_{SS} + V_T)^2 \quad (4)$$

And Ks is the squarer gain and is given by:

$$Ks = K_1R^2 \quad (5)$$

Where, K_1 is the transconductance parameter of transistors M_1 and M_2.

From equations (4) and (5), I_{OFF} will be controlled by the transistors aspect ratio $(W/L)_1$ and by the biasing voltage (V_{SS}). The squarer gain Ks will be controlled independently by the resistance R that can be controlled by the voltage V_G and $(W/L)_3$.

0-7803-8575-6/04/$20.00 ©2004 IEEE

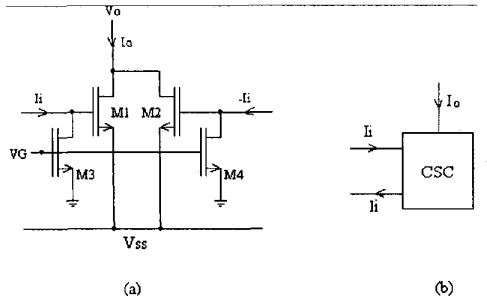

Fig. 1. Proposed Squarer Cell.

B. DESIGN CONSIDRATIONS OF THE PROPOSED SQUARER CIRCUIT

In this section, the design considerations to optimize the input current range, the output current dynamic range, static power dissipation and the output voltage (V_O) that can be driven by the circuit will be discussed.

Assuming that M_3 and M_4 are carefully designed to operate in the linear region with equivalent grounded resistance R, The operation of the squarer circuit is restricted by the saturation condition of the MOS transistors M_1 and M_2. The following conditions can be driven for symmetrical input current range ($|I_{i\text{-min.}}| = I_{i\text{-max.}}$).

$$|RI_i| \le |V_{SS} + V_T| \tag{6}$$

$$V_{O\text{-min.}} = |V_{SS}| - 2V_T \tag{7}$$

Using the above two equations in addition to equations (3) to (5), the input current range ($|I_i|_{max}$), and the output current dynamic range ($I_{O\text{-DR}}$) are given by:

$$|I_i| \le \frac{|V_{SS} + V_T|}{R} \tag{8}$$

$$I_{O\text{-DR}} = K_1 R^2 (I_i)^2 \le I_{OFF} \tag{9}$$

The static power dissipation is linearly proportional to I_{OFF}, so trade off among the input current range, the output current dynamic range, and the static power dissipation is clearly obvious.

C. CURRENT-MODE MULTIPLIER

The block diagram of the proposed four-quadrant current-mode multiplier is shown in Fig. 2(a). The multiplier circuit consists of four similar squarer cells and a current-subtraction circuit. The CMOS realization of the current-mode multiplier is shown in Fig 2(b). Transistors (M_{1A} to M_{4D}) are the squarer cells, transistors (M_5 to M_8) represent a current subtraction circuit to obtain a single ended output current I_O, which is given by:

$$I_O = I_{O1} - I_{O2} \tag{10}$$

Therefore, the output current of the multiplier (I_O) is given by:

$$I_O = (2K_1 R^2) I_X I_Y \tag{11}$$

This topology achieves multiplication and simultaneously cancels out all higher order components of I_X and I_Y. The gain of the multiplier is $2K_1R^2$ where K_1 is the transconductance parameter of the saturated transistors M_{1A} to M_{2D} and R is the equivalent grounded resistance of the linear transistors M_{3A} to M_{4D}.

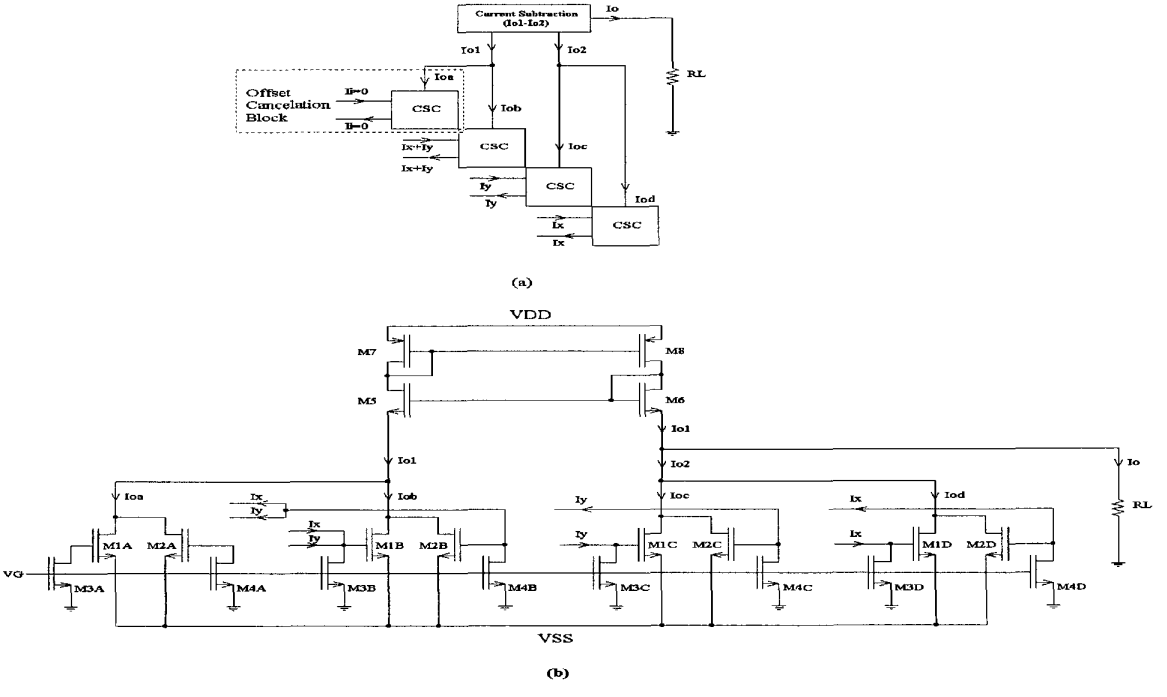

Fig. 2. Proposed Current-Mode Multiplier.

III. FOUR QUADRANT CMOS VOLTAGE-MODE MULTIPLIER

The four-quadrant current-mode multiplier discussed in section II not only has simple core and can be designed to have wide input range, but also it can be easily converted to operate in voltage-mode using balanced output transconductor (BOTA) given in [1]. The BOTA circuit is shown in Fig. 3. It is suitable for driving the proposed current-mode multiplier where it has two balanced output currents as shown in Fig. 3(a).

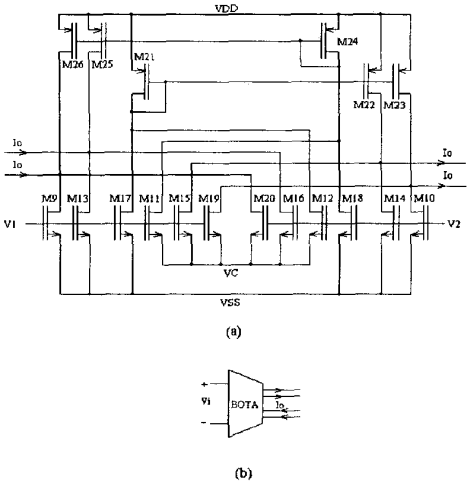

Fig. 3. Balanced Output Transconductor (BOTA) [1].

The BOTA operates as a balanced output transconductor with a programmable transconductance G that controlled by the control voltage V_C and is given by:

$$G = K_9(V_C - V_{SS}) \quad (12)$$

And the output current of the BOTA is given by:

$$I_O = G(V_1 - V_2) = K_9(V_C - V_{SS})(V_1 - V_2) \quad (13)$$

Where K_9 is the transconductance parameter of transistors M_9 to M_{20}, and $(V_1\text{-}V_2)$ is the differential input voltage of the BOTA respectively. The symbol of the used BOTA is shown in Fig. 3(b).

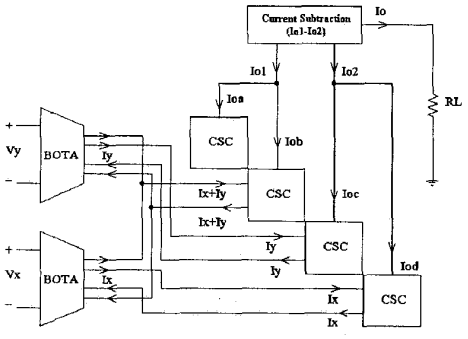

Fig. 4. Block Diagram of The Proposed Voltage-Mode Multiplier.

The complete block diagram of the proposed four-quadrant voltage-mode multiplier is shown in Fig. 4. It is consist of the current-mode multiplier of Fig. 2 driven by two BOTA circuits of Fig. 3.

Assuming that V_X and V_Y are the two differential input voltages to the two BOTAs; the overall output current of the multiplier can be deduced using equations (11), and (13) as follow:

$$I_O = 2K_1R^2(K_9(V_C - V_{SS}))^2 V_X V_Y \quad (14)$$

Equation (14) yields the voltage multiplication of the differential input voltages V_X and V_Y. The overall multiplier gain is $(2K_1R^2(K_9(V_C\text{-}V_{SS}))^2)$ which is controlled by the control voltage V_C of the BOTA circuit.

IV. SIMULATION RESULTS

Simulation results are given in this section using PSPICE with 0.5μm CMOS parameters (level3). The power supply voltages V_{DD} and V_{SS} are balanced (1.5V and -1.5V) respectively.

The DC transfer characteristics of the voltage-mode multiplier shown in Fig. 4 are shown in Fig. 5. The aspect ratios of the transistors are given in Table 1, and R_L=10KΩ. It is clear that the voltage-mode multiplier has wide differential-voltage input range with excellent output linearity. The differential-voltage input varies from -1V to 1V.

The frequency characteristics of the multiplier are shown in Fig. 6, where, V_Y is set to 1V DC and V_X is the AC-varying signal with 1V magnitude. The multiplier has a bandwidth of 25.34MHz.

Fig. 7 shows the use of the multiplier as an analog amplitude modulator. V_X is the sinusoidal modulating signal with magnitude equal to 1V and frequency (*fx* =1 KHz) while V_Y is the sinusoidal carrier with amplitude equal to 1V and frequency (*fy* =20 KHz).

The simulation results of the proposed four-quadrant current-mode and voltage-mode multipliers are summarized in Table 2.

Table 1. Aspect Ratios of The Proposed Multiplier

Transistor	Aspect ratio W/L [μm/ μm]
M_{1A}, M_{2A}, M_{1B}, M_{2B}, M_{1C}, M_{2C}, M_{1D}, M_{2D}.	4/6
M_{3A}, M_{4A}, M_{3B}, M_{4B}, M_{3C}, M_{4C}, M_{3D}, M_{4D}.	14/12
M_5, M_6.	90/4
M_7, M_8.	180/4
M_9, M_{10}, M_{11}, M_{12}, M_{13}, M_{14}, M_{15}, M_{16}, M_{17}, M_{18}, M_{19}, M_{20}.	2/3
M_{21}, M_{22}, M_{23}, M_{24}, M_{25}, M_{26}.	20/2

Table 2. Summary of The Simulation Results of The Proposed Current-Mode and Voltage-Mode Multipliers.

	Current-Mode Multiplier	Voltage-Mode Multiplier
Supply voltage	±1.5V	±1.5V
Input range	±60μA	±1V
Static power consumption (@I_X=I_Y=0μA) (@V_X=V_Y=0V)	0.671mW	1.6mW
Maximum power consumption (@I_X=I_Y=60μA) (@V_X=V_Y=1V)	0.72mW	1.85mW
Bandwidth	31MHz	25.34MHz
%THD (@I_Y=50μA, I_X=50sin(2πf_x)μA, f_x = 1MHz) (@V_Y=1V, V_X=1sin(2πf_x)V, f_x = 1MHz)	4.485%	4.667%

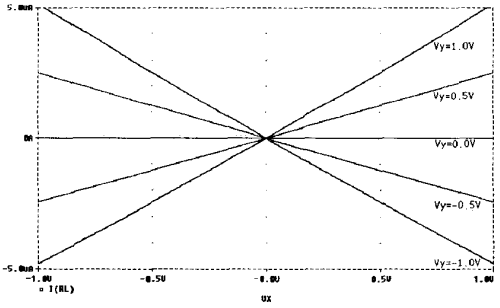

Fig. 5. DC Transfer Characteristics of The Voltage-Mode Multiplier.

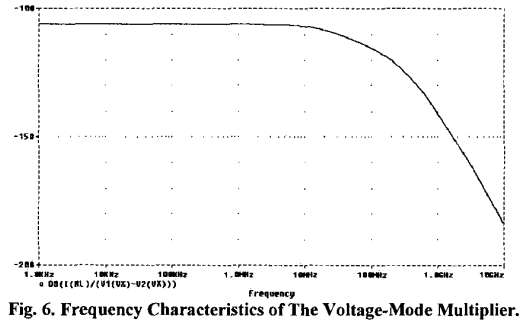

Fig. 6. Frequency Characteristics of The Voltage-Mode Multiplier.

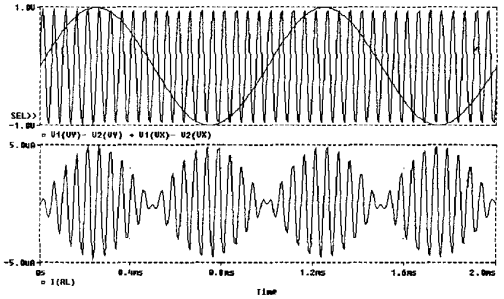

Fig. 7. The Voltage-Mode Multiplier as an Analog Amplitude Modulator.

V. CONCLUSION

In this paper, a novel four-quadrant current-mode multiplier based on a novel squarer cell has been proposed. This multiplier has simple core and can be designed to have wide input current range with low power consumption, moreover it can be easily converted to voltage-mode by using BOTA circuit with wide input voltage range. The proposed circuits were confirmed by using PSPICE simulation and found to have good linearity with wide input dynamic range. The simulations also included the power consumption, the frequency bandwidth, and %THD.

REFERENCES

[1] S. A. Mahmoud, A. M. Soliman,"CMOS Balanced Output Transconductor and applications for analog VLSI," Microelectronics journal, vol. 30, pp. 29-39, 1999.

[2] T. Suzuki, T. Oura, T. Yoneyama, and H. Asai," Design And Simulation Of 4Q-Multiplier Using Linear And Saturation Regions Of MOSFET Complementally," IEICE Trans. Fundamentals, vol. E85-A, pp. 1242-1248, 2002.

[3] G. Han, and E. Sinencio, "CMOS Transconductance Multiplier: A Tutorial," IEEE trans. Circuit Syst. II, vol. 45, pp. 1550-1563, 1998.

[4] C. Toumazou, J. Lidgey, and D. Haigh, Analogue IC Design: The Current Mode Approach. London, U.K.: peregrinus, 1990.

[5] H. A. Alzaher, H. Elwan, and M. Ismail, "A CMOS Fully Balanced Second-Generation Current Conveyor," IEEE trans. Circuit Syst. II, vol. 50, pp. 278-287, 2003.

[6] B. D. Liu, C. Y. Hang, and H. Y. Wu, "Modular Current-Mode Defuzzification Circuit For Fuzzy Logic Controls," Electronics lett., vol. 30, pp. 1287-1288, 1994.

[7] K. Tanno, O. Ishizuka, and Z. Tang, "Four-Quadrant CMOS Current-Mode Multiplier Independent of Device parameters," IEEE trans. Circuits Syst. II, vol. 47, pp. 473-477, 2000.