ISCAS 2000 - IEEE International Symposium on Circuits and Systems, May 28-31, 2000, Geneva, Switzerland

A NOVEL CMOS FOUR QUADRANT MULTIPLIER BASED ON LINEARIZATION OF THE LONG TAIL DIFFERENTIAL PAIR

Aly M. Ismail and Ahmed M. Soliman
Electronics and Communication Engineering Department, Cairo University, Giza, Egypt.

ABSTRACT

In this paper, a novel circuit design technique for linearizing differential pairs is proposed. It is shown that the proposed linearized transconductor offers excellent linearity and exceptionally wide operating range which makes it suitable to operate in analog processing applications. PSpice simulation results are given.

1. INTRODUCTION

Transconductance elements are useful building blocks in analog signal processing systems especially in continuous time filters and four-quadrant multipliers [1-7]. Many implementations have been reported in the literature in order to obtain highly linear transconductors. Among these realizations, the realizations based on the long Tail differential Pair (LTP) have received a great interest since they offer a relatively low level of distortion because of second order effects like body-effect and mobility degradation. In the literature, several techniques have been described in order to extend the linearity range of the LTP [1-7]. In this paper, the analysis of the LTP is first reviewed, then a novel dynamically-biased squaring circuit is proposed. This squaring circuit is then used to linearize the LTP. Finally, using the same approach, a wide-range highly-linear four-quadrant multiplier circuit is proposed. Simulation results are given to show that the novel linearizing technique gives an excellent performance.

2. LONG TAIL DIFFERENTIAL PAIR

The differential pair transconductor represents a useful analog building block due to its simplicity and its high frequency response [4-7]. However, the nonlinearity generated by the constant current operation always restricts the scope of this structure. Consider the matched differential pair shown in Fig. 1. All the transistors used are assumed to be operating in the saturation region, where the drain current of the NMOS transistor operating in that region (neglecting the channel length modulation effect) is given by:

$$I = \frac{K_n}{2}(V_{GS} - V_T)^2 \quad (1)$$

$$K_n = (\mu_n C_{ox})\left(\frac{W}{L}\right) \quad (2)$$

where V_T is the threshold voltage, K_n is the transconductance parameter, μ_n is the effective carrier mobility, C_{OX} is the gate oxide capacitance per unit area, W is the channel width and L is the channel length.

Assuming that all body terminals are connected to the proper supply voltages. The output current as a function of the two input voltages V_1 and V_2 is obtained as:

$$I_{OUT} = \sqrt{K_n I_{SS}}(V_1 - V_2)\sqrt{1 - \frac{K_n(V_1 - V_2)^2}{4I_{SS}}} \quad (3)$$

The differential input voltage $V_i = V_1 - V_2$ is therefore limited to the range:

$$-\sqrt{\frac{2I_{SS}}{K_n}} \le V_i \le \sqrt{\frac{2I_{SS}}{K_n}} \quad (4)$$

which usually limits the operation of the circuit since the ratio I_{SS}/K_n cannot be raised high enough without limiting the common-mode operating range. In addition, the output current is only linear within approximately half of this range due to the effect of the non-linearity term given by. (3).

3. THE ADAPTIVELY BIASED SOURCE COUPLED DIFFERENTIAL PAIR

Consider the modified source-coupled differential pair shown in Fig.2, where all transistors are assumed to be operating in the saturation region. The adapted current source I_C is used to cancel the nonlinearity term and extend the operating region.

In order to cancel the nonlinearity term of the LTP of Fig.2, and from (3), it is seen that the current tail must be given by:

$$I_{SS} = I_B + I_C \quad (5)$$

where

$$I_C = \frac{K_n}{4}(V_1 - V_2)^2 \quad (6)$$

where I_{SS} is the effective current tail value delivered to the differential pair, I_C is the compensating current tail that extends the linearity range of the differential pair and I_B is the uncompensated current tail of the differential pair and K_n is the transconductance parameter of the transistors M1and M2. In this case, the output current is given by:

$$I_{OUT} = \sqrt{K_n I_B}(V_1 - V_2) \quad (7)$$

It is noted that for M1 and M2 to be on, the linearity range is limited to the value:

$$-2\sqrt{\frac{I_B}{K_n}} < (V_1 - V_2) < 2\sqrt{\frac{I_B}{K_n}} \quad (8)$$

0-7803-5482-6/99/$10.00 ©2000 IEEE

It is clear that a squarer circuit that performs the relation given by (6) is needed. In the following section, a novel squaring circuit based on a modified LTP with no limitation on its differential mode range is presented. The non-idealities represent the basic source of linearity error of the transconductor. One can assume that the transistor channels are enough long to neglect the effect of channel length modulation. Since the transistors M1a-M3 have a common source, it is clear that there will not be a contribution of the body-effect in the distortion and the transconductor performance is independent of variations in the threshold voltage assuming perfect matching. Consequently, the main source of distortion that needs to be studied carefully is the mobility reduction that results from the vertical surface electric field. Due to this effect, the μ factor in (2) is given by $\mu n=\mu_o/[1+\theta(V_{GS}-V_T)]$ where μ_o is the zero field mobility of carriers and θ is a constant. The result is a third-order harmonic distortion of value:

$$HD3=\frac{\theta(V_1-V_2)^2}{32\sqrt{\frac{I_B}{K_n}}} \qquad (9)$$

It is clear from (9) that the effect of mobility reduction on the linearity is very small. This is obvious since in the case of current tail compensation, V_S follows the common mode voltage of the differential input voltage, thus verifying the analysis held in [6] proving that Antiphase Common-Source Pair topologies result in higher linearity range and much lower distortion levels when compared with cross coupled pair ones. Therefore, the proposed transconductor is expected to have a very low distortion level.

4. THE PROPOSED SQUARING CIRCUIT

The main idea is to use negative feedback in order to transform the LTP into a squaring circuit. By taking the absolute value of the output current of the LTP, one obtains:

$$|I_{OUT}|=\sqrt{K_{n1}I_C}\,|V_1-V_2|\sqrt{1-\frac{K_{n1}(V_1-V_2)^2}{4I_C}} \qquad (10)$$

where K_{n1} is the transconductance parameter of each of the matched transistors M5 and M6, of the circuit of Fig. 3.
The aim is to apply a negative feedback action such that this value can be adjusted to the value:

$$|I_{OUT}|=\frac{I_C}{a} \qquad (11)$$

where I_C in this case is a variable that represents the degree of freedom in this feedback action. Accordingly, when substituting from (10) in (11), one obtains:

$$4I_C^2-4K_{n1}a^2(V_1-V_2)^2I_C+K_{n1}^2a^2(V_1-V_2)^4=0 \qquad (12)$$

The result is an equation of the second degree whose unique solution is given by:

$$I_C=\frac{1}{2}K_{n1}(V_1-V_2)^2\left(a^2+\sqrt{a^4-a^2}\right) \qquad (13)$$

where the second solution for (12) is refused for inconsistency since it does not satisfy the condition on the operating range of the LTP defined by (4). In order to realize the negative feedback action mentioned above, it is noted that the absolute value of the output current in the LTP is also given by: -

$$|I_{OUT}|=2I_{MAX}-I_C \qquad (14)$$

Substituting for $|I_{OUT}|$ in (11), one obtains:

$$\frac{I_C}{I_{MAX}}=\frac{2a}{a+1} \qquad (15)$$

So by simply picking up the maximum current of the two branches of the LTP and feeding it back to the current tail I_C according to (15), the required squarer circuit can be obtained.
Consider the circuit shown in Fig.3, the current-mode maximum circuit (M9-M14) reported in [8] is applied to the LTP formed from (M15, M16 and M7) and picks up the maximum current of the two branches. Consequently, the signal needed to produce the necessary current tail I_C is fedback as required and scaled by adjusting the aspect ratios of M7-M12. When using the proposed squaring circuit for the adaptive biasing of the LTP as shown in Fig.4, and in order to obtain the required value for the current tail as defined by (13) it is necessary to have:

$$K_{n1}\left(a^2+\sqrt{a^4-a^2}\right)=\frac{K_n}{2} \qquad (16)$$

Therefore, defining

$$a^2+\sqrt{a^4-a^2}=m \qquad (17)$$

where *m* is a rational number. Solving (17) for *a*, one obtains:

$$a=\frac{m}{\sqrt{2m-1}} \qquad (18)$$

The aim is to obtain *a* as a rational number in order to realize (18) by using simple current mirrors. In order to do this, $(\sqrt{2m-1})$ must be a real number.

This is realized by taking $m=\frac{5}{2}$. In this case, one obtains:

$$a=\frac{5}{4} \qquad (19)$$

Substituting in (13), the current flowing in M13 is given by:

$$I_C=\frac{5K_{n1}}{4}(V_1-V_2)^2 \qquad (20)$$

Substituting in (15), one obtains:

$$\frac{I_C}{I_{MAX}}=\frac{2a}{a+1}=\frac{10}{9} \qquad (21)$$

which can be realized by choosing appropriate values of the aspect ratios of M7-M8 and M9-M11 By choosing $K_n=5\,K_{n1}$, one adjusts the aspect ratios of M7-M11 1 in order to satisfy the value of *a*.

5. FOUR QUADRANT MULTIPLIER

The circuit shown in Fig.5 which has been introduced in [4], is a folded CMOS Gilbert's cell [5]. This circuit can be considered as the voltage controlled version of the LTP. This has been achieved using two NMOS matched differential

pairs as well as another PMOS differential pair onto which the control voltages are applied.

The output current can be obtained from the currents shown in Fig.5 as follows:

$$I_O = (i1 - i2) + (i3 - i4) \quad (22)$$

The given circuit consists of two linearized LTP transconductors with different effective current tails I_{SS1} and I_{SS2} . Two compensating current sources are added to the biasing current sources of both the two LTPs. The output current is thus given by:

$$I_{OUT} = \sqrt{K_n}\left(\sqrt{I_{SS1}} - \sqrt{I_{SS2}}\right)(V_1 - V_2) \quad (23)$$

where

$$I_{SS1} = I_{BIAS} - I_5 = I6 \quad (24)$$

$$I_{SS2} = I_{BIAS} - I_6 = I5 \quad (25)$$

therefore:

$$\left(\sqrt{I_{SS1}} - \sqrt{I_{SS2}}\right) = \left(\sqrt{I_6} - \sqrt{I_5}\right) = \sqrt{\frac{K_p}{2}}\left((V_X - V_4) - (V_X - V_3)\right) \quad (26)$$

Hence substituting in (23), the output current is then given by:

$$I_{OUT} = \sqrt{\frac{K_n K_p}{2}}(V_1 - V_2)(V_3 - V_4) \quad (27)$$

This expression is valid provided that:

$$-\sqrt{\frac{2I_B}{K_p}} < (V3 - V4) < \sqrt{\frac{2I_B}{K_p}} \quad (28)$$

$$-2\sqrt{\frac{\min(I5, I6)}{K_n}} < (V1 - V2) < 2\sqrt{\frac{\min(I5, I6)}{K_n}} \quad (29)$$

Hence by choosing an appropriate value for I_B, the required input operating range can be obtained.

6. PSPICE SIMULATIONS

Performances of both the squaring circuit shown in Fig. 3 and the linearized LTP shown in Fig.4 are simulated using PSpice. Transistors aspect ratios are given in Table 1 and 0.5μm CMOS process are used. Supply voltages used are given by: V_{DD}= -V_{SS}=1.5V and IB is set to 15μA.

Fig. 6 shows the output current I_C of the squarer circuit versus V_i which is scanned from –0.8V to 0.8V. Simulation results confirm the validity of (17).

Fig.7 shows the output current I_{OUT} for the linearized LTP and for the ordinary LTP versus V_i which is scanned from – 0.8V to 0.8V. It is seen that the linearity range becomes very wide due to the new linearization technique. Also, simulation results show that for an input of 0.6 Vp-p, the THD was less than 0.026% assuming perfect matching. Fig.8 shows the output current I_{OUT} for the four-quadrant multiplier versus V_i which is scanned from –0.7V to 0.7V for different (V_3-V_4) values.

7. CONCLUSION

A wide linear range four quadrant multiplier has been presented based on a new linearization technique for the LTP. Simulations results confirm the analysis which makes this technique very suitable for many applications in analog signal processing.

8. REFERENCES

[1] H. Khorramabadi, " High Frequency CMOS continuous filters", Ph.D. Dissertation, University of California, Berkeley, USA ,1985.

[2] A. Nedungadi and T.R. Viswanathan " Design of linear CMOS transconductance elements", IEEE Trans. Circuits Syst., vol. 31, pp.891-894, 1984.

[3] S. A. Mahmoud and A.M. Soliman " New CMOS differential difference transconductors and application to fully differential filters suitable for VLSI", Microelectronics Journal, vol. 30 , pp. 169-192, 1999.

[4] J. N. Babanezhad, and G. C. Temes "A 20-V four-quadrant CMOS analog multiplier", IEEE J. Solid State Circuits, , vol. 20, pp.1158-1168, 1985.

[5] B. Gilbert, New analog multiplier opens to powerful function synthesis, Microelectronics Journal, vol. 8, pp.26-36, 1976.

[6] G. Wilson and P. K. Chan, Comparison of four CMOS transconductors for fully integrated analogue filter applications, IEE Proceedings-G, vol.138, pp.683-689, 1991.

[7] A.M. Ismail, S. K. Elmeteny and A.M. Soliman, "A new Family of CMOS highly linear transconductors based on differential pairs", Microelectronics Journal, vol.30, pp.753-767, 1999.

[8] I. Opris, Rail to rail multiple input min/max circuits, IEEE Transactions on Circuits and Systems II, vol. 45, pp.137-140, 1998.

Table 1

Transistor	Aspect Ratio
M1-M2	2.5/1.5
M3-M4	5/3
M5	6/1.5
M6-M8	54/1.5
M9-M10	1/1
M11-M12	5/3
M13	15/1.5
M14-M15	0.5/1.5
M16	1/9
M17	1/1

The aspect ratios of the transistors used in Fig. 4.

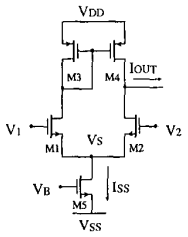

Fig.1 The ordinary LTP transconductor circuit.

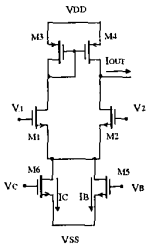

Fig.2 The linearized LTP transconductor circuit.

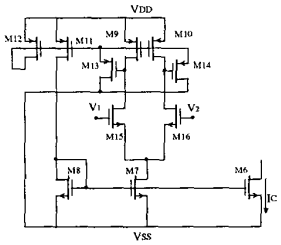

Fig.3 The proposed squaring circuit.

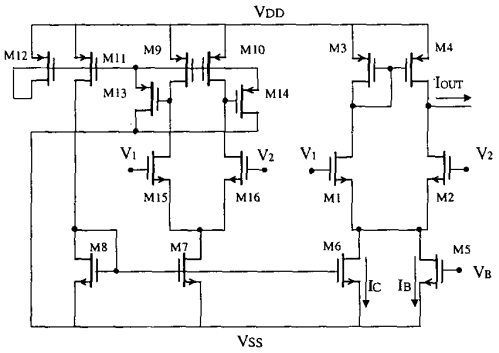

Fig.4 The complete linearized LTP circuit.

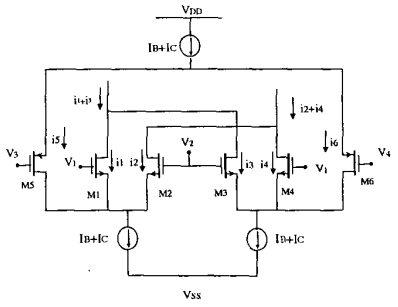

Fig.5 The proposed analog four-quadrant multiplier circuit.

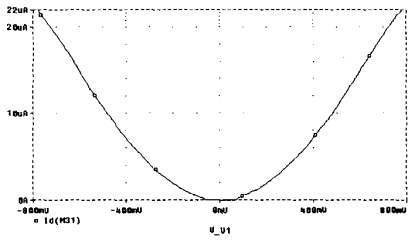

Fig.6 The I-V characteristics of the proposed squaring circuit.

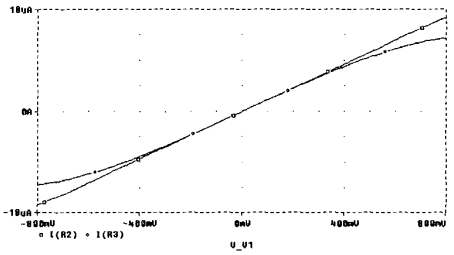

Fig.7 The I-V characteristics of the linearized LTP versus the ordinary LTP.

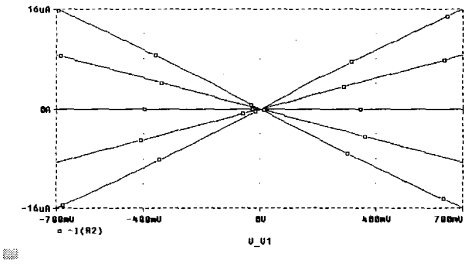

Fig.8 The I-V characteristics of the analog four quadrant multiplier circuit for diffenrent values of (V_3-V_4).