THE CURRENT-FEEDBACK DIFFERENTIAL DIFFERENCE AMPLIFIER: NEW CMOS REALIZATION WITH RAIL TO RAIL CLASS-AB OUTPUT STAGE

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ABSTRACT

A CMOS realization of the current-feedback differential difference amplifier (CFDDA) is proposed. The CFDDA circuit is realized using a wide input range dependent load transconductor (DTA) with three independent input voltages and a rail to rail class- AB voltage buffer. The CFDDA circuit is used to realize a MOS-C oscillator suitable for VLSI. PSpice simulation results for the CFDDA circuit and for its based MOS-C oscillator are also given.

1. INTRODUCTION

The operational amplifier (op-amp) is one of the most important analog integrated circuit building blocks. The classical op-amp acts as a device which if completed with a negative feedback loop, adjusts its output in order to reduce the differential input voltage to a negligible value. For an ideal op-amp with infinite gain this voltage goes to zero. If the voltage at the non-inverting input terminal is called V1 and the voltage at the inverting terminal input is V2 as shown in Fig.1(a) , the basic equation that characterizes the operation of the op-amp is given by:

$$V_1 = V_2 \qquad (1)$$

This equation shows that the op-amp operation is mainly based on the comparison of the two input voltages. This comparing character makes it well suited for monolithic integration despite the strong temperature and process dependence of most device parameters. Since the introduction of the first commercially monolithic op-amp (Fairchild's μA709 produced in 1965) there have been steady evolutionary improvements in performance. However the most revolutionary development has been the emergence in the late of 1980's of an op-amp with an entirely new architecture, now available from several analog semiconductor manufactures. This new device is referred to as a current-feedback op-amp (CFOA) shown in Fig.1(b), also called the transimpedance amplifier [1]-[5]. The CFOA has the advantages, over the classical op-amp, of constant bandwidth which is independent on the closed loop gain and its high slew rate.

This type of op-amp has found wide use in high frequency applications [6]. Also, the concept of the op-amp has been extended to a circuit which compares two differential input voltage signals in contrast to an ordinary op-amp which compares single - ended voltages only. This circuit is the differential difference amplifier (DDA) whose symbol is shown in Fig.1(c) [6]. In a closed loop operation, the DDA forces two differential voltages to the same value, the basic equation that characterizes the operation of the DDA is given by:

$$V_1 - V_2 = V_3 - V_4 \qquad (2)$$

According to [7-10] many interesting circuits can be realized using the DDA with low component count and without matching requirements of components external to the DDA as in the case of the op-amp. The objective of this work is to propose a new analog building block that combines the advantages of the DDA over the op-amp and also the advantages of the CFOA over the op-amp. This block is the current-feedback differential difference amplifier (CFDDA) [2] whose symbol is shown in Fg.1(d). The operation of the CFDDA is described by the following equations :

$$V_4 = V_1 - V_2 + V_3 \qquad (3)$$

$$V_o = R_o I_x \qquad (4)$$

Where Ro is the transresistance gain of the CFDDA, as $R_o \to \infty$ and a negative feedback is applied , eqn.(4) reduces to:

$$I_x = 0 \qquad (5)$$

In this paper, a new CMOS realization of the CFDDA is given in section II. The application of the CFDDA in realizing a MOS-C oscillator suitable for VLSI is given in section III. PSpice simulation results of the CFDDA circuit and for the oscillator circuit which verify the analytical results, are also given.

2. THE PROPOSED CMOS CFDDA CIRCUIT

The CFDDA is realized using a wide input range dependent load transconductor (DTA) with three independent input voltages V_1, V_2 and V_3 and a voltage buffer as shown in Fig.2(a).

The proposed CMOS CFDDA is shown in Fig. 2(b). All the transistors are assumed to be operating in the

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saturation region with their sources connected to their substrates. The drain current of the NMOS transistor in that region is given by:

$$I_D = \frac{K}{2}(V_{GS} - V_T)^2 \quad (6)$$

where $K = \mu_n C_{ox}(W/L)$, (W/L) is the transistor aspect ratio, μ_n is the electron mobility, C_{ox} is the gate oxide capacitance per unit area, and V_T is the threshold voltage (assumed to be the same for all transistors). Transistors M1-M4 are matched transistors. By the current mirroring action of transistors M5 and M6, the current of the transistor M3 is forced to carry a similar current as M2, therefore

$$V_2 - V_{S1} = V_3 - V_{S2} \quad (7)$$

As the result of the biasing current of the differential pair M1 and M2 is equal to the biasing current of the differential pair M3 and M4 , hence

$$V_1 - V_{S1} = V_4 - V_{S2} \quad (8)$$

From the above two equations , the basic equation that characterize the CFDDA is obtained :

$$V_4 = V_1 - V_2 + V_3 \quad (9)$$

Transistor M7 together with the biasing current from M12 form a negative feedback action which provides the necessary current from the output without changing the voltage V_4. This current is mirrored to the input of the rail to rail buffer formed from the transistors M14-M30 through the transistors M8, M9 and M13. The two differential pair M14,M15 and M16, M17 are used to provide the rail to rail operation. Transistors M14 and M15 conduct till the positive supply rail, while transistors M16 and M17 conduct for signal swing down to the negative supply rail. By the current mirroring action of transistors M18,M19 and M20,M21 the currents are summed at the drain of transistors M14 and M15 as shown in Fig. 2(b). Transistors M22 and M23 force these currents to be equal and hence

$$V_o = I_X R_o \quad (10)$$

Where R_o is the transresistance gain and is given by:

$$R_o = r_{ds8} // r_{ds9} // r_{ds13} \quad (11)$$

To provide a low impedance at the output a suitable buffer circuit should be used. It is worth noting that the traditional source follower is not suitable since it will not provide a rail to rail swing capability. In the proposed circuit, the transistors M26 and M27 form the push pull output stage , transistors M24 and M25 are level shifting transistors providing proper biasing for the transistor M27. If the current is withdrawn from the output terminal then the gate voltages of the transistors M26 and M27 is lowered. Thus the current through transistor M26 increases while that through transistor M27 is decreases. Similarly if the output terminal required to sink current, then the gate voltages of the transistors M26 and M27 is increased. Thus the current through transistor M26 decreases while that through transistor M27 increases. To prevent the crossover distortion both transistors M26 and M27 must be ON when no current is withdrawn from the output terminal (standby). This is achieved by using a suitable gate voltage for the transistor M25 which sets the voltage level shift between the gates of M26 and M27. It is clear that:

$$V_{SG26} + V_{GS24} + V_{GS27} = V_{DD} - V_{SS} \quad (12)$$

and,

$$V_{SG28} + V_{GS29} + V_{GS25} = V_{DD} - V_{SS} \quad (13)$$

Since the matched transistors M24 and M25 have equal currents, they thus have the same gate to source voltage. From eqns. (12) and (13) :

$$\sqrt{\frac{2I_{M26}}{K_P}} + \sqrt{\frac{2I_{M27}}{K_N}} = \sqrt{\frac{2I_{SB}}{K_P}} + \sqrt{\frac{2I_{SB}}{K_N}} \quad (14)$$

where I_{SB} is the current through the current source transistor M30.

In the standby mode, no current is withdrawn from the output terminal hence M26 and M27 have equal currents . Therefore from eqn. (14)

$$I_{M26} = I_{M27} = I_{SB} \quad (15)$$

It is clear that the standby current can be controlled by adjusting the value of I_{SB}

PSpice simulation results for the CFDDA circuit using $1.2\mu m$ technology file (Vendor: ORBIT Semiconductors) were carried out with the transistors aspect ratios as given in Table 1 and with the supply voltages ± 2.5 V. Fig.3(a) and 3(b) represent the output voltage of the CFDDA when used as a voltage amplifier with unity gain and with a gain of two. The frequency response of the CFDDA based non-inverting amplifier circuit with a feedback resistance of 20 $K\Omega$ and the other resistance has been scanned to obtain different gain values is shown in Fig.3(c). It is clear that the amplifier circuit realized from the proposed CFDDA experience no loss of bandwidth when the gain is increased. The standby power dissipation of the CFDDA is less than 3.75mW and the output resistance is less than 200Ω .

3. THE CFDDA BASED MOS-C OSCILLATOR CIRCUIT

According to [7-10] many interesting circuits can be realized using the DDA with low component count and without matching requirements of components external to the DDA as in the case of the op-amp. In this section, the application of the CFDDA in realizing a MOS-C oscillator is presented. The CFDDA-MOS-C oscillator is shown in Fig.4 consists of a negative impedance converter (NIC), realized using a single CFDDA and two MOS transistors, two CFDDA based voltage controlled resistors each realized using a single CFDDA and a MOS transistor operating in the non-saturation region, and two capacitors; where the condition of oscillation is given by :

$$\frac{R_2}{R_1} + \frac{C_1}{C_2} = 1 \quad (16)$$

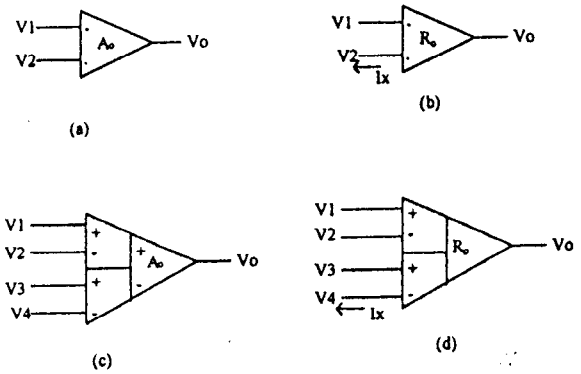

Fig.1 (a) The symbol of the op-amp. (b) The symbol of the CFOA.

(c) The Symbol of the DDA . (d) The Symbol of the CFDDA.

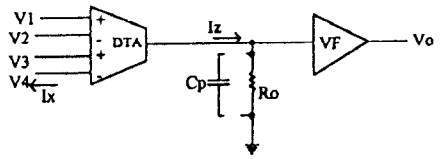

Fig.2(a) The block diagram of the CFDDA.

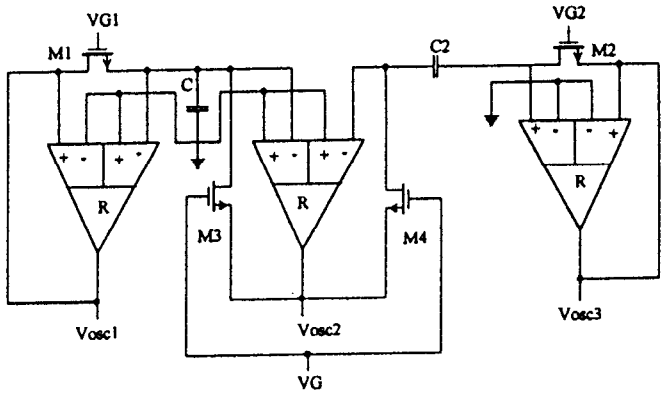

Fig.4 The CFDDA based MOS-C oscillator.

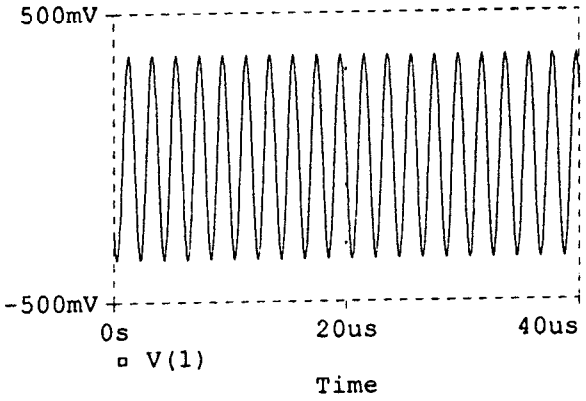

Fig.5 The output waveform Vosc1

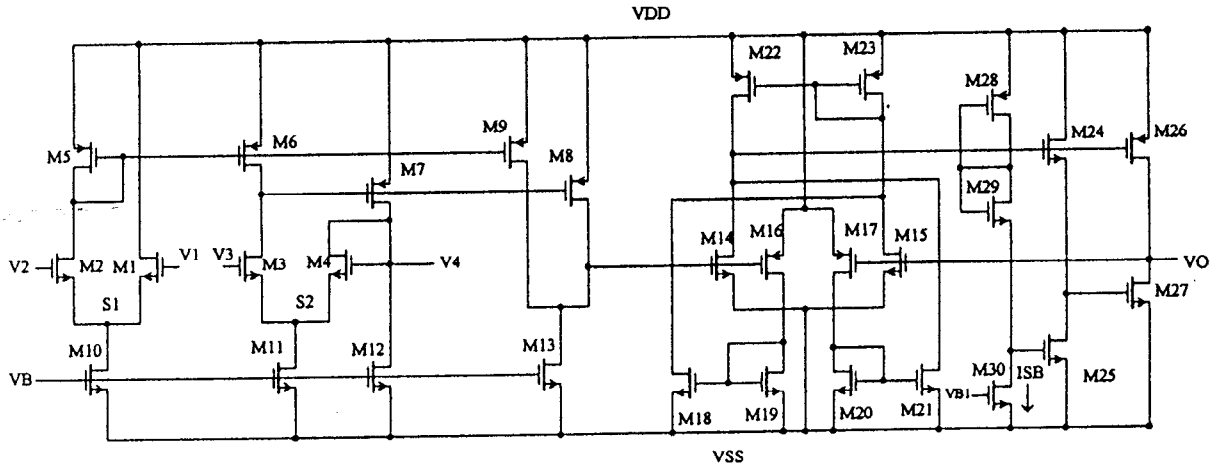

Fig.2(b) The Proposed CFDDA circuit.

taking $\frac{R_2}{R_1} = \frac{C_1}{C_2} = \frac{1}{2}$ (17)

The radian frequency of oscillation is given by :

$$\omega_{osc} = \frac{1}{R_1 C_1} \quad (18)$$

where $R_1 = \frac{1}{2K_1(V_{G1}-V_T)}$ (19)

and

$$R_2 = \frac{1}{2K_2(V_{G2}-V_T)} \quad (20)$$

Fig. 5 shows the output waveform of the oscillator given in Fig.4 where the oscillation frequency is adjusted to 500 KHz . The capacitor's values are C_1 equal to 50pF and C_2 equal to 100pF and $V_{G1} = V_{G2} = V_G = 2.5V$. Note that, V_{osc1} and V_{osc2} are out of phase and shifted only in magnitude by the voltage V_{DS3}.

4. CONCLUSION

A new CMOS realization of the CFDDA based on the cascading connection of a DTA and a voltage buffer has been proposed. The proposed CFDDA collect between the advantages of the DDA and the advantages of the CFOA over the classical op-amp. Application of the CFDDA in realizing a MOS-C oscillator have also been included.

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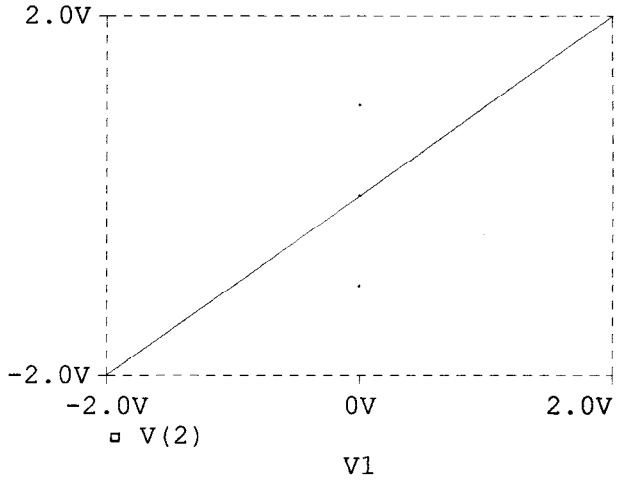


Fig.3(a) The output of the CFDDA voltage follower.

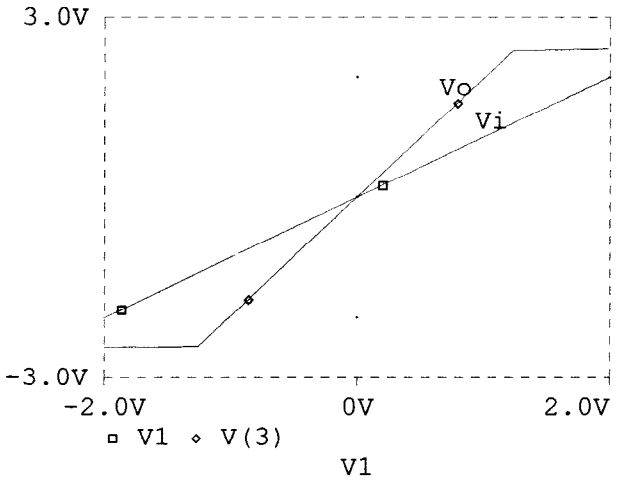
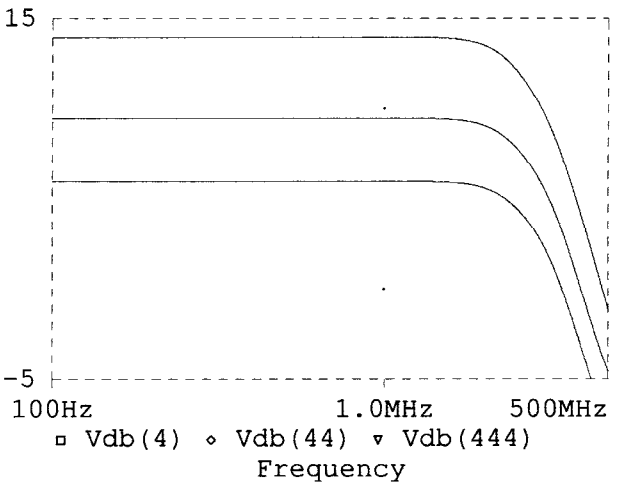


Fig.3(b) The output of the CFDDA voltage doubler.



Fi g.3(c) The frequency response of the CFDDA noninverting amplifier.