LOW VOLTAGE LOW POWER CMOS CURRENT MODE BUILDING BLOCKS FOR HEARING AID APPLICATIONS

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Abstract : Current mode CMOS building blocks for Hearing Aid application are proposed. The proposed circuits include, digital and analog automatic gain controls, digitally controlled G_m-C filters, and a pulse width modulation output stage. The circuits were fabricated in a 2 μ m n-well CMOS process through MOSIS.

1. Introduction

This paper presents new proposed building blocks suitable for hearing aid systems. The proposed cells are insensitive to the threshold voltage variation due to the body effect and hence can be implemented using semicustom ASIC techniques. These cells operate from supply voltages ± 1.5 volt.

The paper is organized as follows. Section two describes a new implementation of the AGC part. Section three describes the realization of digitally programmable second order continuous time filters using the G_m-C technique. A pulse width modulated output stage is described in section four. Experimental results of proposed cells, obtained from test chip fabricated through MOSIS using n-well 2 μ m SCNA technology, are shown in section five.

2. Automatic Gain Control Circuits

For the hearing aid application, it is required that the attack and release times of the AGC be in the order of 5ms and 20ms respectively. This requires an integrator with a large time constant in the feedback path. If a capacitor is used to implement this integrator, then a large capacitor (1-10 μF) is required. This large capacitor cannot be integrated in the same chip.

To solve this problem, a new digitally programmable AGC circuit (DAGC) is proposed. Fig. 1 shows the block diagram of the DAGC circuit. In this figure, the gain of the controlled amplifier is determined by the digital inputs (a_0 through a_3) which are the output of the counter. This counter acts as an integrator. It counts up or down according to the output of the comparator, which compares the output of the controlled amplifier I_o and the knee level I_K. Also, the output of the comparator determines the clock of the counter
which affect the attack and release times of the AGC. Since the input current is bi-directional, it should be compared with I_K and $(-I_K)$. An easier solution is to use an absolute circuit at the input of the AGC and to use a current direction restoring circuit at the output. In this way, the input and the output of the controlled amplifier are unidirectional, this simplifies the design of the controlled amplifier and the comparator.

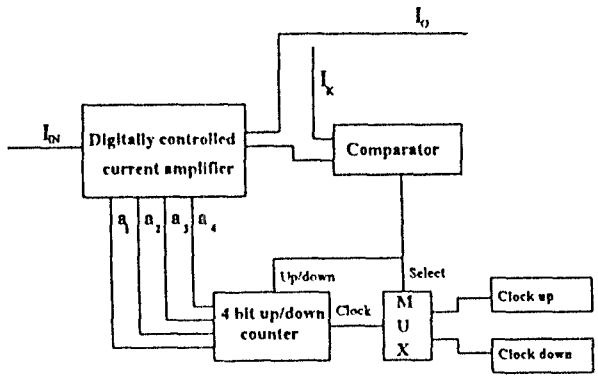

Fig. 1 The digitally controlled AGC (DAGC).

The PSpice simulation result of the DAGC is shown in Fig. 2 when I_{IN} =1 μ A and I_K=5 μ A.

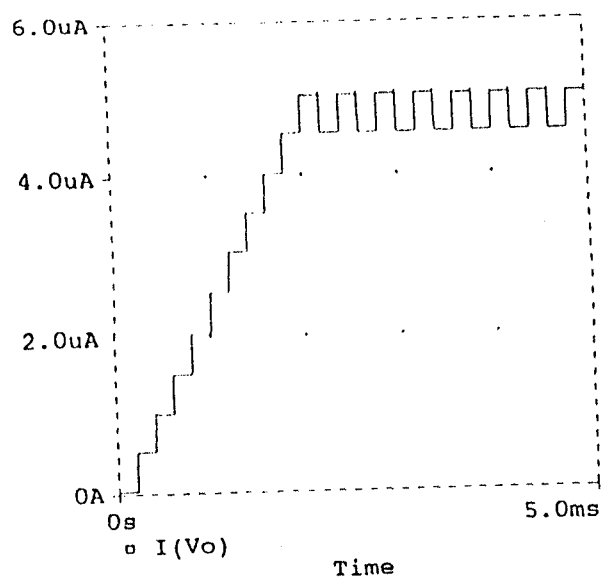

Fig. 2 Output current of the DAGC.

3. The Filter Section

Because of the frequency dependent loss, that is different from one patient to another, It is required to use filters with programmable gain, bandwidth, and

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center frequency. This programmability is obtained using three digital programming bits for each. The basic single input transconductor cell is shown in Fig. 3.

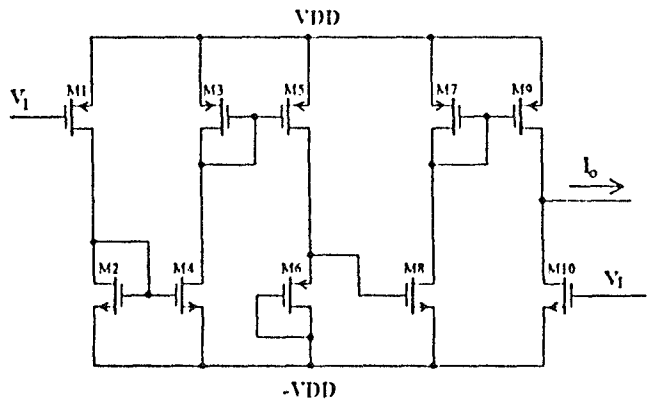

Fig. 3 Single input transconductor circuit.

$$I_o = 2\ K_8\ (V_{DD} - V_{Tn})\ V_I \qquad (1)$$

$$g_m = 2\ K_8\ (V_{DD} - V_{Tn}) \qquad (2)$$

where $K_8 = K_{10}$, and $K_1 = K_6$.

From the last equation it is found that the value of g_m can be controlled by controlling K_8 and K_{10}. This can be achieved by replacing each of the transistors M_8 and M_{10} by the circuit shown in Fig. 4. This circuit is equivalent to a transistor with 3-bit digitally controlled parameter K. The aspect ratios of the transistors M_3, M_6, and M_9 are chosen binary weighted.

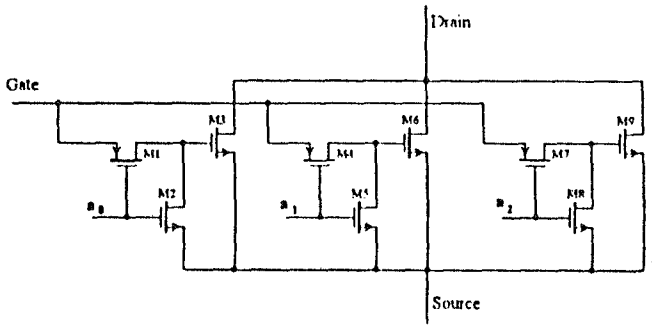

Fig. 4 An equivalent transistor with digitally controlled transistor parameter.

$$\frac{W_{eq}}{L_{eq}} = \frac{W_3}{L_3}\ (a_0 + 2\ a_1 + 4\ a_2) \qquad (3)$$

The PSpice simulation of the digitally controlled G_m is shown in Fig. 5 for different values of the input control bits.

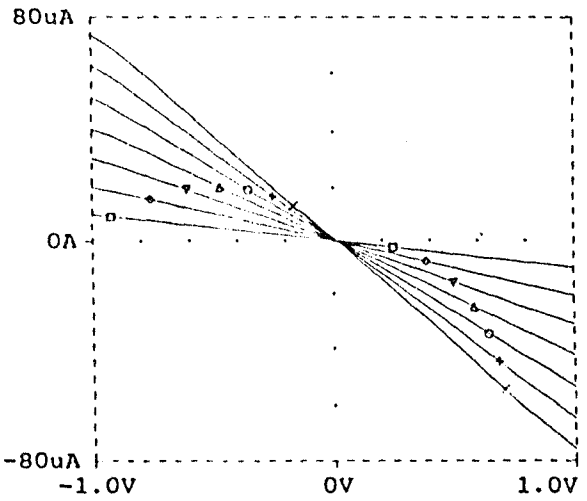

Fig. 5 Output current of the G_m for different values of input control.

The block diagram of a universal second order current mode continuous time filter shown in Fig. 6. This filter can be used to form lowpass, bandpass, and highpass filter by taking the output from different points. By controlling the gains a_0, a_1, a_2, a_L (for the lowpass filter), a_B (for the bandpass filter), and a_H (for the highpass filter). These programmable gains are obtained by using the digitally programmable G_m described above. For the bandpass filter

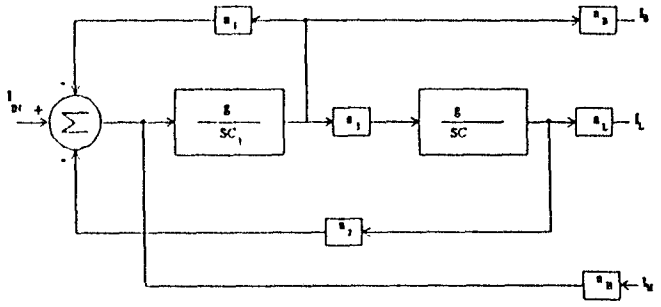

Fig. 6 A universal second order continuous time filter.

$$I_B = a_B \frac{\frac{a_3}{C_1} g\ S}{S^2 + S\frac{a_1}{C_1} g + \frac{a_2 a_3}{C_1 C_2} g^2} I_{IN} \qquad (4)$$

Taking $a_2 = a_3 = a$, then

$$\omega_O = \frac{a}{\sqrt{C_1 C_2}} g \qquad (5)$$

$$-Q = \sqrt{\frac{C_1}{C_2}\frac{a}{a_1}} \qquad (6)$$

$$\text{Center frequency gain} = a_B \frac{a}{a_1} \qquad (7)$$

Fig. 7 shows the PSpice simulations of the bandpass filter with different center frequencies which correspond to different input control bits.

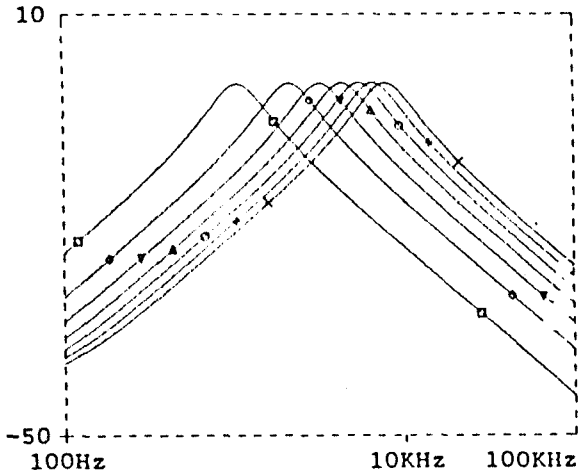

Fig. 7 Frequency response of the bandpass filter with different center frequencies.

4. The Output Stage

The basic idea of a class D amplifier is to convert the variations in the signal amplitude into variations in the pulse width. The can be achieved by comparing the analog signal with a high frequency triangular waveform. The output of the comparator is a pulse width modulated signal whose average is proportional to the input signal amplitude.

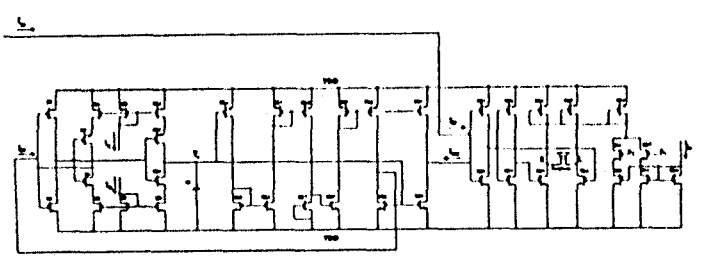

Fig. 8 The complete circuit of the output stage.

The whole circuit of the class D amplifier is shown in Fig. 8. I_{TRI} is the output of the proposed current mode triangular wave generator. I_{IN} is the analog input current. The amplitude of the PWM output current (passing through the earphone) is digitally programmed by the digital bits a_0 and a_1.

The PSpice simulation of the class D output stage for sinusoidal input is shown in Fig. 9.

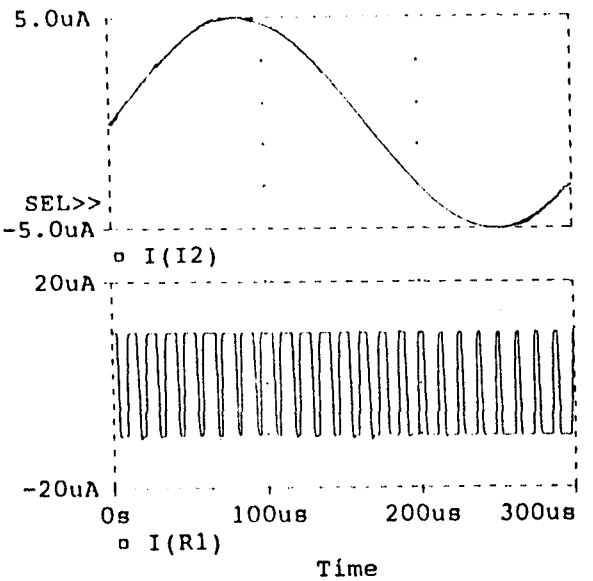

Fig. 9 Output current of the output stage for sinusoidal input.

Conclusion

New building blocks for H. A. applications have been proposed. These building blocks were fabricated through MOSIS. The experimental results were shown to be in agreement with the simulation results. The photodie of the fabricated chip is shown in Fig. 10.

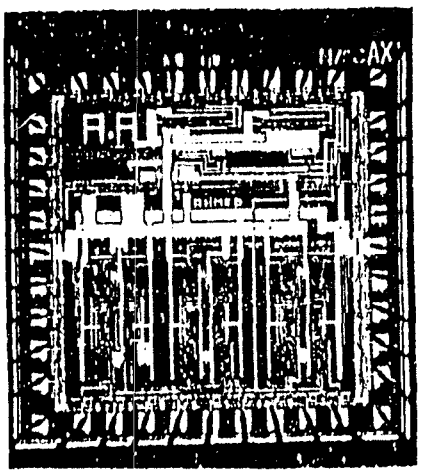

Fig. 10 The photodie of the fabricated chip.

References

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