A CMOS Programmable Silicon Retina implementing vision algorithms

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Abstract—**A Programmable Silicon Retina is presented targeting the use of efficient analog computation for early vision. The decoding and programmability methods employed lead to a dynamic and wide range of vision operations including edge enhancement, edge detection and averaging. A prototype chip implementing a 15 × 15 matrix of photoreceptors was fabricated in a double poly double metal N-well 2μm process.**

I. Introduction

Smart vision systems are becoming more important day after day. They differ from conventional vision systems in the integration of both the imager and the analog processing units on the same focal plane. A novel design for a vision chip is presented. We discuss the different building blocks required to form the vision chip which performs preprocessing-processing vision algorithms on 2D images. Processing depends on the local interaction between the pixel and its eight neighboring points. Contrary to the belief that analog hardware is usually hardwired, the flexibility in specifying the degree of interaction between these points is what defines the function performed on the image. Thus this approach achieves the programmability of digital processing and the power saving and speed of analog processing.

II. Novel Programmable Silicon Retina

The Silicon Retina presented integrates a 2D photoreceptor array with a nine input analog processor on the same focal plane. The analog processor is fully programmable, performing multiply-accumulate operations. A novel decoding scheme was used to decode the required matrix to be presented to the analog processor. Thus only one processor unit is needed, and the analog processor inputs depend on the time state. A block diagram of the chip is shown in Fig. 1 . Initially the multiplier is programmed by generating control voltages corresponding to the convolution filter coefficients. The filter is a 3×3 matrix. It is superimposed upon the input image, starting at the origin, and each input pixel is multiplied by the corresponding window value. Thus at each step of the horizontal counter an output is produced and the sliding window is then moved by one pixel to the right and the operation is repeated. Each fifteen horizontal steps, the window moves one step down and returns to the left most of the chip and the operation is repeated. After fifteen vertical steps the window returns to the origin and a new frame is scanned. Moving the window by one step only in both the horizontal and vertical direction enables the overlapping of the matrix producing better quality.

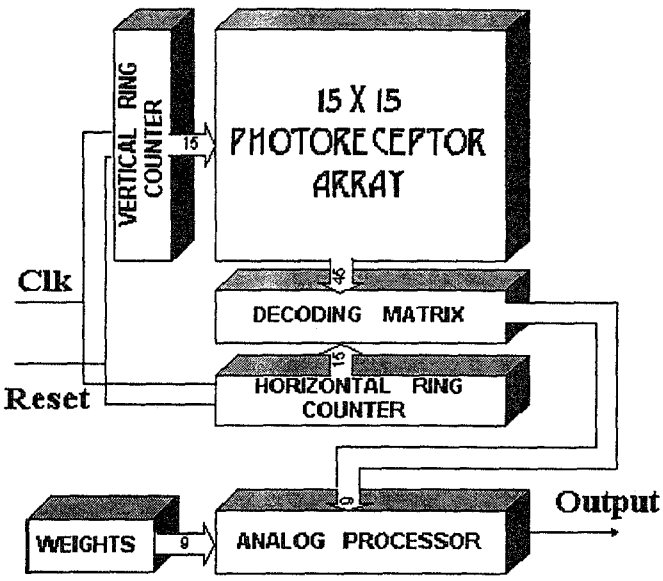

Fig. 1. Block diagram of the Silicon Retina

A. Photo-receptor circuit

The photo-detector detects the light intensity and transduces it into an electrical signal. Due to the wide range of incoming light intensity which changes over seven decades from moon light to bright sun light a compression technique must be used. In PMOS transistors when $V_{sg} < \mid V_{TP} \mid$, the transistor is said to operate in the subthreshold region following the equation

$$I_{sd} = I_o \exp(\frac{V_g}{V_t})(\exp(\frac{-V_s}{V_t}) - \exp(\frac{-V_d}{V_t})) \qquad (1)$$

The input photo-current is very small biasing transistors M_1 and M_2 shown in Fig. 2 in the subthreshold region. Thus producing a voltage V_{ph} proportional to the logarithm of the current, and consequently to the logarithm of the incoming light intensity. This circuit suffers

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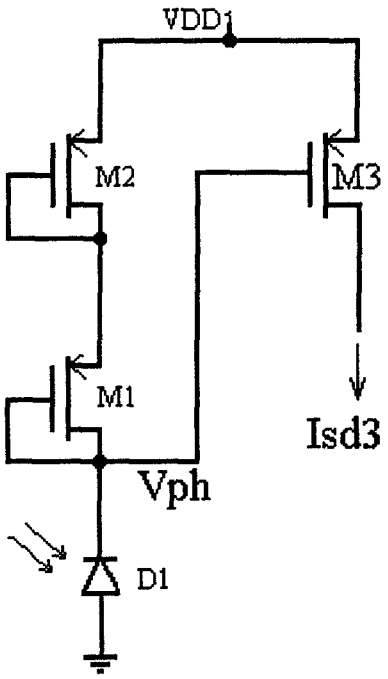

Fig. 2. Photo-receptor circuit

from reduced sensitivity. Thus a third transistor M_3 is introduced to the circuit to convert the output voltage — connected to its gate— to current for driving the rest of the circuit. Since M_3 is operating in the saturation region, then I_{sd_3} is given by

$$I_{sd_3} = \frac{K_3}{2}(2V_t \ln(1 + \frac{I_{ph}}{I_o}) - V_{TP})^2 \qquad (2)$$

The main idea behind converting the output voltage of the photo-receptor to current is to improve the sensitivity of the receptor as the output current changes over a wider range. Current mode processing is more noise immune than voltage. Also in this way the output current increases when light intensity increases and vice versa which is more natural than the output voltage which decreases with the increase of light intensity as shown in Fig. 3. Experimental results show that the current ranges from $3.6\mu A$ in moonlight to $26\mu A$ in bright sunlight following a logarithmic compression.

B. Decoding philosophy

The proposed silicon retina is composed of an array of 15 × 15 sensor. To access these sensors according to the prescribed sequence, there is a need of a decoding algorithm. The decoding algorithm consists of two stages. The first stage is a bus of three data lines for each column of sensors. The reason for the choice of the three data lines is that we are using a masking matrix of 3 × 3 elements, therefor only three sensors in any column at any instant will be the effective ones and the rest of the sensors in the column will be inactive. The sensors will be connected or disconnected from the data lines via pass transistors. The pass transistors are controlled by a vertical ring counter

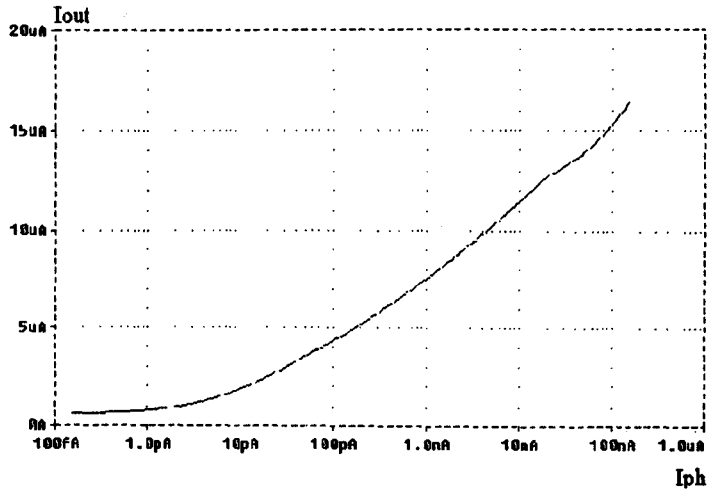

Fig. 3. PSPICE Simulation of Photo-receptor current

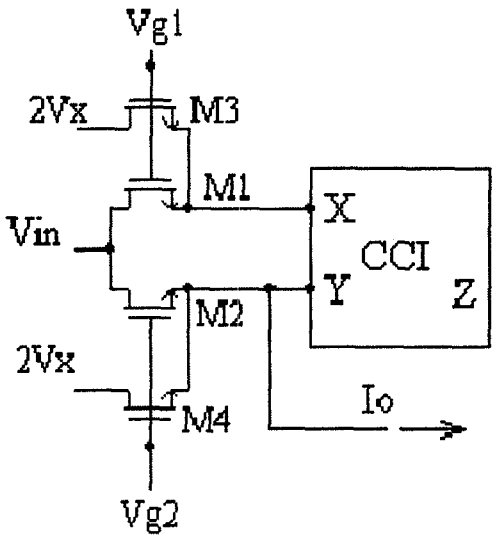

Fig. 4. Multiplier unit

of 15 states each of duration equal to 15 times the system's clock. Since we are using a matrix 3 × 3, then a nine input analog processor must be used. Since we have a total of 45 vertical data lines then a second stage of decoding must be used.

The second stage consists of nine multiplexers whose outputs are connected to the nine inputs of the processor unit. The multiplexer is formed of an array of 15 pass transistors acting as switches. The pass transistors are controlled by a horizontal ring counter of 15 states each of duration equal to the system's clock.

C. Analog processor unit

The analog processor circuit introduced depends on using four transistors operating in the triode region followed by a class one Current Conveyor (CC1) [1] as shown in Fig. 4.

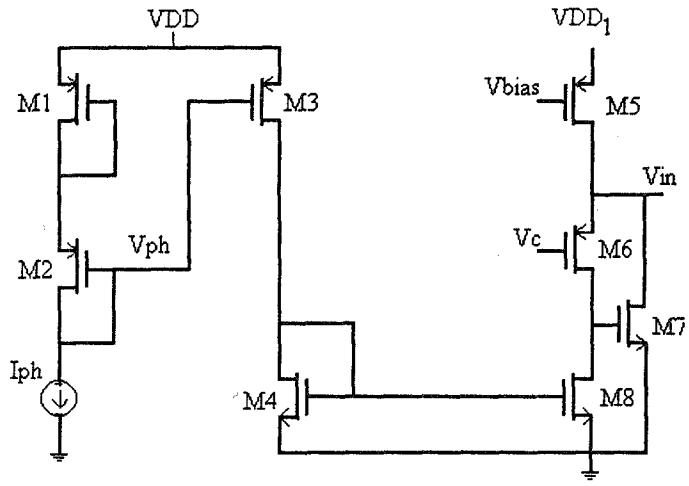

Fig. 5. I_{ph} to V_{in} conversion circuit.

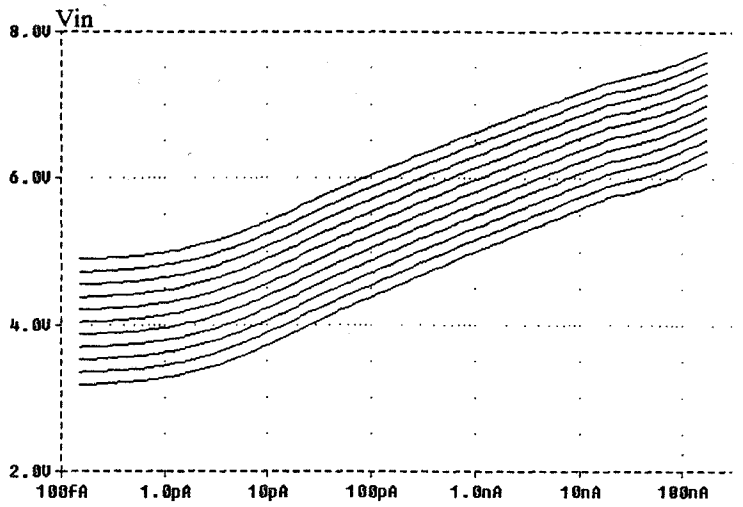

Fig. 6. PSPICE simulation for I_{ph} to V_{in} conversion.

Since all of them have equal sources by the action of the CC1, then

$$\begin{aligned} I_o &= I_{ds_2} + I_{ds_4} - I_{ds_1} - I_{ds_3} \\ &= k(V_{g_2} - V_{g_1})V_{in} \end{aligned} \tag{3}$$

The analog processor circuit would be formed of one current conveyor and nine sets of the transistors applied above. V_{g_1} is adjusted to a constant value and through controlling V_{g_2}, both positive and negative weights with negligible error can be achieved.

The analog processor discussed depends on voltage mode. Thus the current produced by the photo-receptor must be converted into voltage as shown in Fig. 5. Transistor M_5 operates in the saturation region, thus acting as a current source. Transistor M_6 is adjusted to operate in the saturation region, through the control voltage V_c. Transistor M_7 sinks the difference between M_4 and M_8. Then V_{in} is related to V_{ph} by

$$V_{in} = V_c + (\alpha - 1)V_{Tp} - \alpha V_{ph} + \alpha V_{dd1} \tag{4}$$

where

$$\alpha = \sqrt{\frac{K_3 K_1}{K_2 K_4}} \tag{5}$$

and K is the aspect ratio of the transistor.

Thus V_c has a level shifting effect as shown in Fig. 6.

Acknowledgment

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