A Universal Fractional-Order Memelement Emulation Circuit

Nariman A. Khalil[1], Mohammed E. Fouda[2], Lobna A. Said[3], Ahmed G. Radwan[2,4], and Ahmed M. Soliman[5]
[1]Faculty of Engineering, Nahda University (NUB), Egypt
[2]Engineering Mathematics and Physics Dept, Faculty of Engineering, Cairo University, Giza, 12613, Egypt
[3]Nanoelectronics Integrated Systems Center (NISC), Nile University, Giza, Egypt
[4] School of Engineering and Applied Sciences, Nile University, 12588, Giza, Egypt
[5]Electronics and Comm. Eng. Dept.,Cairo University, Egypt

***Abstract*—This paper proposes a current-/voltage-controlled universal emulator that can realize any fractional-order mem-elements (FOME). The proposed emulator consists of second-generation current conveyors (CCII) block, two switches, and a multiplier/divider block. The first switch controls the emulator mode (voltage or current), while, the other controls the type of the emulated FOME. The influence of the fractional-order capacitor (FOC) on the pinched hysteresis loop (PHL) area, is discussed which increases the controllability on the double loop area and the working frequency range. Numerical and PSPICE simulations are presented for selected cases to prove the theoretical findings.**

***Keywords*—Memristor, CCII, emulator, Fractional-order circuits, FOC, Meminductor, Memcapacitor, pinched hysteresis.**

I. Introduction

The concept of the memory element (memelement) is discovered firstly by Chua for the memristor (M) in 1971 [1]. Memristors are characterized by a constitutive non-linear relation between the flux (φ) and the charge (q). The memristor was a theory until HP announced a nano-scale device that approximates the performance of the M [2]. Lately, the theory of memristive elements was generalized to include the memcapacitors (MCs) and the meminductors (MIs) [3]. The memelements are employed in many applications like neuromorphic hardware [6], oscillators [5], and logic circuits [4].

Due to the absence of the memelements as a two-terminal element, several emulators have been proposed to realize their dynamic performance employing the commercial active and passive elements [7]. A lot of research papers used the mutator concept, which transforms from one mem-element into another [8], [9]. A generalized mutator converting between memcapacitor, memristor, and meminductor was proposed using only three active elements providing the designers more elasticity in exploring dynamical properties of memory elements in [10]. Using CCII, the emulator circuit in [11] was introduced to convert the memristive device into floating meminductor and memcapacitor elements. Another technique is to realize a special emulator as in [12]. Additionally, many researchers try to associate the fractional calculus (FC) method with memristive systems in several applications [13].

FC studies the real-order integrals and derivatives operators [14], [15]. It can supply further compact and practical characterization of the real-time physical systems [14]. To gain the advantages of the fractional-order system, the FOME emulators were proposed in [9] presenting the influence of varying the order on the PHL area.

The paper aims to suggest a universal emulator based on the mathematical model of the FOMEs. The emulator is built based on generalized impedances, which increase the flexibility to implement different FOME elements. A special case of this emulator was introduced in [16] which implement the integer-order meminductor. Moreover, the employment of the FOC adds controllability on the pinched double loop area and the range of frequency of the memfractor by changing the order α.

The organization of this paper is as follows: section II discusses the numerical simulations of the current- and voltage-controlled mem-elements and the effect of the α of the FOC on hysteresis loop area. Section III presents the proposed universal emulator and its implementation to realize the four memelements. The PSPICE simulations are introduced in section IV. Finally, the conclusion work is in section V.

II. The Generalized FOMEs Model

The general mathematical model of the X-controlled fractional-order memelements can be defined as follows:

$$Y(t) = D_t^{\beta}(J_t^{\beta})\left(\left(a + kD_t^{\alpha}(J_t^{\alpha})X(t)\right)D_t^{\gamma}(J_t^{\gamma})X(t)\right), \quad (1)$$

where D_t^{α}, J_t^{α}, D_t^{β}, J_t^{β}, D_t^{γ}, J_t^{γ} are fractional operators, the D_t / J_t means fractional-order derivative/integral operation, α, β, and γ are arbitrary real numbers $\in [-1, 1]$. $X(t)$ and $Y(t)$ are the normalized input and output signal, respectively, a is the initial value, and k is scaling constants. The generalization of the mathematical model increases the flexibility to implement any fractional order (FO) memristive elements, as summarized in Table I.

The voltage-current relation for the current-controlled FO memristor and inverse memristor are expressed in Table I where a represents the initial memristance/ inverse memristance, and k is constant. The memristance/inverse memristance is linearly proportional to the accumulated/differentiated current, respectively. The PHL area can be controlled not only by the working frequency but also the fractional-order α of the employed fractional-order capacitor (FOC). Figure 1(a)

978-1-7281-3173-3/19/$31.00 ©2019 IEEE

TABLE I. ALL POSSIBLE REALIZATION OF FOME

γ	β	α	$x(t)$	$y(t)$	FOME	X(t)-Y(t) relation
0	0	0	i(t)	v(t)	non-linear resistor	v(t)=(a+ki(t))i(t)
	-1	-1	i(t)	v(t)	non-linear capacitor	v(t)=J_t^{β}((a+kq(t))i(t))
			v(t)	i(t)	non-linear inductor	i(t)=J_t^{β}((a+kφ(t))v(t))
	0	$-1 \le \alpha \le 0$	i(t)	v(t)	FO current-controlled memristor	v(t)=(a+k J_t^{α} i(t))i(t)
			v(t)	i(t)	FO voltage-controlled memristor	i(t)=(a+k J_t^{α} v(t))v(t)
		$0 \le \alpha \le 1$	v(t)	i(t)	FO voltage-controlled inverse memristor	i(t)=(a+k D_t^{α} v(t))v(t)
			i(t)	v(t)	FO current-controlled inverse memristor	v(t)=(a+k D_t^{α} i(t))i(t)
	$0 \le \beta \le 1$	-1	i(t)	v(t)	FO current-controlled meminductor	v(t)= D_t^{β}((a+k q(t))i(t))
			v(t)	i(t)	FO voltage-controlled memcapacitor	i(t)= D_t^{β}((a+k φ(t))v(t))
$0 \le \gamma \le 1$	0		q(t)	v(t)	FO charge-controlled inverse memcapacitor	v(t)=(a+k σ(t))D_t^{γ} q(t)
			φ(t)	i(t)	FO flux-controlled inverse meminductor	i(t)=(a+k ρ(t))D_t^{γ} φ(t)
$-1 \le \gamma \le 0$			v(t)	i(t)	FO voltage-controlled inverse meminductor	v(t)=(a+k φ(t))J_t^{γ} v(t)
			i(t)	v(t)	FO current-controlled inverse memcapacitor	v(t)=(a+k q(t))J_t^{γ} i(t)

presents the I-V plane of the inverse memristor for $a = 20k\Omega$, $k = 10kA^{-1}s^{-\alpha}$ at $\alpha = 0.8$, where the hysteresis loop area increase as the frequency increases. For the memristor in Fig. 1(b), the PHL area is declined as the frequency increase. Additionally, the PHL of the inverse memristor and the memristor are depicted in Fig. 1(c) and (d) at different α where the operating frequency $\omega = 1rad/sec$, and $a = 20k\Omega$, $k = 10kA^{-1}s^{-\alpha}$. Clearly, the PHL is symmetric when $\alpha = 1$ and asymmetric at $\alpha < 1$.

From Table I, the FO current-controlled meminductor is achieved where the voltage versus current is defined as follows:

$$J_t^{\beta} v(t) = \big(a + k \int_0^t i(t)\big) i(t), \tag{2}$$

where β can take any arbitrary positive real number, the accumulated voltage represents the flux, and a, k are constants. The FO meminductor has interpolated behavior between MI and M. The classical MI and M are gained at $\beta = 1$ and $\beta = 0$, respectively. The influence of various values β on the PHL of the flux versus current ($\varphi - i$) curve is depicted in Fig. 2 where the pinched point location is moved from $(0, 0)$ as β decreases until disappear. Using the same method, the FO voltage-controlled MC can be illustrated as follows:

$$J_t^{\beta} i(t) = \big(a + k \int_0^t v(t)\big) v(t), \tag{3}$$

where the accumulated current represents the charge. The fractional-order voltage-controlled memcapacitor has intermediate characteristics behaviour between MC and M. The influence of different values of β on the PHL of the $q - v$ curve is depicted in Fig. 3 where the pinched point location moves away from zero-crossing into the negative side until it disappears as the value of β decreased. The different realization of current- and voltage-controlled FOME are presented next.

III. A GENERALIZED FOMES EMULATOR

The implementation of the generalized current-/voltage-controlled emulator is presented in Fig. 4 using CCII± block proposed in [17], multiplier, divider, and two switches S_1 and S_2. By switching between them, the current-\voltage-controlled memristive elements are realized. The first switch S_1 has the responsibility for switching between two modes (the current- and the voltage-controlled emulator). Based on the emulated element, the second switch defines the state where the state zero emulates the memristor/inverse memristor, and the state one emulates the FO meminductor and memcapacitor.

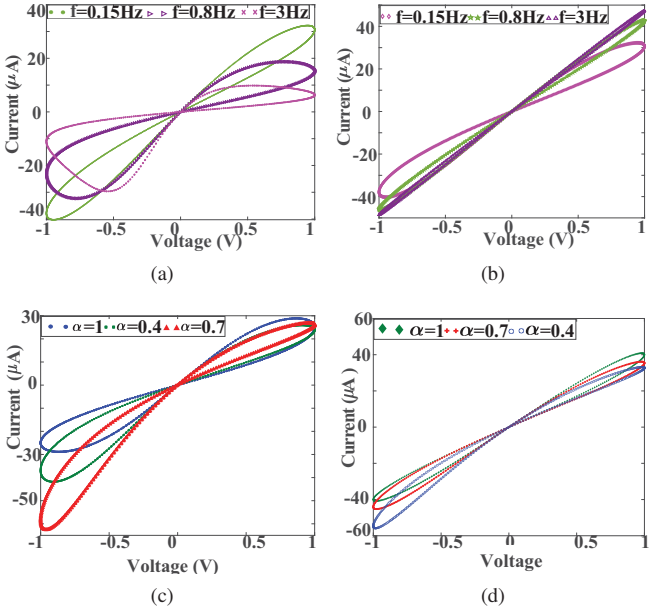


Fig. 1. Numerical simulations for $a = 20k\Omega$, $k = 10kA^{-1}s^{-\alpha}$ at $\alpha = 0.8$ of (a) inverse memristor, (b) memristor, and at different orders for (c) inverse memristor, (d) memristor

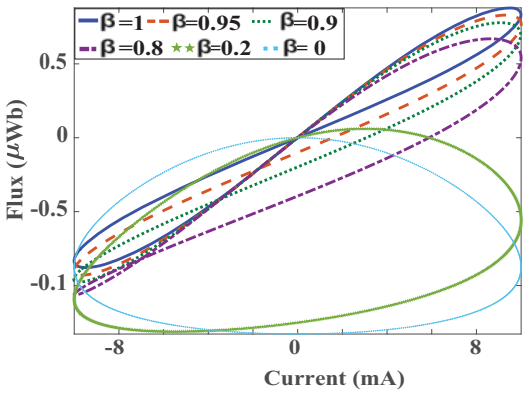


Fig. 2. The FO current-controlled MI for different β at $a = 80\mu$H and $k = 5\mu HC^{-1}s^{-\alpha}$

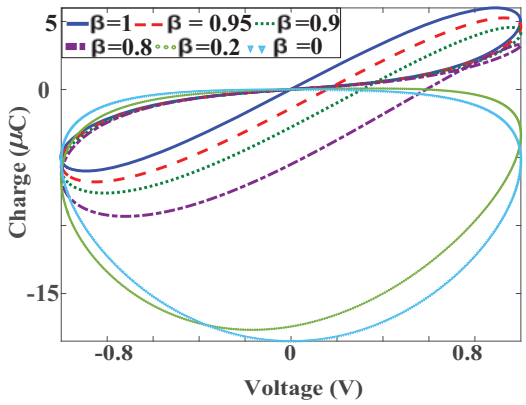


Fig. 3. the FOMC for different β when $a = 100\mu$F and $k = 400\mu FWb^{-1}s^{-\alpha}$

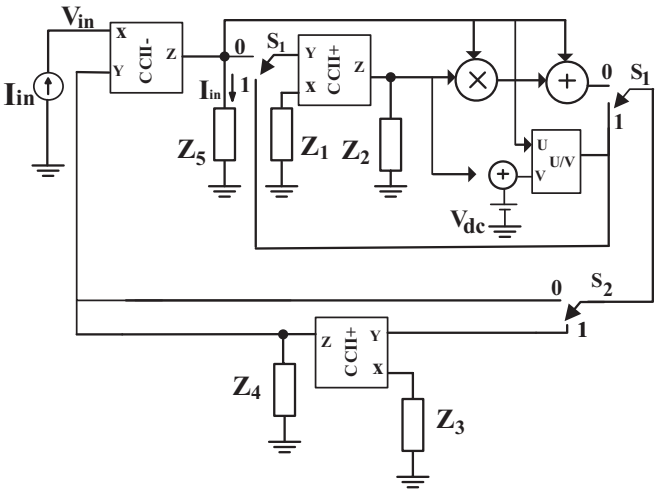


Fig. 4. The proposed current-and voltage-controlled emulator

When the two switches at state zero, the input voltage and current relation employing the three general impedances are defined as follows:

$$V_{in} = \left(Z_5 + d\left(\frac{Z_5^2 Z_2}{Z_1}\right) i_{in}\right) i_{in}, \tag{4}$$

where d represents the voltage multiplier gain. All possible impedances combinations are presented in Table II where the current-controlled memristor and inverse memristor are realized. At $S_2 = 1$, the input voltage and the current relation is defined as follows:

$$V_{in} = \left(\frac{Z_4}{Z_3}\left(Z_5 + \left(d\frac{Z_5^2 Z_2}{Z_1}\right) i_{in}\right)\right) i_{in}. \tag{5}$$

When $S_1 = 1$, the circuit in Fig. 4 simulates the behaviour of the voltage-controlled FOME . The voltage-current relation at $S_2 = 0$ and $S_2 = 1$, respectively, are given by:

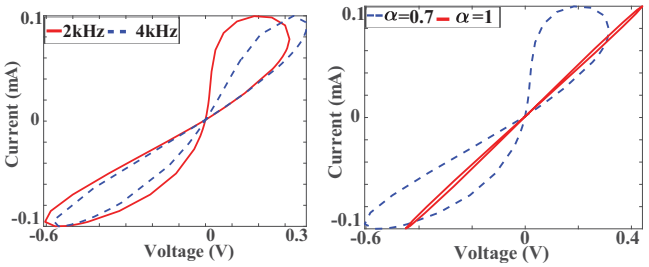


Fig. 5. PSPICE simulation for the current-controlled memristor at (a) $\alpha = 0.7$, and (b) different orders at $2kHz$

$$i(t) = \frac{V_{dc} + \frac{Z_2}{Z_1} v(t)}{dZ_5} v(t), \tag{6a}$$

$$i(t) = \frac{Z_3}{Z_4} \frac{V_{dc} + \frac{Z_2}{Z_1}\frac{Z_3}{Z_4} v(t)}{dZ_5} v(t), \tag{6b}$$

where d is the divider gain. From(6), the voltage-controlled FOMEs are realized as summarized in Table II. Note that a capacitor at X-terminal of CCII will affect the circuit due to R_X of the CCII.

IV. Simulations Results

Due to missing the solid-state fractional-order capacitor samples, Valsa approximation is employed to synthesize the behaviour of FOC [18]. The current/voltage-controlled universal emulator is implemented employing AD844 as CCII, AD633 as an analog multiplier, and AD734 as a divider with and sinusoidal current input. The memristor is assembled at order $\alpha = 0.7$ and 1 with parameters $R = 5k\Omega$, $R_1 = 10k\Omega$, and $C_1 = 10nF$. The pinched hysteresis of the I-V curve is presented in Fig. 5 (a) at $\alpha = 0.7$ with different frequencies where the loop area is asymmetric and decreased with increasing frequencies. Also, increasing α; the double loop is shrunk and becomes symmetric at $\alpha = 1$ as depicted in Fig. 5(b). The order of the capacitor has an effect on the range of frequency which increases with decreasing the order. Additionally, the voltage-controlled memristor is emulated with parameters $R = 5k\Omega$, $R_1 = 5k\Omega$, and $C_1 = 10nF$ at $\alpha = 1$ where the pinched hysteresis of the I-V curve is shrunk with increasing frequency as shown in Fig. 6. The inverse memristor of the current-controlled emulator mode is simulated with parameters $R = R_1 = 100\Omega$ and $C_1 = 10nF$ at $\alpha = 1$. The pinched hysteresis of the I-V curve is increased with increasing frequency as shown in Fig. 7. Finally, the I-V characteristic of the current-controlled meminductor is presented in Fig. 8(a) for $\alpha = 0.8$ which is decreased with increasing the frequency. The $\varphi - I$ hysteresis shrunk with increasing the frequency as depicted in Fig. 8(b) at $\alpha = 1$.

V. Conclusion

Based on the mathematical model of FOME, the universal current and voltage controlled emulator was introduced. The generalized impedances were used to increase the flexibility to assemble the four memristive elements. The numerical simulations were introduced and investigated with different

TABLE II. ALL POSSIBLE REALIZATION USING PROPOSED EMULATOR

S_1	S_2	Z_1	Z_2	Z_3	Z_4	Z_5	Memelements	a	k
0	0	R_1	$1/s^{\alpha}C_1$	-	-	R	FO current-controlled memristor	R	R^2/R_1C_1
		$1/s^{\alpha}C_1$	R_1	-	-	R	FO current-controlled inverse memristor	R	$R^2R_1C_1$
0	1	R_1	$1/sC_1$	$1/s^{\beta}C_2$	R_2	R	FO current-controlled meminductor	RR_2C_2	$dR_2C_2R^2/R_1C_1$
1	0	R_1	$1/s^{\alpha}C_1$	-	-	R	FO voltage-controlled memristor	V_{dc}/dR	$1/dRR_1C_1$
		$1/s^{\alpha}C_1$	R_1	-	-	R	FO voltage-controlled inverse memristor	V_{dc}/dR	R_1C_1/dR
		$1/sC_2$	R_1	-	-	$1/s^{\alpha}C_1$	FO voltage-controlled memcapacitor	$V_{dc}C_2/d$	C_2/dR_1C_1
1	1	R_1	$1/sC_1$	$1/s^{\beta}C_2$	R_2	R	FO flux-controlled meminductor	V_{dc}/dRR_2C_2	$1/dR_1C_1R_2C_2R$

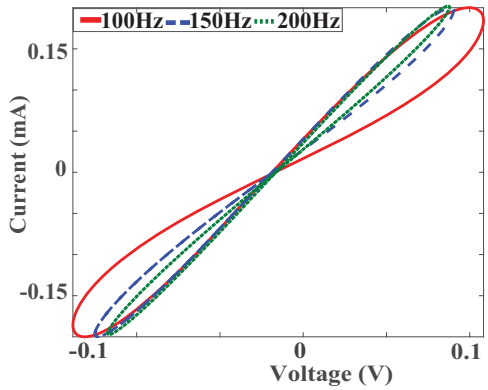


Fig. 6. PSPICE simulations results of the hysteresis for the current versus voltage for the voltage-controlled memristor at $\alpha = 1$

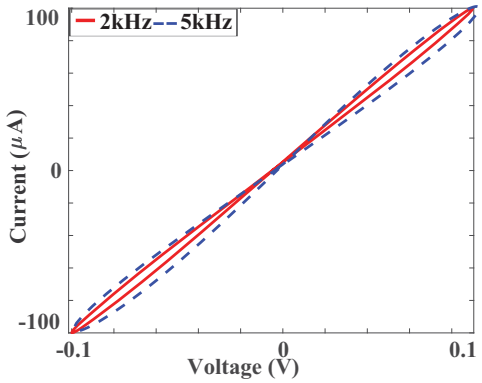
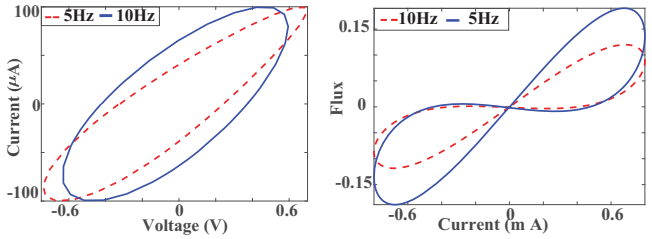


Fig. 7. PSPICE simulations results of the I-V curve for the current-controlled inverse memristor at $\alpha = 1$



(a) (b)

Fig. 8. PSPICE simulations results of the current-controlled meminductor (a) the I-V characteristic at $\alpha = 0.8$, (b) $\varphi - i$ at $\alpha = 1$

order α versus frequency with respect to the proposed models. To prove the introduced emulators, PSPICE simulation results were performed.

REFERENCES

[1] L. Chua, "Memristor-the missing circuit element," *IEEE Transactions on circuit theory*, vol. 18, no. 5, pp. 507–519, 1971.

[2] D. B. Strukov, G. S. Snider, D. R. Stewart, and R. S. Williams, "The missing memristor found," *nature*, vol. 453, no. 7191, p. 80, 2008.

[3] M. Di Ventra, Y. V. Pershin, and L. O. Chua, "Circuit elements with memory: memristors, memcapacitors, and meminductors," *Proceedings of the IEEE*, vol. 97, no. 10, pp. 1717–1724, 2009.

[4] N. Soliman, M. E. Fouda, A. G. Alhurbi, L. A. Said, A. H. Madian, and A. G. Radwan, "Ternary functions design using memristive threshold logic," *IEEE Access*, vol. 7, pp. 48 371–48 381, 2019.

[5] H. G. Hezayyin, G. M. Ahmed, M. E. Fouda, L. A. Said, A. H. Madian, and A. G. Radwan, "A generalized family of memristor-based voltage controlled relaxation oscillator," *International Journal of Circuit Theory and Applications*, 2018.

[6] M. Fouda, F. Kurdahi, A. Eltawil, and E. Neftci, "Spiking neural networks for inference and learning: A memristor-based design perspective," *arXiv preprint arXiv:1909.01771*, 2019.

[7] G. Wang, S. Jiang, X. Wang, Y. Shen, and F. Yuan, "A novel memcapacitor model and its application for generating chaos," *Mathematical Problems in Engineering*, vol. 2016, 2016.

[8] D. Biolek and V. Biolkova, "Mutator for transforming memristor into memcapacitor," *Electronics letters*, vol. 46, no. 21, pp. 1428–1429, 2010.

[9] N. A. Khalil, L. A. Said, A. G. Radwan, and A. M. Soliman, "General fractional order mem-elements mutators," *Microelectronics Journal*, 2019.

[10] D. Yu, Y. Liang, H. H. Iu, and L. O. Chua, "A universal mutator for transformations among memristor, memcapacitor, and meminductor," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 61, no. 10, pp. 758–762, 2014.

[11] Y. V. Pershin and M. Di Ventra, "Emulation of floating memcapacitors and meminductors using current conveyors," *Electronics Letters*, vol. 47, no. 4, pp. 243–244, 2011.

[12] D. Yu, Y. Liang, H. Chen, and H. H. Iu, "Design of a practical memcapacitor emulator without grounded restriction," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 60, no. 4, pp. 207–211, 2013.

[13] S. He, S. Banerjee, and B. Yan, "Chaos and symbol complexity in a conformable fractional-order memcapacitor system," *Complexity*, vol. 2018, 2018.

[14] I. Podlubny, *Fractional differential equations: an introduction to fractional derivatives, fractional differential equations, to methods of their solution and some of their applications*. Elsevier, 1998, vol. 198.

[15] M. F. Tolba, L. A. Said, A. H. Madian, and A. G. Radwan, "Fpga implementation of the fractional order integrator/differentiator: Two approaches and applications," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 66, no. 4, pp. 1484–1495, 2018.

[16] M. E. Fouda and A. G. Radwan, "Memristor-less current-and voltage-controlled meminductor emulators," in *Electronics, Circuits and Systems (ICECS), 2014 21st IEEE International Conference on*. IEEE, 2014, pp. 279–282.

[17] A. S. Sedra and K. Smith, "A second generation current conveyor and its applications," *IEEE Trans. Circuit Theory*, vol. 132, no. 1, 1970.

[18] J. Valsa, P. Dvorak, and M. Friedl, " Network model of the CPE," *Radioengineering*, vol. 20, no. 3, pp. 619–626, 2011.