A Universal Floating Fractional-Order Elements/Memelements Emulator

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***Abstract*—In this paper, a generalized floating emulator block is proposed using grounded elements. The proposed emulator is a universal emulator that is used to realize any floating elements such as fractional-order element (FOE) and fractional-order memelements (FOME). Different implementations for the introduced emulator are presented using different active blocks and generalized impedances. The fractional-order parameters add an extra degree of controllability on the hysteresis loop (HL) and the location of the pinched point, which will be investigated. Circuit simulations for the proposed circuits are performed.**

***Keywords*—Floating impedance, memristor emulator, fractional-order circuits, memfractor, meminductor, memcapacitor.**

I. Introduction

Recently, the fractional calculus (FC) is widely employed in modeling and analyzing the real system. FC is the generalization of differentiation and integration into the fractional-order domain. The system flexibility is increased through the fractional-order parameters [1]. Several applications employed the FC such as filters [2] and oscillators [3]. In the circuit theory, the passive elements are generalized to the fractional-order domain such as fractional-order inductor (FOI) and fractional-order capacitor (FOC). Due to the initiation of FOE and because of their absence in the market as a two-terminal device, different emulators were proposed to simulate their behavior using mutators in [4], [5]. Due to the use of FC in modeling the real systems [1], many research articles tried to associate the technique of FC with the memristive elements in several applications [6].

The Memristor, R_M, was discovered by Chua, which is characterized by a constitutive non-linear relationship between the charge q and the flux φ [7]. Then, the memristive system was generalized to the capacitor and inductor named memcapacitors (MC) meminductor (MI), respectively [8]. Memristive elements have gained a lot of attention in several applications such as relaxation oscillators [9] and chaotic systems [10]. Due to the advantages of FC, the electrical circuit elements were generalized to the fractional-order domain [11]. The FOME was defined as memfractor element in [11] where the mathematical model is defined as follows [11]:

$$D_t^{\alpha_1}\varphi(t) = F_M^{\alpha_1,\alpha_2} D_t^{\alpha_2} q(t), \tag{1}$$

where α_1, α_2 are arbitrary real numbers between 0 and 1, and $F_M^{\alpha_1,\alpha_2}$ is called a memfractor. The memfractor has intermediate characteristics between the four memelements where the integer values of α_1 and α_2 give different memelements. When (α_1,α_2) equal to (1,1), (0,1), (0,0), (1,0) the R_M, MI, second-order memristor (R_{2M}), and MC are realized, respectively. From Eqn.1, the non-integer values of α_1 and α_2 give an interpolated characteristic of memfractor between two different memelements as discussed in [11]. The fractional-order memcapacitor (FOMC) and fractional-order meminductor (FOMI) are defined by the relation between the fractional derivative of the charge with the voltage and the flux with current, respectively. Due to missing the commercial off-the-shelf element, different circuits have been proposed emulating their behavior [12].

Recently, many emulators were designed to simulate the behavior of memristive elements. A floating memcapacitor emulator was introduced based on four current conveyors and approved practically in [13]. In [14], a floating memristor emulator was proposed which can operate at a high operating frequency. The memristor-less memcapacitor emulator was proposed in [15]. In addition, the mutator can be used in the realization of the memelements where it converts from memristor load to MI or MC [16]. A universal mutator was proposed in [12], which transforms between the memristor, the memcapacitor, and the meminductor by using three active elements and validated experimentally. In [17], the FOMI and FOMC emulators were presented based on two-and three-port mutators. Also, the influence of the fractional-order α on the HL of $q-v$ and $\varphi-i$ curve were discussed.

The objective of that paper is to propose a universal emulator to realize any floating elements such as FOEs and FOMEs by using different impedances combinations. Also, five different implementations of the universal emulator are introduced employing various active blocks. The employment of FOC adds an extra degree of freedom on the HL area and the location of the pinched point for the FOMEs that presented at different orders. Besides the realization of FOMEs, the floating FOI order $0 < \alpha \leq 1$ and FOC order $1 < \alpha \leq 2$ elements are achieved using one and two FOCs, respectively. The simulations of different elements are implemented to verify the reliability of the proposed emulator.

This paper is organized as follows: Section II proposes a universal floating emulator with five different realizations. The PSPICE simulations for the floating elements based on the introduced realizations are introduced in Section III. Finally, the conclusion is presented in section IV.

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TABLE I. THE REALIZATION OF FLOATING IMPEDANCE USING PROPOSED EMULATOR

No.	Z_1	Z_2	Z_3	Z_{in}	Element
1.	R_M	R	$\frac{1}{s^\alpha C}$	$\frac{R_M}{s^\alpha CR}$	FOMC
2.	R	R_M	$\frac{1}{s^\alpha C}$	$\frac{R}{s^\alpha CR_M}$	
3.	R	$\frac{1}{s^\alpha C}$	R_M	$s^\alpha CRR_M$	FOMI
4.	R_1	R_2	R_M	$\frac{R_M R_1}{R_2}$	R_M
5.	R_M	R_2	R_1		
6.	$\frac{1}{s^\alpha C_1}$	R_1	$\frac{1}{s^\beta C_2}$	$\frac{1}{s^{\alpha+\beta}C_1C_2R_1}$	FOC
7.	R_1	$\frac{1}{s^\alpha C}$	R_2	$s^\alpha CR_1R_2$	FOI

II. THE PROPOSED UNIVERSAL EMULATOR

The universal emulator shown in Fig. 1(a) is designed based on a general block where its characteristic matrix is illustrated as follows:

$$\begin{bmatrix} I_1 \\ I_2 \\ V_3 \\ I_4 \\ V_5 \\ I_6 \\ I_7 \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ a_1 & -a_1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & b_1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & a_2 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & b_2 & 0 & 0 \\ 0 & 0 & 0 & 0 & -b_2 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ I_3 \\ V_4 \\ I_5 \\ V_6 \\ V_7 \end{bmatrix}, \quad (2)$$

where a_i ,b_i i=1,2 are the parameters of the non-linearity of block terminals and ideally they have only the value of ± 1 to define the voltage sign and the current direction, respectively. The driven input impedance of the proposed emulator presented in Fig.1(a) is given as follow:

$$V_3 = a_1V_1 - a_1V_2, \quad (3a)$$

$$I_4 = b_1I_3 = b_1\frac{a_1V_1 - a_1V_2}{Z_1}, \quad (3b)$$

$$V_5 = a_2V_4 = b_1a_2\frac{a_1V_1 - a_1V_2}{Z_1}, \quad (3c)$$

$$I_1 = I_6 = -I_7 = b_2I_5 = b_1a_2b_2\frac{Z_2(a_1V_1 - a_1V_2)}{Z_1Z_3}, \quad (3d)$$

$$Z_{in} = \frac{V_1 - V_2}{I_1} = \frac{1}{a_1b_1a_2b_2}\frac{Z_1Z_3}{Z_2}. \quad (3e)$$

From Eqn.3, any floating element can be realized depending on the selection of passive elements as summarized in Table I. Moreover, the floating MI, MC, and inductor can be implemented at $\alpha = 1$. The main advantage of the proposed block is that all employed impedances in the circuit are grounded, which improve the circuit linearity and performance. Different realizations for the proposed universal emulator are presented in Figs.1(b)-(f) using various active elements such as second-generation current conveyor family (CCII), differential voltage current conveyor (DVCC), transconductance amplifier family (TA), balanced output TA (BOTA), BOCCII, and the modified DDCCTA introduced in [18].

Firstly, realization I is depicted in Fig. 1(b) where the differential input voltage is applied on two current conveyor (CC) blocks with the same impedance at X-terminal (Z_1). To achieve the characteristic of the proposed emulator, BOCCII block is employed. The summation current of two CC blocks for the two Z-terminals is equal to $I_Z = (a_1b_1V_1 + a_2b_2V_2)\frac{1}{Z_1}$ where the necessary condition to achieve differential input is $a_1b_1 = -a_2b_2$. Due to the feedback of two Z-terminals of BOCCII, the input current is equal to: $I_5 = b_3I_2 = -b_3I_1 = a_3b_3(a_1b_1V_1 + a_2b_2V_2)\frac{Z_2}{Z_1Z_3}$. With achieving the previous condition, the input impedance $Z_{in} = Z_1Z_3/a_1b_1a_3b_3Z_2$ which is the same input impedance given in Eqn.3. The positive and negative floating impedance can be realized using different combinations of the four members of CCII family as summarized in [5].

TABLE II. THE POSSIBLE IMPLEMENTATION OF FLOATING ELEMENT USING THE PROPOSED REALIZATIONS

Case No.	1	2	3	4	5	6	7
realization I	✓	✓	✓	✓	✓	✓	✓
realization II	✓	✓	✓	✓	✓	✓	✓
realization III	X	✓	✓	✓	X	X	✓
realization IV	X	X	X	X	✓	X	✓
realization V	X	X	X	X	✓	X	✓

Based on the characteristic of the DVCC block in [19], realization II is introduced as presented in Fig.1(c). By direct analysis of the circuit, the input impedance in Eqn.3 is achieved. The positive and negative impedance can be implemented where the negative impedance is realized by employing BOICCII+ or BOCCII-. Figure 1(d) presents realization III using TA and BOCCII blocks. The input impedance is given as follows: $Z_{in} = \frac{Z_3}{a_2b_2Z_2G}$. Alternative realizations are realized by interchanging between the BOCCII$\pm$ and BOICCII$\pm$.

Using the same procedure, realization IV is presented as shown in Fig.1(e) employing Z_1 and Z_2 as general impedances and Z_3 as conductance, so the input impedance is depicted as follows: $Z_{in} = \frac{Z_1}{a_1b_1Z_2G_3}$. The positive and negative impedance can be realized by switching between the two input terminals of BOTA block. Realization V depicted Fig.1(f) is based on one active block called modified DDCCTA in [18]. It gives differential input voltage balanced output current in one block. By employing that block, the input impedance is defined as follows: $Z_{in} = \frac{Z_1}{abZ_2g_m}$.

Realizations (III-V) employ two active elements with two generalized impedances which restrict the possible implementation of the floating element as presented in Table II. Realizations I and II use four and three generalized impedances which can be used to realize any floating element as summarized in Table II. The lowest number of active and passive elements are used in realization II, which improve the circuit linearity.

III. SIMULATION RESULTS

PSPICE simulations are introduced in this section showing the reliability of the proposed emulator. This emulator circuit has been realized and implemented using the off-shelf components such as AD844 and AD633 to simulate the performance of the active blocks and voltage multiplier, respectively. Valsa CPE implementation circuit proposed in [20] is employed to simulate the fractional-order capacitor. In [21], the introduced voltage-controlled memristor emulator is used to simulate the memristor behaviour where the circuit parameters are $R_s = R_1 = 1.4k\Omega$,$R_2 = 690\Omega$,$C = 0.01\mu F$ and DC supply voltage ± 10.

FOMI (case 3) can be implemented by realizations I, II, and III where realization II is depicted in Fig.3(a) as an example for this case with simulation parameters $R = 1k\Omega$ and $C = 10nF/sec^{1-\alpha}$. The $\varphi - i$ curve at order $\alpha = 1$ is depicted in Fig.4 (a) where the HL area is decreased with

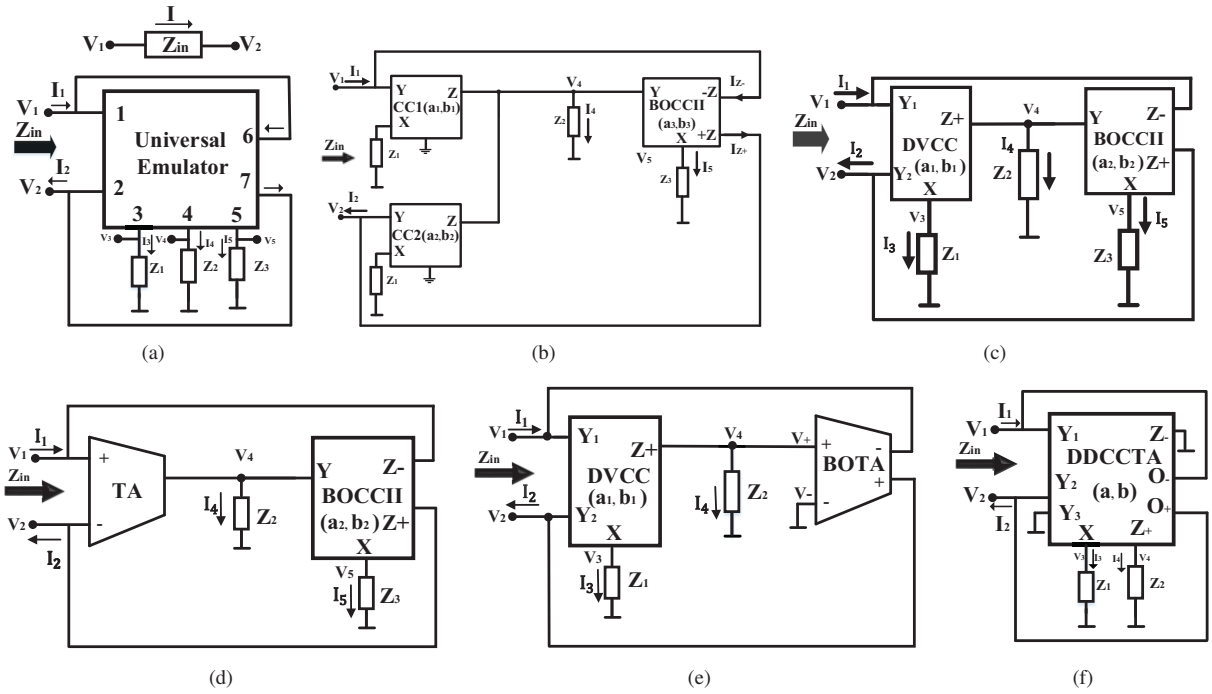


Fig. 1. (a) The proposed emulator (b) realization I, (c) realization II, (d) realization III, (e) realization IV, and (f) realization V

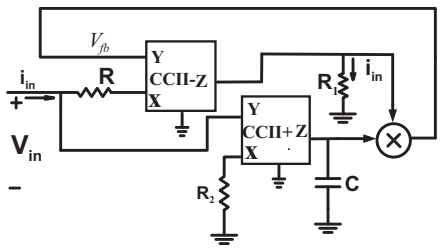


Fig. 2. Voltage-controlled memristor emulator

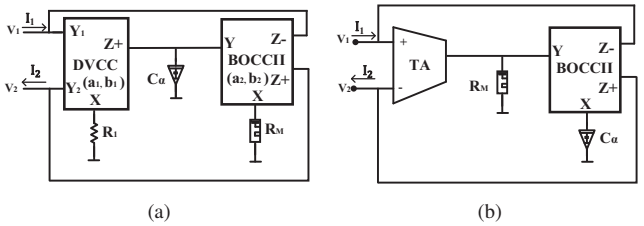


Fig. 3. (a) Floating FOMI emulator using realization II (b) FOMC emulator using realization III

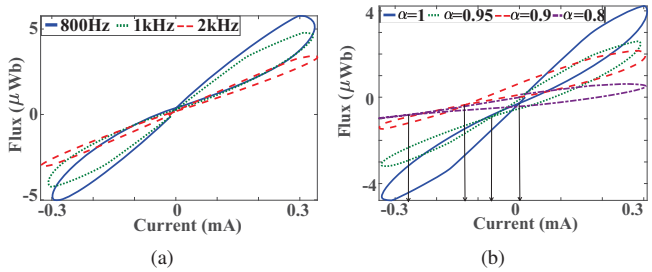


Fig. 4. The simulations results of the HL achieved using the introduced floating FOMI emulator at different frequencies (a) $\alpha = 1$ and (b) for various orders at 1kHz

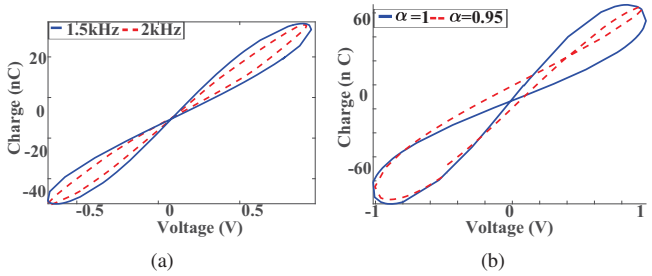
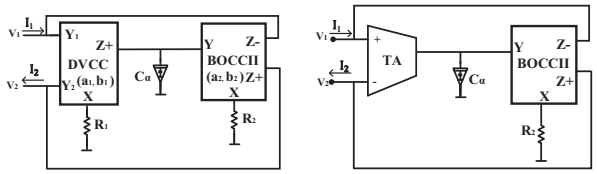


Fig. 5. The simulations results of the HL achieved using the introduced floating FOMC emulator at different frequencies (a) $\alpha = 1$ and at various orders (b)at 2kHz

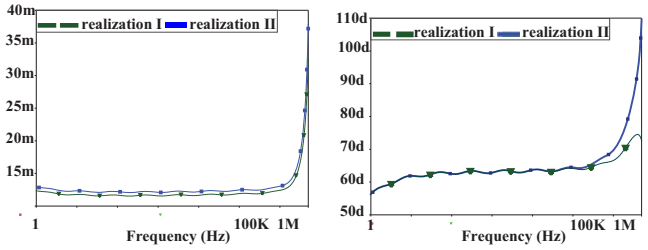
increasing the frequency. In addition, the changes of order α affects on the location of the pinched point where the drop off order α moves the pinched point away from the zero point until disappeared as depicted in Fig.4 (b). The floating FOMC (case 2) is implemented using realization III as presented in Fig.3(b) where the simulation parameters are $R = 1k\Omega, C = 10nF/scc^{1-\alpha}$. The $q-v$ curve is introduced in Fig.5 (a) that the HL is increased with decreasing the working frequency. Also, the HL and the location of pinched point are affected by changing the order α of the FOC used as depicted in Fig.5 (b).

The FOI is realized using realizations I and II as shown in Figs. 6(a) and (b), respectively. The magnitude and phase responses of FOI order $\alpha = 0.7$ are introduced in Fig.7(a) and (b) where the frequency range is between 1Hz to 500kHz,



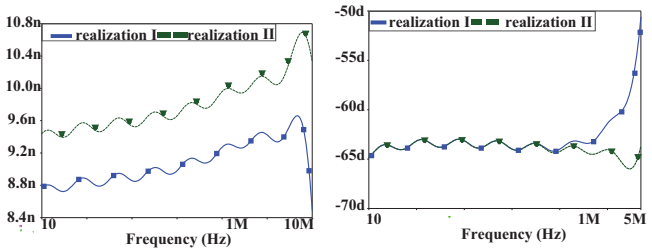
(a) (b)

Fig. 6. The FOI (a) realization I and (b) realization II



(a) (b)

Fig. 7. FOI at order $\alpha = 0.7$ using realizations II, III (a) magnitude response, and (b) phase response



(a) (b)

Fig. 8. FOC at order $\alpha = 1.7$ using realizations I and II (a) magnitude response, and (b) phase response

respectively. Also, the FOC is performed using realizations I and II at $\alpha = 1.3$. The magnitude and phase response at $\alpha = 1.7$ are presented in Figs. 8(a) and (b) where the frequency range is between 1Hz to 100kHz, respectively.

IV. Conclusion

A Universal floating emulator was proposed employing generalized grounded elements. Five realizations for the proposed emulator were introduced using different active elements. The introduced emulators were employed to realize any floating elements such as FOMEs and FOEs. Different cases of the floating element were validated on PSPICE simulations using AD844 and passive elements. The effect of fractional-order α on the HL area of FOMEs were discussed at different orders.

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