A Low-Power Time-Domain Comparator for IoT Applications

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***Abstract*—This paper introduces a low-power time-domain comparator with a modified current starved inverter circuit. The proposed comparator converts the analog input voltage into a time delay that creates a phase difference between the input signal and the reference signal. Then a phase detector is utilized to determine either the input signal is leading or lagging compared to the reference signal. Moreover, the power optimization is achieved by limiting the short circuit power (P_{SC}) that passes through both charging and discharging phases. A prototype of the proposed comparator is designed and simulated in 0.13 μm CMOS technology where it draws 0.6 μA from a 1 V supply with a sampling rate equals 10 MHz. Moreover, the simulation results of the proposed comparator offer a FoM of 60 fJ/conversion step. Finally, the proposed time-domain comparator circuit is compatible with wide range of applications (i.e., internet of things (IoT) sensors and integrated DC-DC converters).**

***Index Terms*—low-power, time-domain, comparator design, time-based comparator, voltage-to-time converter, controllable delay cell, IoT applications.**

I. Introduction

In the last few years, there has been a rapid growth in need of wireless sensor nodes for the internet of things (IoT) applications. This growth has led to evolutional milestones in IoT applications such as home automation, healthcare, and environmental/manufacture monitoring. However, these sensing nodes are not installed under normal conditions and suffer from unpredictable dynamics. Therefore, they are required to achieve extremely low-power consumption. As they are supplied by either a battery or an energy harvesting module that requires low-power and high-efficiency power management integrated circuits.

Typically, IoT sensors output analog signals similar to the environmental surroundings while the data processing is done digitally through digital signal processors (DSPs). Therefore, analog-to-digital converters (ADCs) are essential blocks for interfacing data from the analog domain, through sensors, transducers, or receivers and DSPs. For low-power purposes: the successive approximation register (SAR) ADC is preferred [1]. Since its minimal use of analog circuit blocks. SAR-ADC mainly consumes power in two blocks the comparator and the digital-to-analog converter (DAC).

StrongArm comparator and double-tail latched comparator are commonly used for SAR-ADC design due to their high speed and power efficiency [2]. However, these comparator designs suffer from a large offset in order of tens of mV and large kickback noise in order of hundreds of μV. This requires additional circuits for offset and noise cancellation which increase the implementation cost (i.e., power and area).

Recently, an alternative solution, time-domain comparator, is introduced in [1], [2], [3], [4], [5], [6], [7] over the conventional voltage-domain comparator. The time-domain comparator encodes the input voltage difference into a time delay using a voltage-to-time converter (VTC) followed by a single-bit time-to-digital converter (TDC) that digitizes the pulse time delay. Moreover, the time-domain comparator is composed of almost digital circuits getting benefit from CMOS technology scaling. Since the improvement in the digital circuits surpasses the improvement in the analog circuits for two reasons: 1) the supply voltage scales down with the technology leading to decreasing the voltage swing. However, the noise does not scale with technology leading to smaller signal to noise ratio that makes the analog system less immune to the noise and 2) the threshold voltage does not scale with the same factor as the supply voltage. Therefore, the cascoding technique becomes harder and more difficult [8], [9].

The rest of the paper is organized as follows. The proposed time-domain comparator is discussed in Section II, while the simulation results are presented in Section III. Finally, a conclusion is drawn in Section IV.

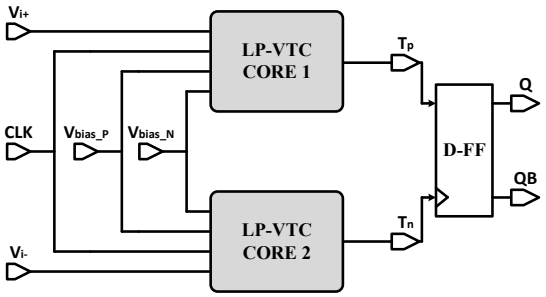
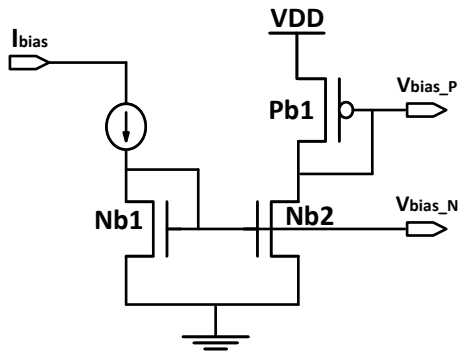


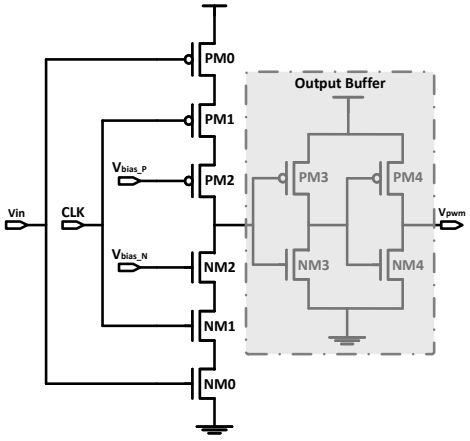
Fig. 1: Proposed Time-Domain Comparator Block Diagram

II. PROPOSED TIME-DOMAIN COMPARATOR ARCHITECTURE

Fig. 1 portrays the proposed time-based comparator that transforms the analog input signal into a delay pulse through a low-power VTC (LP-VTC) circuit. This time delay difference represents a phase difference between the two LP-VTC cores. This phase difference is detected by a phase detector. The analog conversion process of the input signal into a delay pulse through LP-VTC is also referred to as either a Pulse Position Modulator (PPM) or Pulse Width Modulator (PWM), depending on whether the delay is applied to one or both edges of the input clock signal. Using a conventional VTC circuit that is based on an NMOS-based current starved inverter [10], [9] suffers from short-circuit power (P_{SC}).



(a) Biasing Circuit Schematic



(b) Low-Power VTC Circuit Schematic

Fig. 2: Proposed Comparator Circuit Implementation

Fig. 2 shows the circuit implementation of the proposed LP-VTC circuit as well as its biasing circuit. The modified current starved circuit utilizes two input bias voltages to limit the maximum current that passes through the charging phase and the discharging phase [11]. During the charging phase (CLK logic-low), the output node is charged through PM0 with a current rate less than or equal the limiting current in PM2, modeling PM1 as a low resistance. During the discharging

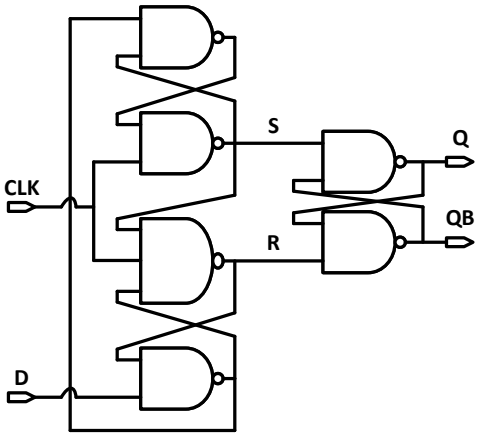


Fig. 3: A Positive-Edge Triggered D-FlipFlop Circuit Schematic

phase (CLK logic-high), the output node is discharged through NM0 with a current rate less than or equal the limiting current in NM2, modeling NM1 as a low resistance. Finally, the current mismatch in the biasing circuit is eliminated by transistors matching. Matching is guaranteed by increasing the transistor length (L) relative to the transistor width (W), as at a fixed current (I), the normalized current mismatch is inversely proportional to L [12].

For D-FlipFlop (D-FF) implementation: a positive edge triggered FlipFlop is shown in Fig. 3. This D-FF is composed of two stages where the first stage is an SR-latch with enable signal (CLK). And the second stage is a static SR-latch. The circuit mechanism of D-FF works as follows [13]: 1) CLK is logic-low: the output of both NAND gates equals logic-high and 2) CLK is logic-high: the output follows the input signal (D). Meanwhile, the shown topology is a positive edge triggered D-FF. As it synchronizes the output state changes during the clock pulse transition from logic-high to logic-low. The comparator least significant bit (LSB) is mainly controlled by the D-FF setup time (T_{su}). However, a sense amplifier based D-FF has a lower setup time than the adopted D-FF but it dissipates more power [14], [15], [16].

III. SIMULATION RESULTS

A prototype of the proposed time-domain comparator is implemented by hardware calibrated UMC 0.13 μm technology. The proposed comparator occupies 0.0058 mm^2. Moreover, all simulations are carried out using Cadence Virtuoso. Using 1 V supply and 100 nA biasing current, the prototype is simulated and verified as follows:

A. Overdrive Recovery Test

Overdrive recovery test portrays an essential role in the comparator design. Since this test indicates either the recovery time is enough to discharge the previous state or an error will occur in the comparator output [17]. Fig. 5 shows both the

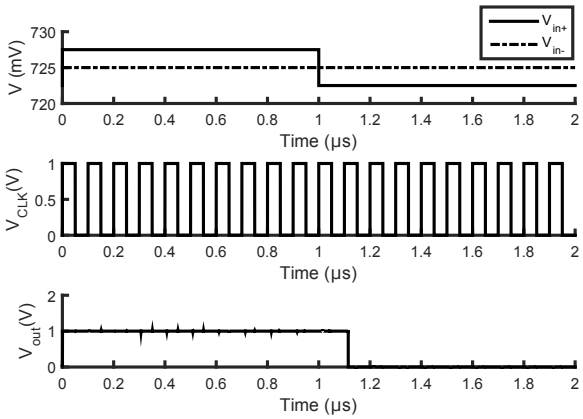


Fig. 4: Comparator Overdrive Recovery Test (V_{in} = 2 mV and f_s = 10 MHz)

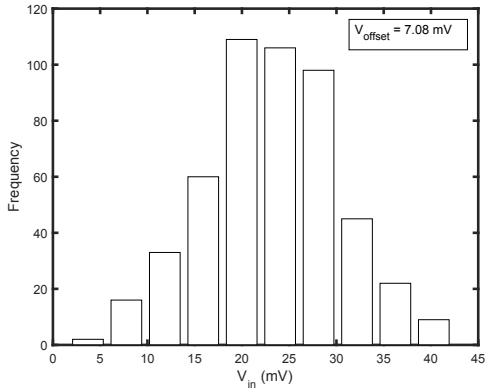


Fig. 5: Offset Voltage Monte-Carlo Simulation

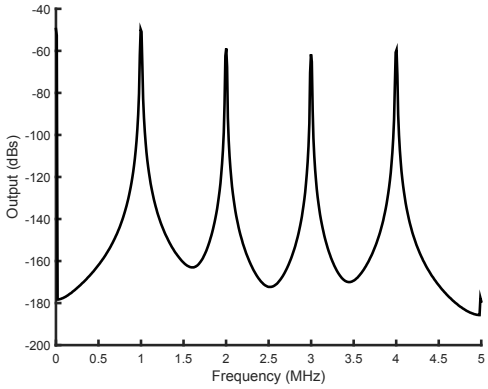


Fig. 6: Output Spectrum for Sinusoidal Input of 1 MHz Input Frequency

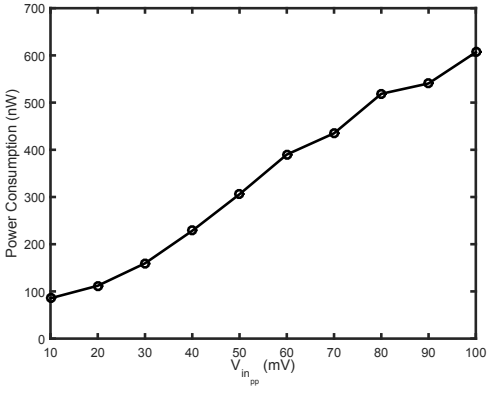


Fig. 7: Power Consumption versus $V_{in_{pp}}$

input and the corresponding output waveforms after applying overdrive recovery test by 2 mV input difference. The difference is reduced to determine the comparator sensitivity.

B. Input referred offset voltage calculation

Fig. 6 shows the input referred offset voltage using Monte-Carlo simulations. Offset voltage analysis is done by ramping V_{i+} signal from -25 mV till 25 mV while fixing V_{i-} by the input common mode voltage (V_{cm}) then measuring the crossing time of the output signal from low to high over 500 samples.

C. Linearity Test

Fig. 7 shows Fast Fourier Transform (FFT) of the output signal with an input signal frequency less than the sampling frequency by 10X. The single tone test acts as an indicator for the comparator linearity as it measures the signal-to-noise ratio (SNR). The proposed comparator represents 1-bit ADC where SNR equals -9.08 dBs.

D. Power Consumption

Fig. 8 shows the power consumption of the proposed comparator while varying the input peak-to-peak voltage $(V_{in_{pp}})$. In this design, the power consumption is calculated at half the sampling rate for each design. And V_{cm} is set to be 725 mV. At low input voltages, the power is dissipated only through the biasing circuit while the core VTC circuit is off.

E. Figure-of-Merit (FoM)

To make a comparison with other comparators operating with different design aspects, a figure-of-merit (FoM), defined by equation 1, is used to compare the proposed work with various comparator designs [21]:

$$FoM = \frac{P}{f_s} \tag{1}$$

Where P is the power consumption, and f_s is the sampling frequency. Moreover, the voltage-domain comparators [19], [20] are optimized on the gate level using the same technologyto guarantee fair comparison by [22].Table I shows the state-of-the-art ADCs with different sampling rates and resolution. From the shown results, this time-domain comparator has one of the best power efficiencies of published work. The power consumption of the proposed comparator circuit is lower than that in [4] and [20] by factors of 1.64X and 31X, respectively. However, the implementation area of the

TABLE I: Performance summary between this work and the state-of-the-art comparator architectures

Design Parameter	[4]	[1]	[18]	[19]	[20]	This work
Technology (μm)	0.18	0.18	0.18	0.13	0.13	0.13
Supply Voltage (V)	1	0.6	0.5	0.6	1.2	1
Topology	Time-Domain	Time-Domain	Time-Domain	Voltage-Domain	Voltage-Domain	Time-Domain
LSB (mV)	0.2	0.585	0.146	0.5	0.01	2
Offset (mV)	N/A	N/A	N/A	4.32	51.5e-6	7.08
Speed (MHz)	1.4	0.1	0.2	0.3	100	10
Power (μW)	1	0.13	0.6	0.068	19	0.61
Area (μm^2)	26632	2375	N/A	180	1925	5750
FoM (pJ/Conv)	0.71	1.3	3	0.34	0.12	0.06

proposed time-domain comparator as well as the other time-domain topologies [4], [1]is larger than the dynamic voltage domain comparators [19], [20].

IV. Conclusion

Using 1 V supply and UMC 0.13 μm technology, a time-domain comparator is introduced for low-power applications. This indirect conversion method optimizes the power consumption by encoding the input voltage difference into time-domain first then using a phase detector to digitize the phase difference. Moreover, this time-domain comparator provides 10M conversions per second with 2 mV sensitivity while it consumes 0.6 μW. Finally, the proposed architecture is advantageous in deep-submicron technology compared to voltage-based comparators. As it takes the full privileges of the switching characteristics due to CMOS technology scaling.

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