ACTIVE R SIMULATION OF AN INDUCTOR AND A SERIES RESONATOR

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Abstract

A technique for simulating a driving point impedance which employs only resistors and internally compensated operational amplifiers, is presented. Using the proposed technique; three circuits for realizing a nonideal grounded inductance, and three circuits for realizing a series resonator are introduced.

1. INTRODUCTION

Active R design using the 6 dBs/octave rolloff characteristics of operational amplifiers has recently received considerable attention. The active R synthesis of an impedance is interestingly a new subject which was attacked earlier by Allen and Means[1], who dealt with inductor simulation.

In this paper a general procedure for simulating a driving point impedance is presented. Consequently the realization of a nonideal grounded inductance is illustrated by three circuit examples. The method of inductor simulation is clearly different from that of Allen and Means[1].

The realization of a series resonator is also illustrated by three circuit examples. Each of the proposed circuits resembles a series resonator containing a capacitor, a resistor and a FDNR element which, according to Bruton[2] transformation, is equivalent to an LCR series resonance circuit.

2. ACTIVE R SIMULATION OF DRIVING POINT IMPEDANCE

From the diagram in Fig. 1

$$Z_{in} = \frac{V_1}{I_1} \tag{1}$$

$$I_1 = \frac{V_1 - V_2}{R_o} \tag{2}$$

$$\frac{V_2}{V_1} = T(s) \tag{3}$$

From the above equations, it is seen that:

$$Z_{in} = \frac{R_o}{1 - T(s)} \tag{4}$$

This represents a driving point impedance which can be arbitrarily synthesized by the appropriate choice of T(s).

Assuming $A_i = \frac{GB_i}{s} = \frac{2\pi f_{Ci}}{s}$, $(i = 1,2)$ (5)

where GB is the gain-bandwidth product or the unity gain cross over radian frequency of the operational amplifier; the block T(s) of Fig. 1 can be realized as an active R one, which completely dispense capacitors, but uses only resistors and internally compensated operational amplifiers. The synthesis of a specific impedance function imposes some restrictions on the network used for the realization.

3. INDUCTOR REALIZATION

The inductances in Fig. 2 are realized as follows:

<u>First inductance</u>

$$\frac{V_3}{V_1} = \frac{b}{1 + s\left(\frac{b}{GB_1}\right)}, \quad b = 1 + \frac{R_2}{R_1} \tag{6}$$

$$V_2 = \frac{V_1 - V_3}{1 + \frac{2}{A_2}} \simeq V_1 - V_3 \quad (7)$$

Thus the second stage can be used as a unity gain differential amplifier, provided that:

$$f << \frac{f_{c_2}}{2} \quad (8)$$

From equations (6), (7) one obtains:

$$T(s) = \frac{V_2}{V_1} = \frac{(1 - b) + s(b/GB_1)}{1 + s(b/GB_1)} \quad (9)$$

Applying (4), with R_4 chosen as large as possible it follows that:

$$Z_{in} = R + sL \quad (10)$$

with:

$$R = \frac{R_o}{b}, \; L = \frac{R_o}{GB_1}, \; Q = \frac{\omega L}{R} = b \frac{f}{f_{c_1}} \quad (11)$$

Thus to design an inductance L with a specified Q at a certain frequency f, the design equations are:

$$R_o = L.GB_1, \; \frac{R_2}{R_1} = Q. \frac{f_{c_1}}{f} - 1 \quad (12)$$

It is obvious, from (11), that Q increases linearly with f. However, it is not possible to increase f independently since the condition of (8) must be satisfied.

Second inductance

$$V_2 = \frac{V_1 - V_3}{1 + \frac{2}{A_1}} \simeq V_1 - V_3 \quad (13)$$

Thus the first stage is treated as a unity gain differential amplifier, provided that:

$$f << \frac{f_{c_1}}{2} \quad (14)$$

It can be shown that:

$$T(s) = \frac{V_2}{V_1} = \frac{s}{s + B.GB_2}, \; B = \frac{R_4}{R_3+R_4} \quad (15)$$

Applying (4), and by choosing R_1 as large as possible, it follows that:

$$Z_{in} = R + sL$$

with:

$$R = R_o, \; L = \frac{R_o}{B.GB_2}, \; Q = \frac{1}{B} \cdot \frac{f}{f_{c_2}} \quad (16)$$

It is evident, from (11) and (16), that for the same value of L this circuit utilizes a value of R_o smaller than that of the previous circuit, which is more suitable for integration. Consequently, this circuit is superior to the previous one when a high value of the inductance is required.

Third inductance

$$T(s) = \frac{V_2}{V_1} = - \frac{a}{1 + s(\frac{b}{GB})}, \; b = 1+a, \; a = \frac{R_2}{R_1} \quad (17)$$

Applying (4), taking $R_1 >> R_o$, it follows that:

$$Y_{in} = \frac{1}{R'} + \frac{1}{R + sL} \quad (18)$$

with:

$$R' = R_o, \; R = \frac{R_o}{a}, \; L = \frac{R_o}{GB} \cdot \frac{b}{a} \quad (19)$$

Of course this inductance is better than the previous two inductances in using only one operational amplifier, and in having no restrictions such as those of (8) or (14). The main disadvantage is the existence of a shunting resistance R', which, for design considerations, cannot be avoided or chosen as large as possible. The equivalent values of the inductance, series resistance and quality factor are:

$$R_{eq} = \frac{(R+R')RR' + \omega^2 L^2 R'}{(R+R')^2 + \omega^2 L^2},$$

$$L_{eq} = \frac{LR'^2}{(R+R')^2 + \omega^2 L^2},$$

$$Q_{eq} = \frac{\omega L R'}{(R+R')R + \omega^2 L^2} \quad (20)$$

4. SERIES RESONATOR REALIZATION

By making T(s) of the form:

$$T(s) = \frac{a_1 s + a_2}{b_o s^2 + b_1 s + b_2} \quad (21)$$

with:

$$b_1 = a_1, \; b_2 = a_2 \quad (22)$$

and by applying (4), it follows that:

$$Z_{in} = R + \frac{1}{Cs} + \frac{1}{Ds^2} \quad (23)$$

which represents a series DCR resonator

whose equivalent circuit is shown in Fig. 3.a, with:

$$R = R_o, \quad C = \frac{b_o}{a_1 \cdot R_o}, \quad D = \frac{b_o}{a_2 \cdot R_o} \qquad (24)$$

Equation (23) is that of Bruton[2]. With the aid of the equivalent RLC series resonance circuit it can be proved that:

$$\omega_o = \frac{1}{\sqrt{RD}}, \quad Q = C\sqrt{R/D} \qquad (25)$$

By applying the equations (21)-(25) on the circuits of Fig. 3.b, the results are shown in Table 1. A quick survey for the circuits under consideration reveals that:

It is too difficult for circuit 1 to guarantee $A_1 = A_2$ unless both operational amplifiers are integrated on the same chip. Also, for a given GB it is possible to separately specify one performance factor namely R or C or D while the other two factors are dependent.

It is to be noted that the resistors R_5, R_6 in both cases of the circuits 2,3 should be chosen as large as possible. This enables us to consider that the grounded resistance shunting the series resonator as having an infinite value, which is a reasonable approximation.

As for circuit 2, it is advantageous over circuit 1 in the avoidance of the necessity of having identical operational amplifiers. Also, two performance factors out of three can be separately specified. The two circuits are only similar in having Q = 1.

Concerning circuit 3, it is possible to get Q > 1 which is an advantage over the previous two circuits.

5. REFERENCES

1. P.E. Allen and J.A. Means, "Inductor simulation derived from an amplifier rolloff characteristic", IEEE. Trans. on Circuit Theory, pp. 395-396, July 1972.

2. L.T. Bruton, "Network transfer functions using the concept of FDNR", IEEE. Trans. on Circuit Theory, Vol. CT-16, pp. 406-408, August 1969.

Table 1

Circuit No	1	2	3
Circuit parameters		$\alpha = \frac{R_6}{R_5+R_6}$ $\gamma = \frac{R_4}{R_3+R_4}$ $b = 1 + \frac{R_2}{R_1}$	$b = 1+a$ $a = \frac{R_2}{R_1}$
Realizability conditions	$A_1=A_2$	$\alpha = \gamma$ $\alpha b \frac{GB_1}{GB_2} = 1$ $R_5, R_6 >>$	m=n=b=k $R_5, R_6 >>$
R	R_o	R_o	R_o
C	$\frac{1}{R_o \cdot GB}$	$\frac{b}{R_o \cdot GB_2}$	$\frac{k}{R_o \cdot GB_2}$
D	$\frac{1}{R_o (GB)^2}$	$\frac{b}{R_o \cdot GB_1 \cdot GB_2}$	$\frac{k^2}{(k-1) R_o} \times \frac{1}{GB_1 \cdot GB_2}$
f_o	f_c	$\frac{f_{c2}}{b}$	$\frac{\sqrt{(k-1) f_{c1} \cdot f_{c2}}}{k}$
Q	1	1	$\sqrt{(k-1) \frac{f_{c1}}{f_{c2}}}$

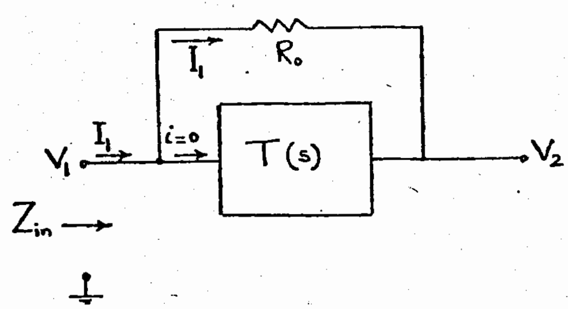
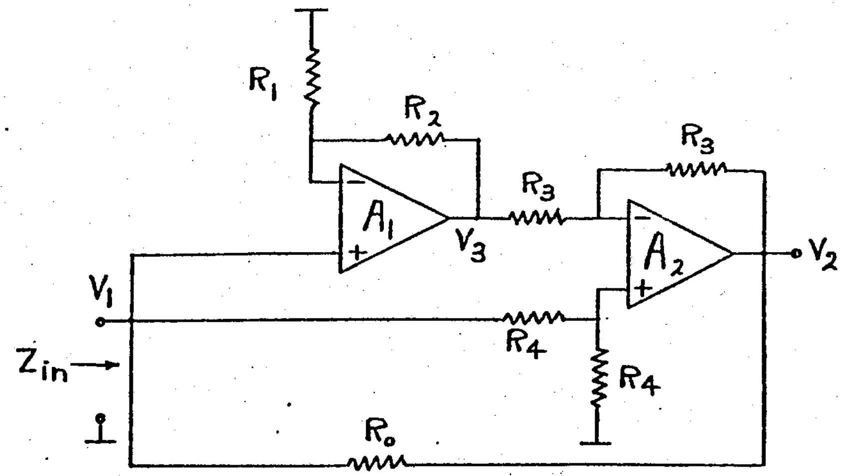
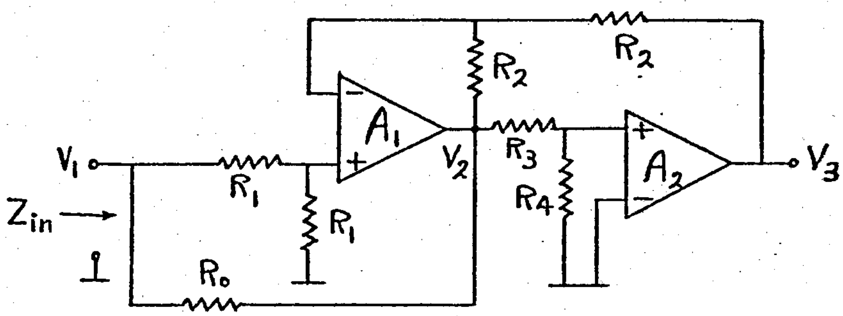


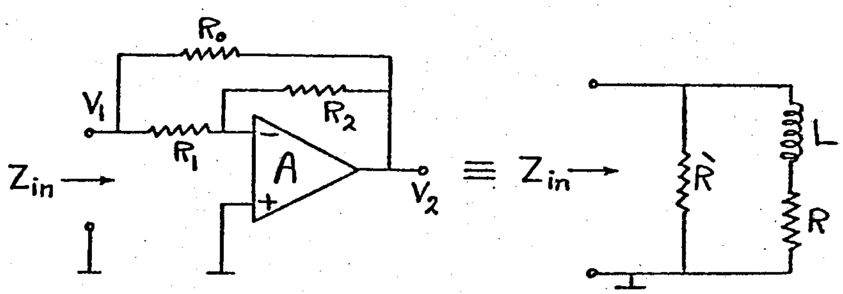
Fig 1



First inductance



Second inductance



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Third inductance

Fig 2. Grounded inductance realization

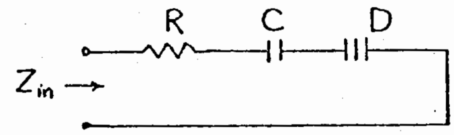
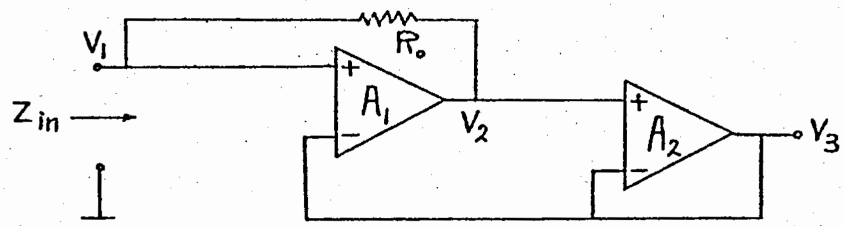
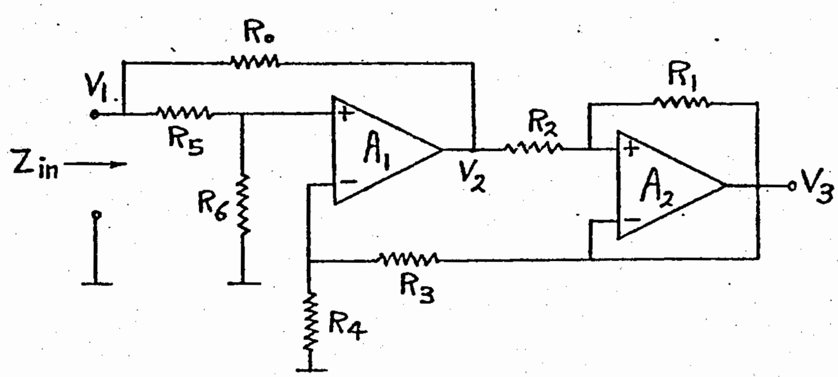


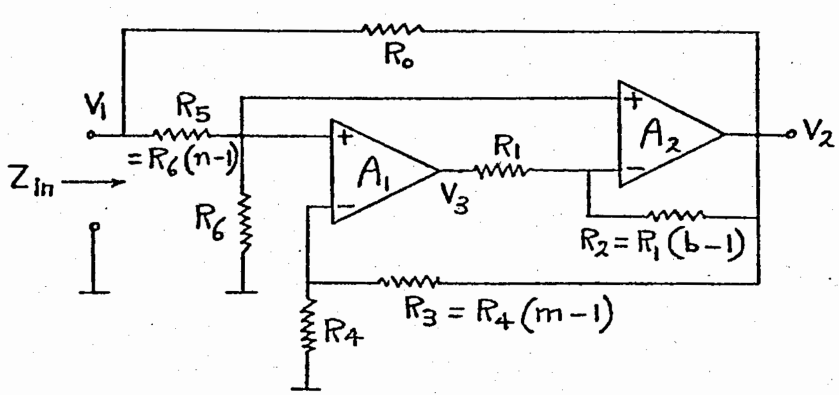
Fig 3a.



First resonator



Second resonator



Third resonator

Fig 3b. Series resonator realization