Transactions Briefs

Variable Gain Amplifiers Based on a New Approximation Method to Realize the Exponential Function

Khaled M. Abdelfattah and Ahmed M. Soliman

***Abstract*—A new current mode variable-gain amplifier (VGA) is developed. The new circuit is based on a novel approximation function that is very close to the ideal exponential relation over a very wide range. Pspice simulations are provided based on Mietec 0.5-μm CMOS technology. The simulations show that the dynamic range achieved is over 50 dB in a single stage. The proposed circuit consumes average power less than 1.2 mW using $\pm$1.5 V supply voltages.**

***Index Terms*—Variable gain amplifiers.**

I. Introduction

Variable-gain amplifiers (VGAs) are employed in many applications to maximize the dynamic range of the overall system [1]. VGA is always used to build an automatic gain control loop (AGC). An AGC is used in any communication system [1], and used also in hearing aid applications [2]. An important feature of VGAs is that the gain should increase linearly on a decibel scale, which means that the gain should have an exponential relation with respect to the control signal. This allows for the amplifier to have a wide dynamic range, and also makes the settling time of the AGC constant. However, due to the lack of the exponential relation in the devices fabricated in CMOS technology, one of the solutions was to use the parasitic bipolar transistors to have the exponential relation [3]. This solution was unsatisfactory due to the bad frequency response of the parasitic devices, hence, approximation methods have been introduced [3]–[9] with several realization methods using MOS transistors.

There are two approximation function that have been introduced in the literature with many realizations offered to enhance the performance in terms of the power consumption, the speed, and the dynamic range [3]–[9]. The first method is to expand the exponential relation with its Taylor series and truncate the expansion according to the required accuracy needed.

The second method, which is the mostly used, is based on the following equation:

$$G = \exp(X) = \frac{\exp\left(\frac{X}{2}\right)}{\exp\left(-\frac{X}{2}\right)} \approx \frac{1+\frac{X}{2}}{1-\frac{X}{2}}. \tag{1}$$

A primary drawback of this method is that the region over which the above equation is valid is restricted to

$$-1.4 < X > 1.4.$$

Beyond this region, the difference between the original exponential function and the approximation function will be more than 3 dB. This means that the maximum dynamic range achieved is about 30 dB.

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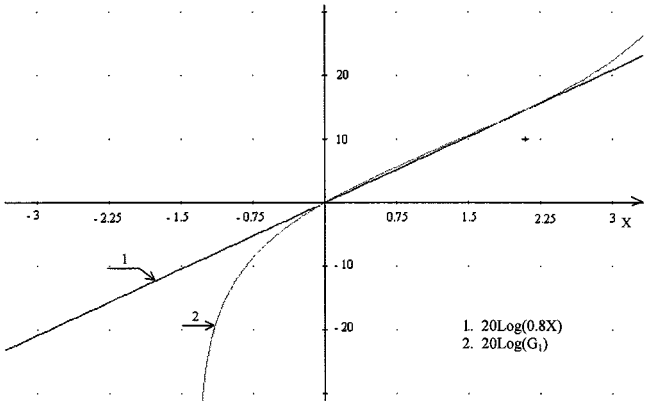

Fig. 1. Approximation function G_1 and $\exp(0.8X)$ on a decibel scale.

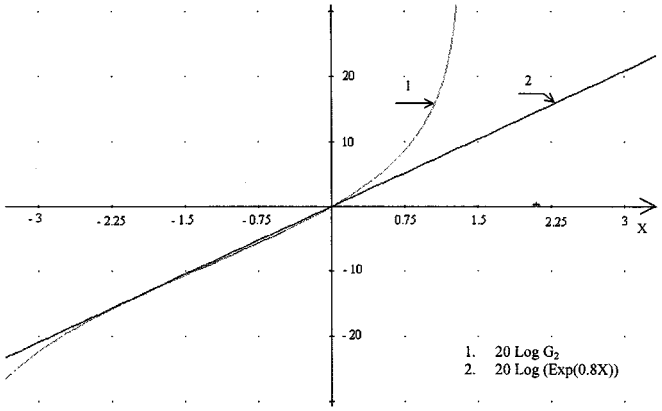

Fig. 2. Approximation function G_2 and $\exp(0.8X)$ on a decibel scale.

II. The Proposed Idea

The problem with the approximation function of (1) is that as X approaches 2, or -2, the value of the function approaches ∞ and zero, respectively. Thus, the rate of change of the function becomes more rapid than the original function for values of $|X| > 1.4$, and thus, a significant deviation from the original function is produced.

If another approximation is used where the values of X at which the function equals ∞ and zero are increased, a better accuracy in representing the exponential relation is expected.

Consider the gain expression G that is given by the following relation:

$$G = \exp(X) = \frac{\exp(\alpha X)}{\exp(-(1-\alpha)X)} \approx \frac{1+\alpha X}{1-(1-\alpha)X}. \tag{2}$$

Controlling the value of α will control the values at which the function equals ∞ and zero. Unfortunately, one can not find one value of α that increases the range for both positive and negative values of X.

Simulation results show that the optimum selection of α should be either 0.25 or 0.75, depending on whether it is required to increase the negative or positive range of X.

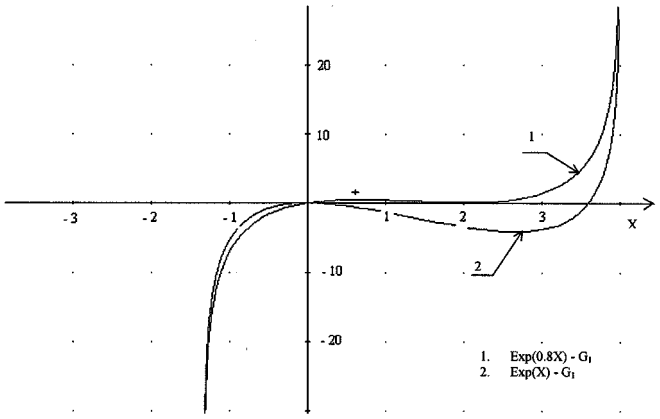

Fig. 3. Difference between the proposed function G_1 and $\exp(X)$ and also the difference between the same function G_1 and $\exp(0.8X)$ on a decibel scale.

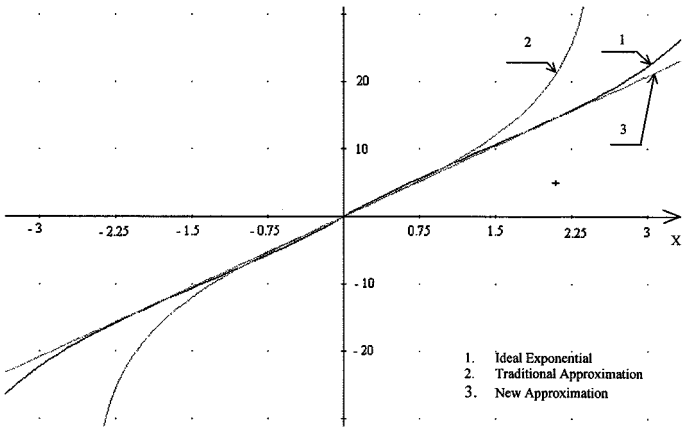

Fig. 4. New approximation function and conventional approximation function and the ideal exponential on a decibel scale.

Based on the above optimum selection of α, two functions G_1 and G_2 are introduced and defined as follows:

$$G_1 = \exp(X) = \frac{\exp\left(\frac{3X}{4}\right)}{\exp\left(-\frac{X}{4}\right)} \approx \frac{1+\frac{3X}{4}}{1-\frac{X}{4}} \tag{3}$$

$$G_2 = \exp(X) = \frac{\exp\left(\frac{X}{4}\right)}{\exp\left(-\frac{3X}{4}\right)} \approx \frac{1+\frac{X}{4}}{1-\frac{3X}{4}}. \tag{4}$$

Plotting the above functions together with $\exp(X)$ versus X, shows significant improvement in the range over which the function increases linearly on a decibel scale, however, there is difference between $\exp(X)$ and G_1 and G_2. This calls for comparing G_1 and G_2 with other decibel-linearly increasing functions. G_1 and G_2 show perfect matching with $\exp(0.8X)$ in the region 0 to 3 for G_1 and in the region -3 to 0 for G_2.

Figs. 1 and 2 show G_1 and G_2 together with $\exp(0.8X)$ on a decibel scale. Fig. 3, shows the difference between G_1 and $\exp(X)$, and also the difference between G_1 and $\exp(0.8X)$ on a decibel scale versus X. It is evident that $\exp(0.8X)$ is much better suited to match G_1 and G_2 than $\exp(X)$.

It is noted from Figs. 1 and 2 that if a combined function G_3 is realized such that

$$\begin{aligned} G_3 &= G_1 \text{ For } X > 0 \\ &= G_2 \text{ For } X < 0. \end{aligned} \tag{5}$$

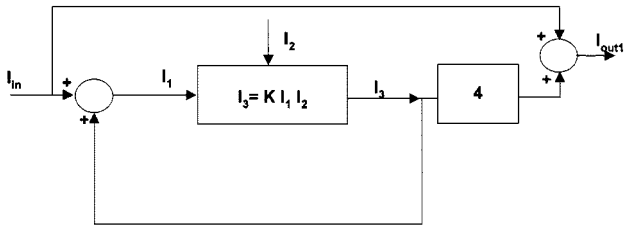

Fig. 5. Block diagram for the realization of G_1.

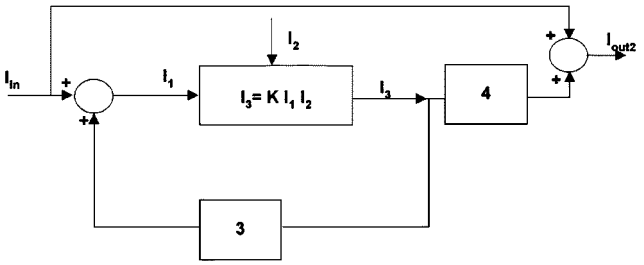

Fig. 6. Block diagram for the realization of G_2.

TABLE I
ASPECT RATIOS OF TRANSISTORS IN THE CIRCUIT OF FIG. 10 WHEN REALIZING G_1

Transistors	Aspect ratios (W/L)
M1A,M1B,M2A,M2B	5/5
M3A,M3B,M4A,M4B	5/5
M5A,M5B,M6A,M6B	10/5
M7A,M7B,M8,M10,M11	5/5
M9,M13,M14,M15	2.5/5
M12	20/5
M15	10/5
M16,M17,M18,M19	2.5/5
M20, M21,M22,M23	5/5

TABLE II
ASPECT RATIOS OF THE TRANSISTORS OF THE CIRCUIT OF FIG. 10 WHEN REALIZING G_2

Transistors	Aspect ratios (W/L)
M1A,M1B,M2A,M2B	5/5
M3A,M3B,M4A,M4B	5/5
M5A,M5B,M6A,M6B	10/5
M7A,M7B,M8	5/5
M9,M15	2.5/5
M10,M11	15/5
M12	20/5
M13,M14	7.5/5
M15	10/5
M16,M17,M18,M19	2.5/5
M20, M21,M22,M23	5/5

The dynamic range of the new gain function is expected to be more than 50 dB as shown in Fig. 4. For the purpose of fair comparison, (1) is modified to

$$G^* = \exp(0.8X) \approx \frac{1+0.4X}{1-0.4X}. \tag{6}$$

Fig. 4 compares G_3 and G^* in representing the ideal exponential function $\exp(0.8X)$. It is very clear how much improvement is achieved using G_3.

III. CIRCUIT DESCRIPTION

For realizing the function G_3, a new idea based on a feedback system is used, the block diagrams used to implement G_1 and G_2 are shown in

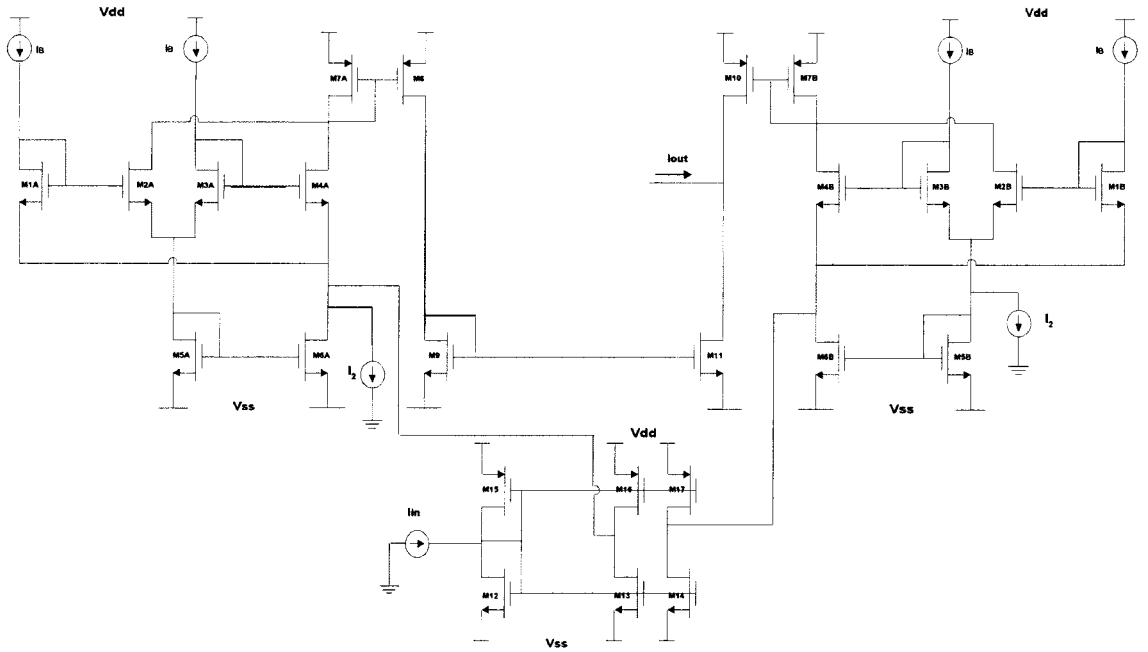

Fig. 7. The multiplier circuit introduced in [10].

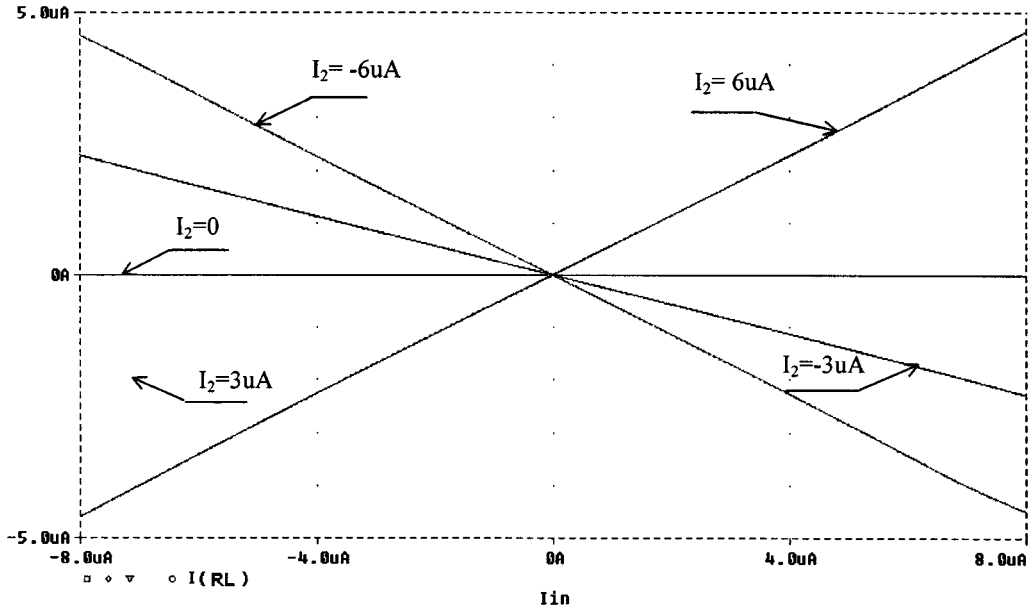

Fig. 8. DC simulation of the multiplier.

Figs. 5 and 6, respectively, where the input, output, and control signal are chosen to be current signals.

The main building block of Figs. 5 and 6 is the multiplier which makes the realization of either G_1 or G_2 very low power, because unlike other topologies [4] that used a separate circuit to generate the exponential and used its output to modulate the input signal using a multiplier, the presented circuit uses only a multiplier to realize G_1 and a similar one for G_2. The idea can also be applied to voltage mode circuits using a voltage mode multiplier.

An efficient four-quadrant multiplier that is previously reported [10] will be used and shown in Fig. 7. The multiplier is characterized by

$$I_3 = \frac{I_1 I_2}{2I_B} \tag{7}$$

where I_B is an internal bias current shown in Fig. 7.

Simulation results of the multiplier are shown in Figs. 8 and 9, where in Fig. 8 I_2 takes different values starting from -6 μA to $+6$ μA in steps of 3 μA. In Fig. 9, ac analysis is performed with different values of I_2 as shown in the figure.

Using the multiplier characteristic given in (7), and substituting in (3) and (4), gives

$$G_1 = \frac{I_{\text{out1}}}{I_{\text{in}}} = \frac{1 + \frac{3I_2}{2I_B}}{I - \frac{I_2}{2I_B}} \tag{8}$$

$$G_2 = \frac{I_{\text{out2}}}{I_{\text{in}}} = \frac{1 + \frac{I_2}{2I_B}}{I - \frac{3I_2}{2I_B}} \tag{9}$$

where

I_{in}	input current;
I_{out1} , I_{out2}	output currents of both functions;
I_2	control current.

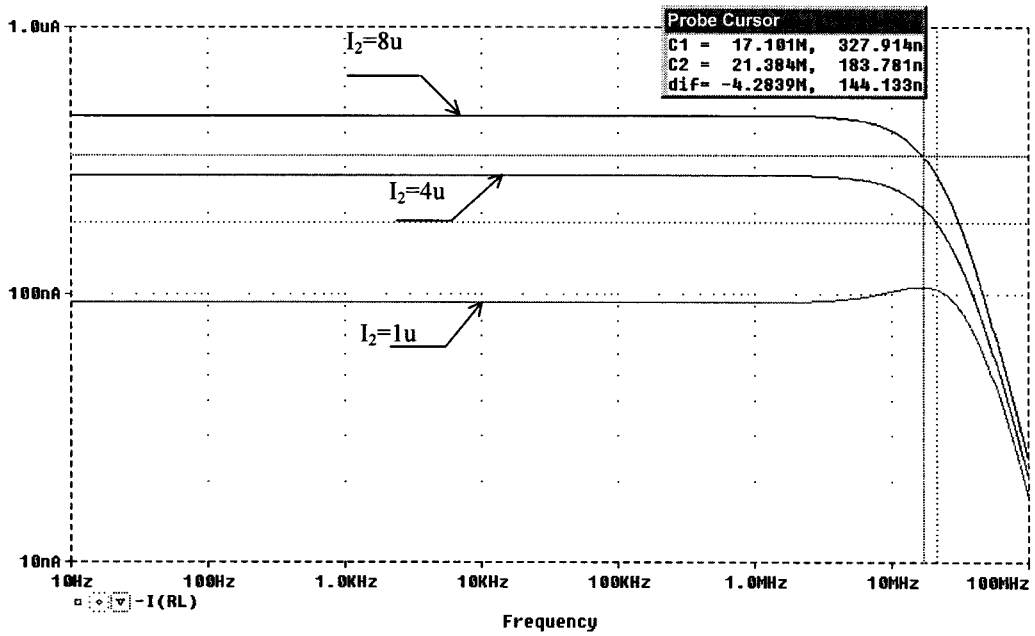

Fig. 9. Frequency response of the multiplier for three different gain values.

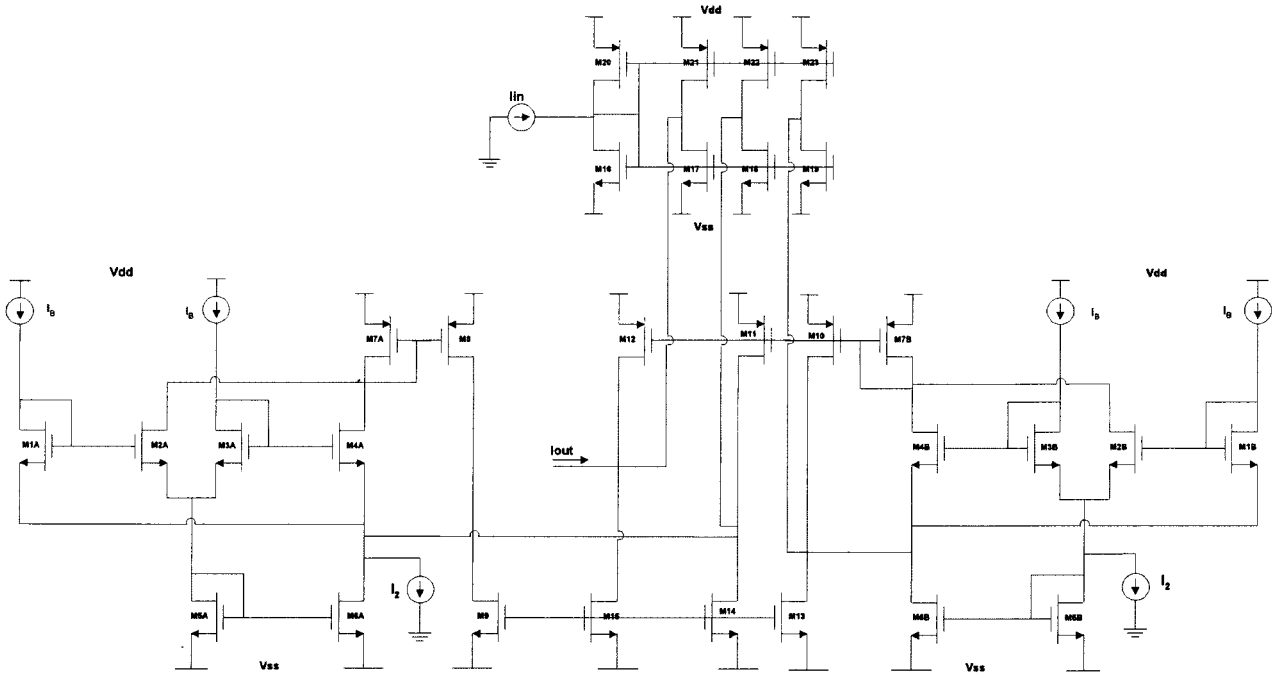

Fig. 10. Circuit used for implementing G_1 and G_2.

Circuit implementations of both G_1 and G_2 are based on Fig. 10 but with different aspect ratios. Tables I and II give the aspect ratios of the transistors of Fig. 10, when used to implement G1 and G2, respectively.

Combining both functions together to build G_3 is realized as in Fig. 11, where a simple multiplexer circuit that is controlled via I_2 is used to select either $I_{\text{out}1}$ or $I_{\text{out}2}$. A simple control circuit for the VGA is shown in Fig. 12. However, both transmission gates used in the MUX are off when I_2 equals zero, which will lead to zero gain at zero control current. Fortunately, solving this this problem is pretty easy and can be done by noticing that at each of the output nodes of G_1 or G_2, a copy of the input current is being added, so instead of adding this copy at the output of both G_1 and G_2 we can add it once at the output of the whole circuit, i.e., after the transmission gates. Thus, if the control current, I_2, equals zero the current gain equals one which is the correct value.

IV. Simulation Results

DC simulation of the whole circuit is shown in Fig. 13, where I_2 is swept over the whole range from -8 μA to 8 μA giving an overall output dynamic range of about 50 dB.

AC simulation is given in Fig. 14 where I_2 is given maximum (8 μA), zero, and minmum (-8 μA) values. The figure shows that the bandwidth of the circuit is 1.6, 10, and 15.2 MHz for maximum, unity,

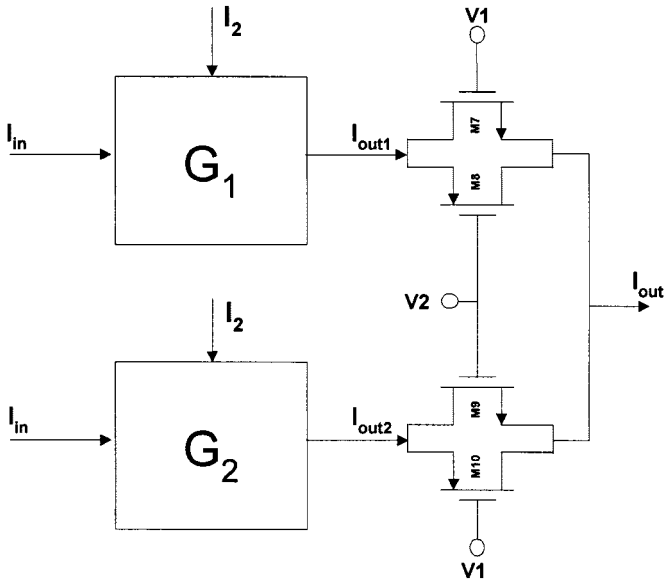

Fig. 11. Block diagram to realize G_3.

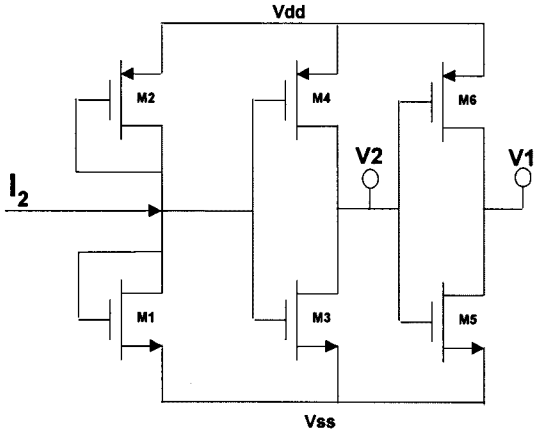

Fig. 12. Circuit used to generate the control voltages V_1 and V_2 to be used in the block diagram of Fig. 11.

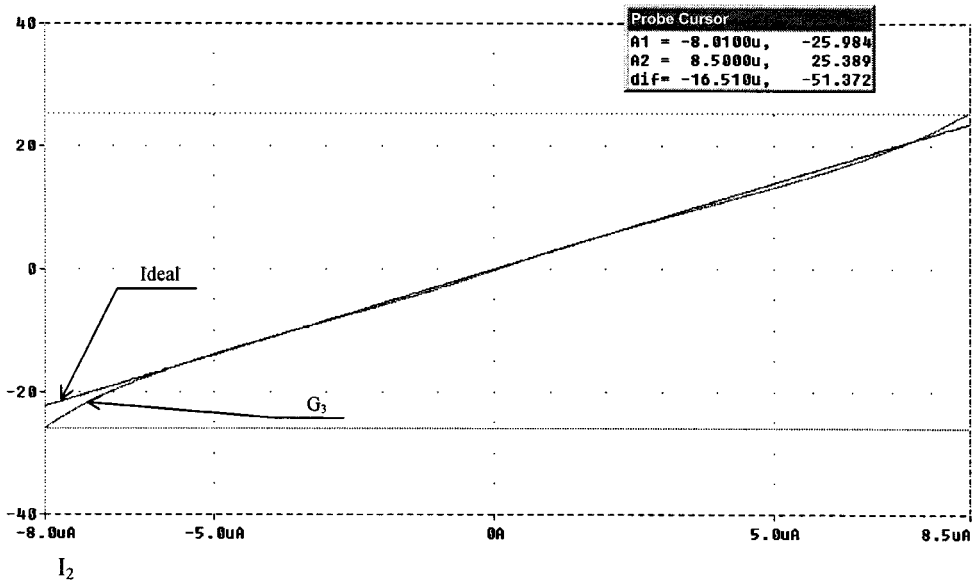

Fig. 13. Combined approximation function (G_3) and an ideal exponential function versus control signal I_2.

and minimum gain values, respectively. Transient analysis is shown in Fig. 15 where I_2 was chosen to be a ramp and $I_{\rm in}$ is a sinusoidal signal with frequency of 200 kHz and amplitude of 1 μA. The figure shows the variable gain effect on the output current.

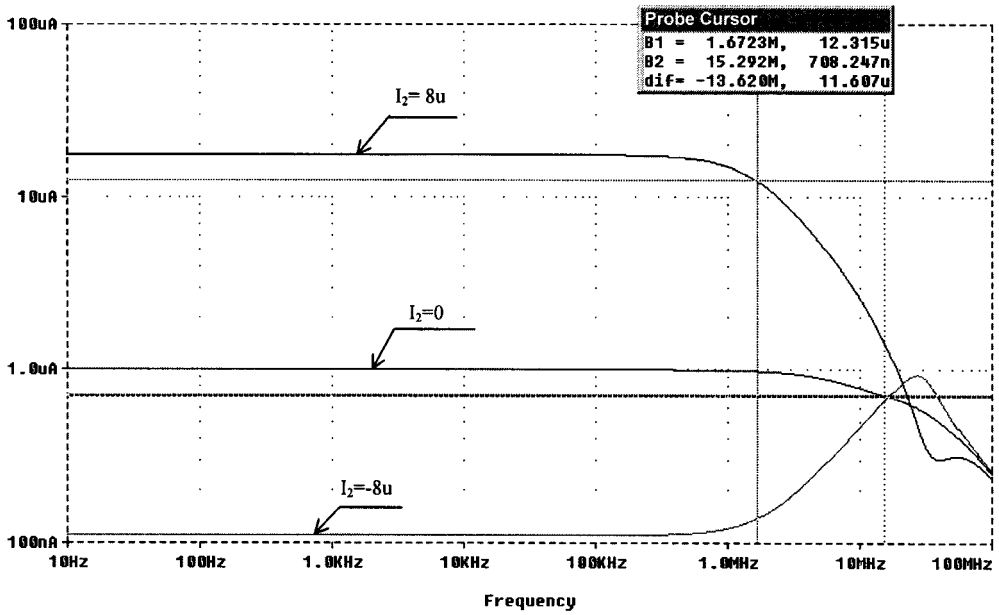

Fig. 14. Frequency response of the output current for three different gain values.

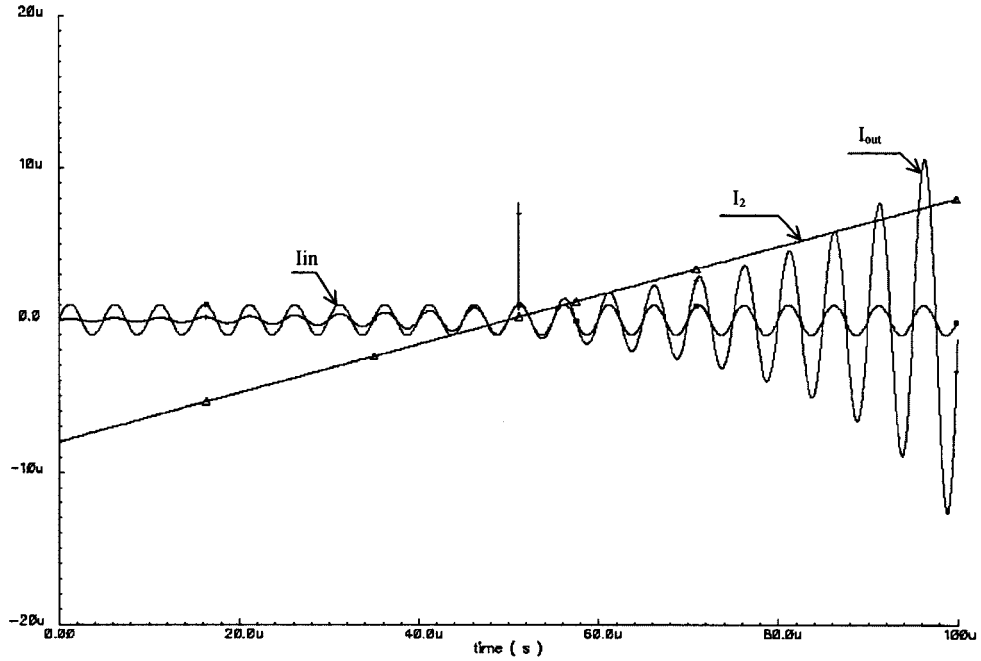

Fig. 15. Transient analysis of the overall circuit, Iin is a 200-kHz siusoidal signal and I_2 is a ramp. $I_{\rm out}$ is shown to have variable ampliude.

Reaction time of the circuit was simulated and found to be 240 ns when a step function with a rise time of 100 ns is applied to I_2, the step changes from $-2x$ μA to $-x$ μA, where x is a positive integer that takes the values 1, 2 or 4. Also the reaction time for similar ranges but with positive values of I_2 was found to be approximately 240 ns. However, the reaction time when I_2 changes from -1 μA to $+1$ μA is found to be 300 ns. This additional time is needed to switch off the first transmission gate and switch on the other one. (I_2 goes from the negative value to a positive one). Total harmonic distortion (THD) analysis was also performed using a 50-kHz sinusoidal input current and an output current of 0.5 μA and yielded -21 dB for maximum gain and -48 dB for minimum gain. The amount of distortion can be greatly reduced if a a fully differential scheme is used. The simulated input referred noise current has a maxium value of 120 pA/Hz$^{1/2}$.

V. Conclusion

A novel approximation function to realize the exponential relation found in almost all VGA circuits is developed. The function increases the dynamic range realized by the normal approximation function by more than 20 dB. As an application, a low-power current mode VGA is presented, consuming average power of less than 1.2 mW and having a bandwidth of 1.6 MHz at maximum positive gain.

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On the Jitter Requirements of the Sampling Clock for Analog-to-Digital Converters

Nicola Da Dalt, Moritz Harteneck, Christoph Sandner, and Andreas Wiesbauer

***Abstract*—In this brief, the effect of sampling clock jitter on the SNR of an analog-to-digital (AD) conversion is investigated from a practical perspective. Aperture jitter analyses have been dealing up to now with white spectrum jitter. This assumption does not hold for the output of phase-locked loops (PLL)-like frequency synthesizers, where the spectrum is shaped by the loop transfer function. Based on a linear approximation, a powerful expression for the SNR is derived, applicable to a jitter process with generic autocorrelation function and generic input signal. A lot of different definitions of jitter are available in the literature; this brief addresses also the problem of identifying correctly among them the "effective" jitter for a given SNR. This can be profitably used in the specification as well as verification of the jitter requirements of a frequency synthesizer used as sampling clock generator in the AD converter systems. The results have been checked through numerical simulation.**

***Index Terms*—ADC, jitter, sampling, SNR.**

I. Introduction

In modern mixed signal systems, there is an increasing demand of high performance analog-to-digital (AD) converters. In this field, high performance means primarily high resolution and high sampling frequency. One key factor to reach high performance is the availability of very low jitter sampling clocks (for the recent wide band applications, for instance, clocks with jitter in the order of few picoseconds are required). Indeed, it is known that the aperture jitter or phase noise [1]–[4] of the sampling clock represents a fundamental limitation to the maximum SNR reachable by a given sampling system.

In the available recent literature (see for instance [5], [6]), the jitter of the sampling clock is considered to be gaussian distributed and white (flat spectrum). This second assumption is, anyway, far away from reality. Indeed the spectral distribution of the phase noise of a phase-locked loop (PLL) frequency synthesizer is mainly shaped by the voltage-controlled oscillator (VCO) noise spectrum, by the phase noise spectrum of the input clock and by the transfer function of the control loop [1], [7], [8]. In this brief the effect of jitter with generic power-spectral density on the SNR of AD conversion is investigated and a general expression for the SNR is derived. The analysis is based on a linear approximation of the sampling process (also used in [5]), which holds if the amplitude of the jitter t_j is small compared to the inverse of the maximum frequency component of the sampled signal.

The intention of the brief is to focus on the effect of the sampling instant uncertainty on the SNR; therefore, the sampling process itself, apart from the sampling instant uncertainty, is considered ideal and we neglect the quantization noise in the calculation of the SNR [6]. It will be found that the SNR is determined by the second-time derivative of the input signal autocorrelation function and by the timing jitter autocorrelation function, both evaluated at zero.

Another important aspect of the subject is how to specify requirements on the jitter of the clocks used for AD conversions. In the available literature, there are a number of different jitter definitions (cycle, cycle-to-cycle, period, accumulated, absolute, long-term, and for each of those the rms, 3-sigma, peak, peak-to-peak value can be provided). Until now, there is no clear indication of which is the "correct" specification for AD applications. Three operative (measurable) definitions of jitter are used here, and it will be demonstrated that, as a consequence of the SNR expression derived in this brief, the correct specification to be given is the long-term jitter.

The brief is organized as follows. In Section II, the SNR expression is derived and applied to the case of sinusoidal input signals; in Section III, operative definitions of jitter are given and the correct way of specifying jitter for AD conversions is investigated; in Section IV the results are checked by numerical simulations.

II. SNR in the Linear Approximation

In what follows, T is the sampling period and the jitter t_j is considered as a time discrete random process with time step T, having zero mean and being independent from the analog time continuous input signal x. The former assumption is without loss of generality, the latter is well verified in most of the real systems.

The sampling process is illustrated in Fig. 1. Due to the presence of jitter t_j on the sampling clock, the instants of sampling are moved away from the ideal point. For instance, the kth sample will not be taken exactly at time kT, but at $kT + t_j(kT)$.

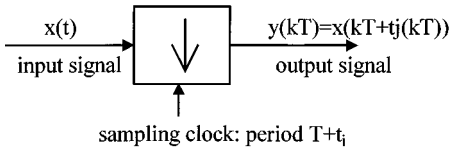

Fig. 1. Sampling process.

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