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SHORT PAPER

A Note on the Generation of Generalized Impedance Converter Circuits Using NAM Expansion

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Abstract The nodal admittance matrix (NAM) expansion is used to generate the voltage generalized impedance converter (VGIC) and the current generalized impedance converter (CGIC) with both A and D of the transmission matrix (T) being negative. Simulation results are included.

Keywords Voltage generalized impedance converter · Current generalized impedance converter · Current conveyors · Inverting current conveyors

1 Introduction

Most recently the NAM expansion method was used to generate a total of 16 pathological realizations for the VGIC [9] realizing Antoniou basic T matrix equation with positive A and D coefficients [1]. Based on the two alternatives pairing of the pathological elements a total of 32 VGIC circuits are obtained using CCII or ICCII or combination of both of them. One of the configurations obtained for the VGIC is suitable for inductance realization [6], and the other configuration is suitable for frequency dependent negative resistance (FDNR) realization.

At the same time the 16 inductor circuits have been generated from the generalized conveyor realization of the type 2b L-C mutator [8].

Similarly a total of 16 pathological realizations for the CGIC [4, 9] as defined by Antoniou with positive A and D coefficients [1] are generated using NAM expansion. Based on the two alternatives pairing of the pathological elements a total of 32 CGIC circuits are obtained using CCII or ICCII or combination of both of them. One of the configurations obtained for the CGIC is suitable for inductance realization, and

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the other configuration is suitable for FDNR realization. At the same time the 16 inductor circuits have been generated from the generalized conveyor realization of the type 2c L-C mutator [8]. In addition the VGIC and CGIC with both A and D of the T matrix being negative [7] have been considered by Swamy and an additional equal number of VGIC and CGIC circuits are derived and given in Table form [10]. This research note serves to complete very briefly the work published in [9] using NAM expansion to the VGIC and CGIC with both A and D of the T matrix being negative [7].

2 The VGIC with negative A and D

The VGIC is defined by the following transmission matrix:

$$Ta = \begin{bmatrix} -\frac{Y_2 Y_4}{Y_1 Y_3} & 0 \\ 0 & -1 \end{bmatrix} \tag{1}$$

The forward voltage gain is

$$A_V = \frac{V_2}{V_1} = -\frac{Y_1 Y_3}{Y_2 Y_4}$$

The reverse current gain is

$$A_I = -\frac{I_1}{I_2} = -1$$

Consider the admittance matrix type (i) given in [3] as follows:

$$Y = \begin{bmatrix} A_V A_I \infty_1 & -A_I \infty_1 \\ -A_V \infty_1 & \infty_1 \end{bmatrix} \tag{2}$$

The Y matrix in (2) can be expressed as

$$Y = \begin{bmatrix} -A_V \infty_1 & \infty_1 \\ -A_V \infty_1 & \infty_1 \end{bmatrix} \tag{3}$$

For $A_V = -\frac{N_V}{D_V}$ the Y matrix can be written as

$$Y = \begin{bmatrix} \frac{N_V}{D_V} \infty_1 & \infty_1 \\ \frac{N_V}{D_V} \infty_1 & \infty_1 \end{bmatrix} \tag{4}$$

Four alternative classes of the VGIC are defined next.

2.1 Classes I-a and II-a VGIC

Applying pivotal expansion operation given in [3] on (4) the following NAM is obtained:

$$Y = \begin{bmatrix} 0 & \infty_1 & -\infty_1 \\ 0 & \infty_1 & -\infty_1 \\ N_V & 0 & D_V \end{bmatrix} \tag{5}$$

The intrinsic infinity parameters in the above matrix are realized using a nullator between nodes 2 and 3 and a current mirror (CM) between nodes 1 and 2. Taking N_V as Y_1Y_3/Y_2 and D_V as Y_4 the NAM equation becomes

$$Y = \begin{bmatrix} 0 & \infty_1 & -\infty_1 \\ 0 & \infty_1 & -\infty_1 \\ \frac{Y_1Y_3}{Y_2} & 0 & Y_4 \end{bmatrix} \tag{6}$$

Adding a blank fourth row and column to (6) the above NAM stamp can be expanded in two alternative ways resulting in two different classes of VGIC circuits as explained next.

2.1.1 Class I-a VGIC

Four alternative VGIC circuits are generated based on the following NAM equation obtained from (6) using pivotal expansion operation [3].

$$Y = \begin{bmatrix} 0 & \infty_1 & -\infty_1 & 0 \\ 0 & \infty_1 & -\infty_1 & 0 \\ 0 & 0 & Y_4 & -Y_1 \\ Y_3 & 0 & 0 & Y_2 \end{bmatrix} \tag{7}$$

The above NAM equation can be further expanded to a 6×6 NAM equation with Y_1 and Y_3 to be located in diagonal positions to be realizable by grounded admittances as shown in Fig. 1. The two alternative realizations of Fig. 1 using two CCII+ and one CCII− are shown in Figs. 2(a) and 2(b).

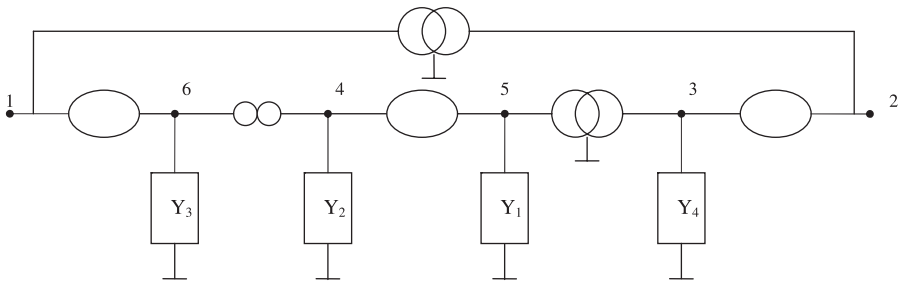

Fig. 1 Pathological realization 1 of class I-a VGIC using CM between nodes 1 and 2

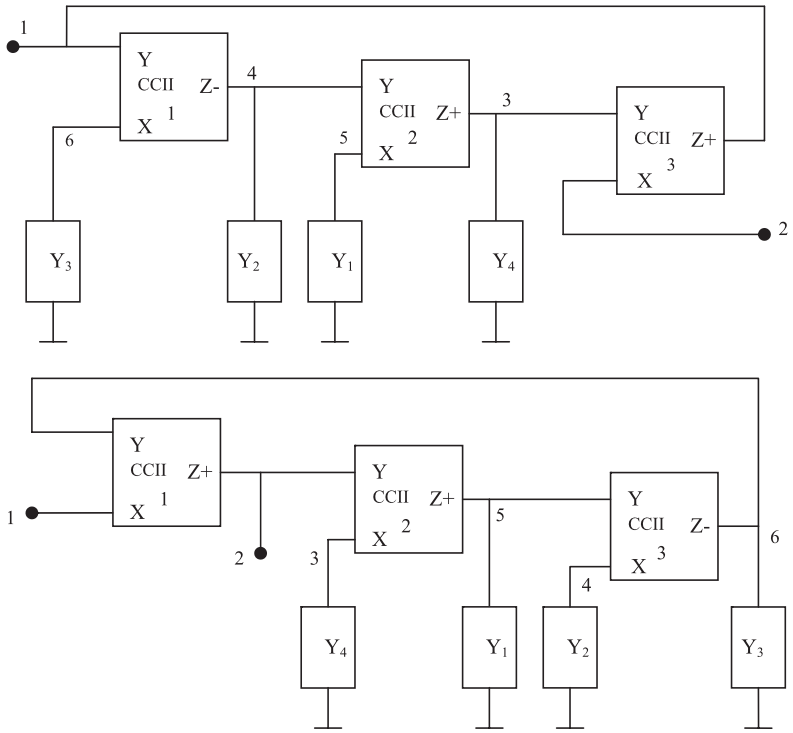

Fig. 2 (**a**) Realization 1 of the VGIC of Fig. 1. (**b**) Realization 2 of the VGIC of Fig. 1

2.1.2 Class II-a VGIC

In this class four alternative VGIC circuits are generated based on the following NAM equation obtained from (6) using pivotal expansion operation [2] as follows:

$$Y = \begin{bmatrix} 0 & \infty_1 & -\infty_1 & 0 \\ 0 & \infty_1 & -\infty_1 & 0 \\ 0 & 0 & Y_4 & Y_1 \\ -Y_3 & 0 & 0 & Y_2 \end{bmatrix} \tag{8}$$

Similarly classes III-a as well as IV-a can be obtained and are summarized in Table 1.

3 The CGIC with Negative *A* and *D*

The CGIC is defined by the following transmission matrix:

$$Ta = \begin{bmatrix} -1 & 0 \\ 0 & -\frac{Y_1 Y_3}{Y_2 Y_4} \end{bmatrix} \tag{9}$$

$$A_V = \frac{V_2}{V_1} = -1, \qquad A_I = -\frac{I_1}{I_2} = -\frac{Y_1 Y_3}{Y_2 Y_4}.$$

Table 1 The Y matrix of the additional four classes of the VGIC

VGIC	4×4 $[Y]$ matrix
Class I-a	$\begin{bmatrix} 0 & \infty_1 & -\infty_1 & 0 \\ 0 & \infty_1 & -\infty_1 & 0 \\ 0 & 0 & Y_4 & -Y_1 \\ Y_3 & 0 & 0 & Y_2 \end{bmatrix}$
Class II-a	$\begin{bmatrix} 0 & \infty_1 & -\infty_1 & 0 \\ 0 & \infty_1 & -\infty_1 & 0 \\ 0 & 0 & Y_4 & Y_1 \\ -Y_3 & 0 & 0 & Y_2 \end{bmatrix}$
Class III-a	$\begin{bmatrix} 0 & \infty_1 & \infty_1 & 0 \\ 0 & \infty_1 & \infty_1 & 0 \\ 0 & 0 & Y_4 & Y_1 \\ Y_3 & 0 & 0 & Y_2 \end{bmatrix}$
Class IV-a	$\begin{bmatrix} 0 & \infty_1 & \infty_1 & 0 \\ 0 & \infty_1 & \infty_1 & 0 \\ 0 & 0 & Y_4 & -Y_1 \\ -Y_3 & 0 & 0 & Y_2 \end{bmatrix}$

The Y matrix of the CGIC can be represented by the admittance matrix type (i) given in Table IV of [3] as follows:

$$Y = \begin{bmatrix} -A_I \infty_1 & -A_I \infty_1 \\ \infty_1 & \infty_1 \end{bmatrix} \tag{10}$$

For $A_I = -\frac{N_I}{D_I}$, the Y matrix can be written as

$$Y = \begin{bmatrix} \frac{N_I}{D_I} \infty_1 & \frac{N_I}{D_I} \infty_1 \\ \infty_1 & \infty_1 \end{bmatrix} \tag{11}$$

Four alternative classes of the CGIC are defined in the following sections. Each class includes four pathological realizations as given next.

3.1 Classes I-a and II-a CGIC

Applying pivotal expansion operation given in [3] on (11) the following NAM equation is obtained:

$$Y = \begin{bmatrix} 0 & 0 & N_I \\ \infty_1 & \infty_1 & 0 \\ -\infty_1 & -\infty_1 & D_I \end{bmatrix} \tag{12}$$

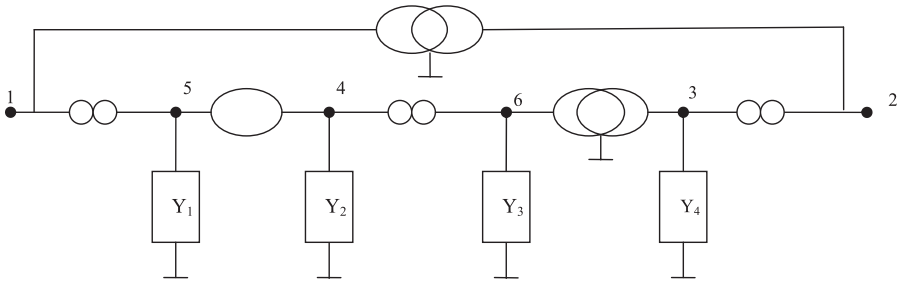

Fig. 3 Pathological realization 1 of class I-a CGIC using VM between nodes 1 and 2

The intrinsic infinity parameters are realized using a voltage mirror (VM) between nodes 1 and 2 and a norator between nodes 2 and 3.

Taking N_I as Y_1Y_3/Y_2 and D_I as Y_4 the above NAM equation becomes

$$Y = \begin{bmatrix} 0 & 0 & \frac{Y_1Y_3}{Y_2} \\ \infty_1 & \infty_1 & 0 \\ -\infty_1 & -\infty_1 & Y_4 \end{bmatrix} \tag{13}$$

Adding a blank fourth row and column to (13) the NAM stamp can be expanded in two alternative ways resulting in two different classes of CGIC circuits as explained next.

3.1.1 Class I-a CGIC

Four alternative CGIC circuits are generated based on the following NAM equation obtained from (13) using pivotal expansion operation.

$$Y = \begin{bmatrix} 0 & 0 & 0 & Y_1 \\ \infty_1 & \infty_1 & 0 & 0 \\ -\infty_1 & -\infty_1 & Y_4 & 0 \\ 0 & 0 & -Y_3 & Y_2 \end{bmatrix} \tag{14}$$

The above NAM equation can be further expanded to a 6×6 NAM equation with Y_1 and Y_3 to be located in diagonal positions to be realizable by grounded admittances as shown in Fig. 3. The two alternative realizations of Fig. 3 using two ICCII− and one CCII− are shown in Figs. 4(a) and 4(b).

A second pathological realization of the class I-a CGIC can be derived by NAM expansion and is shown in Fig. 5. The two alternative realizations of Fig. 5 using ICCII−, CCII+ and CCII− are shown in Figs. 6(a) and 6(b).

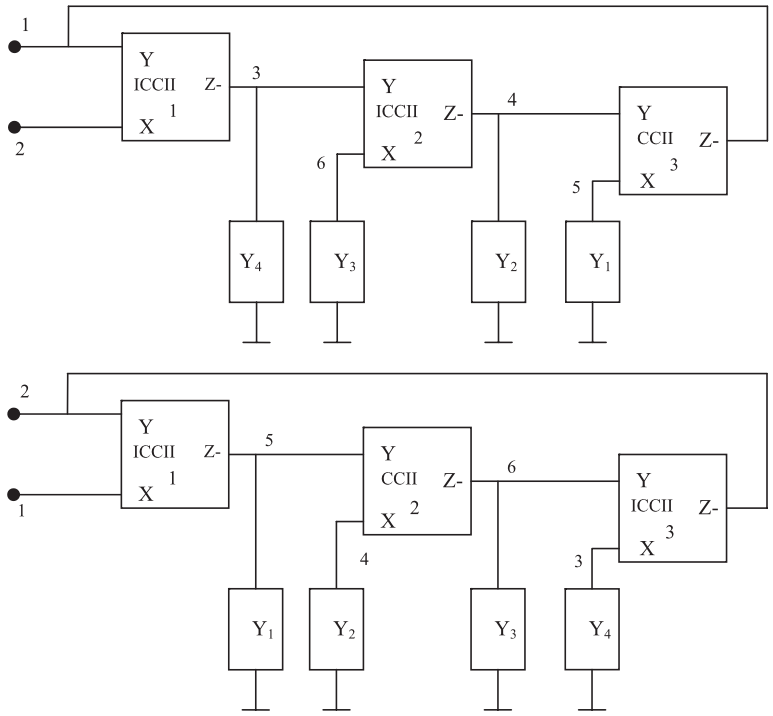

Fig. 4 (**a**) Realization 1 of the CGIC of Fig. 3. (**b**) Realization 2 of the CGIC of Fig. 3

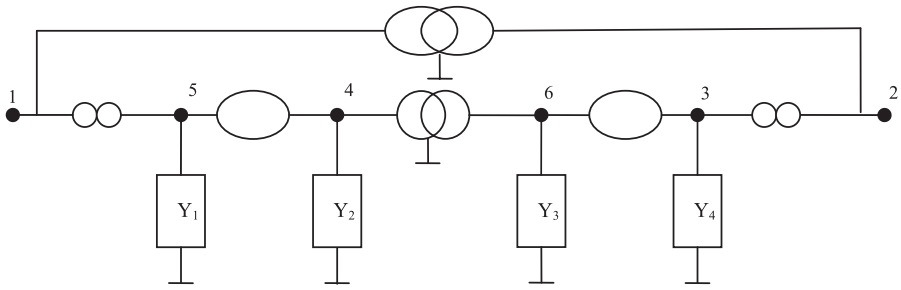

Fig. 5 Pathological realization 2 of class I-a CGIC using VM between nodes 1 and 2

3.1.2 Class II-a CGIC

Four alternative CGIC circuits are generated based on the following NAM equation obtained from (13) using pivotal expansion operation.

$$Y = \begin{bmatrix} 0 & 0 & 0 & -Y_1 \\ \infty_1 & \infty_1 & 0 & 0 \\ -\infty_1 & -\infty_1 & Y_4 & 0 \\ 0 & 0 & Y_3 & Y_2 \end{bmatrix} \tag{15}$$

Table 2 The Y matrix of the additional four classes of the CGIC

CGIC	4×4 $[Y]$ matrix
Class I-a	$\begin{bmatrix} 0 & 0 & 0 & Y_1 \\ \infty_1 & \infty_1 & 0 & 0 \\ -\infty_1 & -\infty_1 & Y_4 & 0 \\ 0 & 0 & -Y_3 & Y_2 \end{bmatrix}$
Class II-a	$\begin{bmatrix} 0 & 0 & 0 & -Y_1 \\ \infty_1 & \infty_1 & 0 & 0 \\ -\infty_1 & -\infty_1 & Y_4 & 0 \\ 0 & 0 & Y_3 & Y_2 \end{bmatrix}$
Class III-a	$\begin{bmatrix} 0 & 0 & 0 & Y_1 \\ \infty_1 & \infty_1 & 0 & 0 \\ \infty_1 & \infty_1 & Y_4 & 0 \\ 0 & 0 & Y_3 & Y_2 \end{bmatrix}$
Class IV-a	$\begin{bmatrix} 0 & 0 & 0 & -Y_1 \\ \infty_1 & \infty_1 & 0 & 0 \\ \infty_1 & \infty_1 & Y_4 & 0 \\ 0 & 0 & -Y_3 & Y_2 \end{bmatrix}$

Similarly classes III-a as well as IV-a can be obtained and are summarized in Table 2.

4 Simulation Results

To demonstrate the practicality of the VGIC and the CGIC two examples are considered next.

In the first example a second-order high-pass filter having f_O of 1 MHz and $Q = 0.707$ is designed using a capacitor of 100 pF in series with $R = 2.25$ kΩ and an active inductor of 0.253 mH. The active inductor is realized using the VGIC of Fig. 2(a) with a capacitor C of 100 pF at node 3 and four equal resistors each of 1.59 kΩ is connected to each of the other four nodes 2, 4, 5 and 6.

Spice simulation is carried out using the CMOS circuit of the differential voltage current conveyor (DVCC) in [2] shown in Fig. 7 and with aspect ratios as given in Table 3 based on the 0.5 μm CMOS model from MOSIS. The supply voltages used are $V_{DD} = 1.5$ V, $V_{SS} = -1.5$ V, $V_{B1} = -0.52$ V and $V_{B2} = 0.32$ V.

Three DVCC are used to realize the CCII− and the two CCII+; in the circuit of Fig. 2(a).

Figure 8(a) represents the magnitude and phase responses of the high-pass filter with the output taken from node 1 in Fig. 2(a). The total power dissipation in the

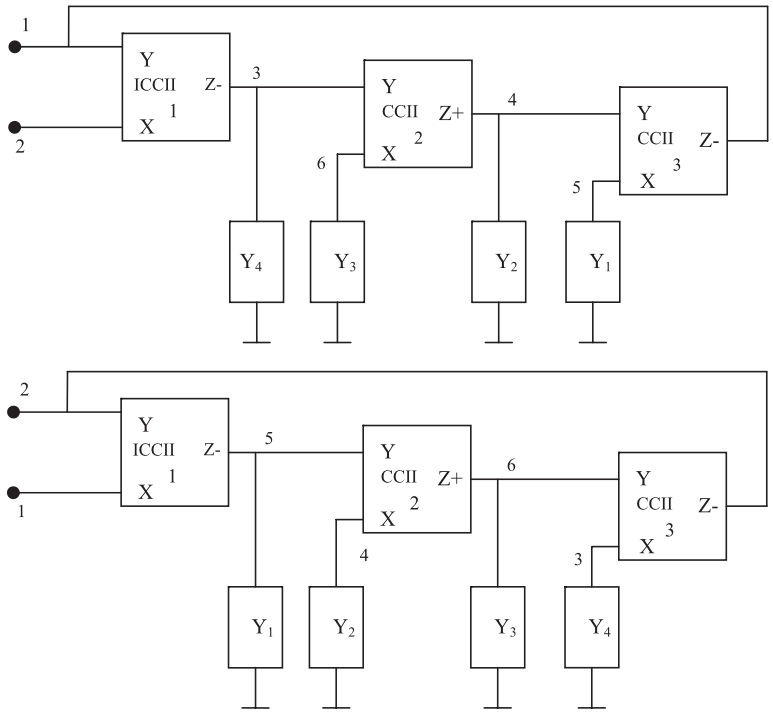

Fig. 6 (**a**) Realization 1 of the CGIC of Fig. 5. (**b**) Realization 2 of the CGIC of Fig. 5

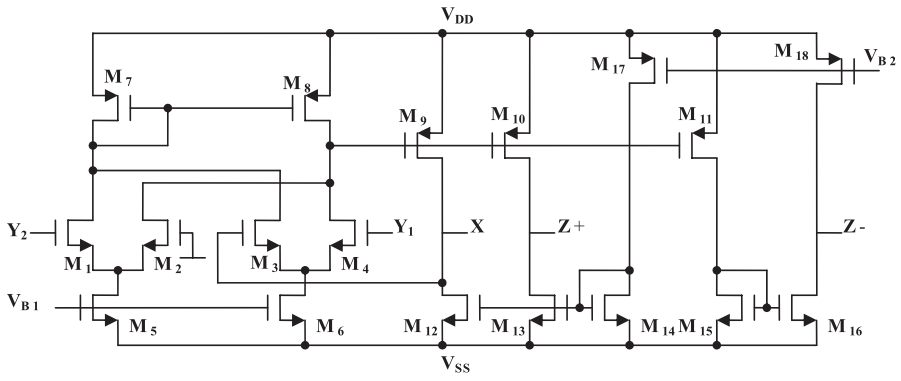

Fig. 7 CMOS circuit realizing DVCC [2]

circuit is 3.03551 mW. The deviation from the ideal response is mainly due to the parasitic capacitor C_{Z1} acts in parallel with the resistor connected to node 4. On the other hand the capacitor C connected at node 3 can absorb the parasitic capacitor C_{Z2} by subtracting its value from the design value of C.

Table 3 Transistor aspect ratios of the CMOS circuit shown in Fig. 7

MOS transistors	W (μm)/L (μm)
M_1, M_2, M_3, M_4	4/1
M_5, M_6	8/1
M_{12}, M_{13}, M_{14}, M_{15}, M_{16}	20/2.5
M_7, M_8	10/1
M_9, M_{10}, M_{11}, M_{17}, M_{18}	40/2

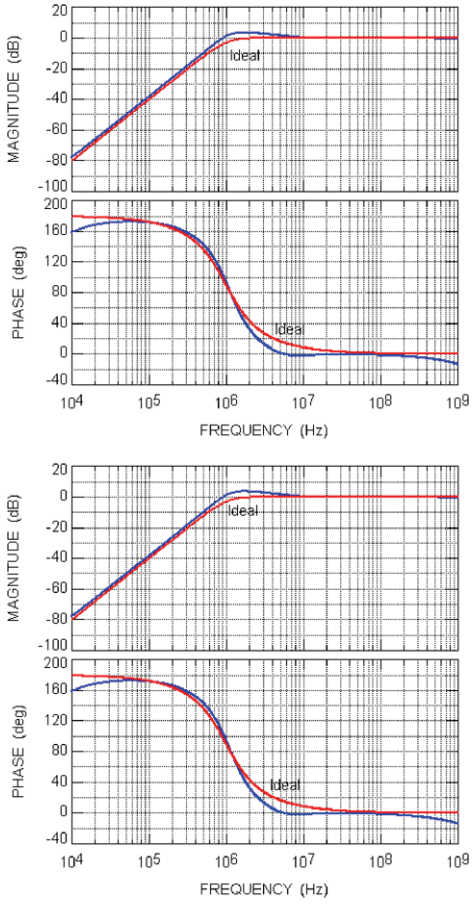

Fig. 8 (**a**) Simulated magnitude and phase responses of a high-pass filter realized using VGIC of Fig. 2(a). (**b**) Simulated magnitude and phase responses of a high-pass filter realized using CGIC of Fig. 6(a)

In the second example the same second-order high-pass filter is realized using the CGIC of Fig. 6(a) to realize the active inductor using a capacitor C of 100 pF at node 4 and all other four branches at nodes 2, 3, 5 and 6 as equal resistors of 1.59 kΩ.

Three DVCC are used to realize the ICCII−, CCII+ and CCII−; realizing the CGIC shown in Fig. 6(a).

Figure 8(b) represents the magnitude and phase responses of the high-pass filter with the output taken from node 1. The total power dissipation in the circuit is 3.01848 mW. The deviation from the ideal response is mainly due to the parasitic capacitor C_{Z1} acts in parallel with the resistor connected to node 3. On the other hand the capacitor C connected at node 4 can absorb the parasitic capacitor C_{Z2} by subtracting its value from the design value of C.

5 Conclusions

This research note completes the work in [9] by considering the additional types of the VGIC and CGIC defined with negative A and D coefficients of the T matrix [7]. The 4×4 expanded Y matrices are summarized in Tables 1 and 2. The importance of pathological realization in active circuit modeling has been recently demonstrated in [5]. Simulation results demonstrating the practicality of the generated VGIC and CGIC circuits are included.

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