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A new family of highly linear CMOS transconductors based on the current tail differential pair

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Abstract

A new family of linear differential transconductors based on the current tail differential pair is presented. The proposed transconductor employs MOS transistors operating in the saturation region. It is shown that the proposed transconductors offer superior linearity and wider range in addition to the simplicity and high frequency response, which characterizes the current tail differential pair transconductor. PSpice simulation results are given.

Keywords: CMOS transconductors; Differential pair

1. Introduction

Linear transconductor circuits are useful building blocks in analog signal processing [1–7]. Based on the transconductor elements, Gm-C filters and basic simple analog building blocks such as multipliers, programmable gain amplifiers, oscillators, and other nonlinear circuits can be built. Several MOS transconductors for voltage-controlled filter circuits were reported [8–11]. Nedungadi and Viswanathan [5] describe a compensated common source pair. Viswanathan [6] proposed a cross-coupled structure. Other authors have adopted similar strategies but with different implementations [8].

In this paper, the analysis of the current tail differential pair transconductor, also known as the Long Tail Differential Pair (LTP) is first presented. A family of transconductors using MOS transistors operating in the saturation region is proposed and their performance is investigated. The principle of operation and the analysis of the proposed transconductors are presented. A new voltage-controlled transconductor as well as a new multiplier divider circuit are also presented. Finally, a low voltage rail-to-rail transconductor circuit is presented.

P Spice simulations are included based on using the 0.7 micrometer CMOS technology (see Table 1).

2. Transconductor circuits' description

2.1. Long tail differential pair (LTP)

The differential pair transconductor forms a useful benchmark owing to its simplicity and its high frequency response [3,4]. However, the nonlinearity generated by the constant current operation always restricts the scope of this structure.

Consider the matched differential pair shown in Fig. 1. All the transistors used are operating in the saturation region, where the drain current of the NMOS transistor operating in that region (neglecting the channel length modulation effect) is given by:

$$I = \frac{K_n}{2}(V_{GS} - V_T)^2, \tag{1}$$

$$K_n = (\mu_n C_{ox})\left(\frac{W}{L}\right) \tag{2}$$

where V_T is the threshold voltage, K_n is the transconductance parameter, μ_n is the effective carrier mobility, C_{ox} is the gate oxide capacitance per unit area, W is the channel width and L is the channel length.

Assuming that all body terminals are connected to the proper supply voltages. The currents I_1 and I_2 of Fig. 1 are given by:

$$I_1 = \frac{K_n}{2}(V_1 - V_S - V_T)^2, \tag{3}$$

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Table 1
Model parameters set of 0.7 μm CMOS Technology (obtained through MIETIC)

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MODEL MODN NMOS LEVEL = 3
+ TOX = 17E-9 XJ = 0.1U NFS = 1.2E11 VTO = 0.75 NSUB = 7.0E16
+ DELTA = 0.85 UO = 470 THETA = 0.08 RSH = 520 KAPPA = 0.001
+ ETA = 0.0052 VMAX = 1.94E5 LD = 0.1U DELL = 0.2U WD = 0.05U
+ JS = IE-3 CJ = 5.0E-4 MJ = 0.32 CJSW = 2.8E-10 MJSW = 0.23
+ PB = 0.86 FC = 0.5 CGSO = 3.1E-10 CGDO = 3.1E-10 + KF = 3E-28 AF = 1

MODEL MODP PMOS LEVEL = 3
+ TOX = 17E-9 XJ = 0.05U NFS = 0.5E11 VTO = -0.95 NSUB = 3.5E16
+ DELTA = 0.8 UO = 158 THETA = 0.135 RSH = 870 KAPPA = 0.001
+ ETA = 0.03 VMAX = 7.2E5 LD = 0.06U DELL = 0.15U WD = 0.1U
+ JS = 1E-3 CJ = 6E-4 MJ = 0.51 CJSW = 3.6E-10 MJSW = 0.35
+ PB = 0.90 FC = 0.5 CGSO = 2.2E-10 CGDO = 2.2E-10 KF = 5E-30 AF = 1
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$$I_2 = \frac{K_n}{2}(V_2 - V_S - V_T)^2. \tag{4}$$

The current I_{SS} is given by:

$$I_{SS} = \frac{K_n}{2}(V_1 - V_S - V_T)^2 + \frac{K_n}{2}(V_2 - V_S - V_T)^2 \tag{5}$$

and the output current is given by:

$$I_{OUT} = I_1 - I_2 = \frac{K_n}{2}(V_1 - V_2)(V_1 + V_2 - 2(V_S + V_T)). \tag{6}$$

The output current as a function of the two input voltages V_1 and V_2 is obtained as:

$$I_{OUT} = \sqrt{K_n I_{SS}}(V_1 - V_2)\sqrt{1 - \frac{K_n(V_1 - V_2)^2}{4I_{SS}}}. \tag{7}$$

The output characteristics can be made linear by having either a small input voltage, or a relatively large current I_{SS}. Alternatively, choosing a small K_n, this means the input devices are long and narrow. The differential input voltage $V_i = V_1 - V_2$ is limited to the range:

$$-\sqrt{\frac{2I_{SS}}{K_n}} \le V_i \le \sqrt{\frac{2I_{SS}}{K_n}}. \tag{8}$$

From Eqs. (7) and (8), it is seen that the linearity range of the transconductor increases as the ratio (I_{SS}/K_n) increases. One major problem is the effect on the common mode input voltage, which limits the operating range of the circuit. Setting $V_1 = V_2 = V_{CM}$, the current in each of the differential pair branches is given by:

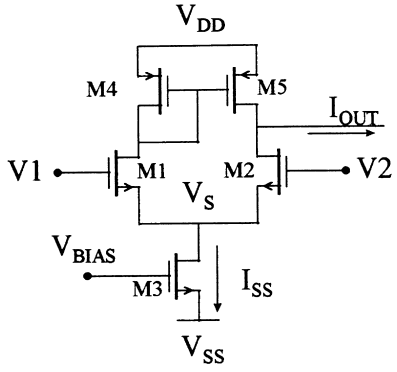


Fig. 1. The LTP CMOS transconductor.

$$\frac{K_n}{2}(V_{CM} - V_S - V_T)^2 = \frac{1}{2}I_{SS}, \tag{9}$$

$$V_{CM,min} = V_{S,min} + V_T + \sqrt{\frac{I_{SS}}{K_n}}. \tag{10}$$

For the LTP to operate properly;

$$V_{S,min} + V_T \ge V_{BIAS}. \tag{11}$$

Hence;

$$V_{CM} \ge V_{BIAS} + \sqrt{\frac{I_{SS}}{K_n}}. \tag{12}$$

From Eq. (12), it is seen that as the ratio (I_{SS}/K_n) increases V_{CM} increases, hence the common mode region of operation decreases. The compromise between the degree of linearity and the range of operation limits the performance of the transconductor. Although this transconductor implementation has many advantages mainly; its simplicity, small number of transistors required, good high frequency response and high Common Mode Rejection Ratio (CMRR); its relatively poor range of linearity makes it unsuitable for many applications.

2.2. Extended long tail differential pair (ELTP)

The main idea is to try to extend the linear region of the simple differential pair resulting in transconductors with higher linearity and wider input voltage differential mode range.

2.2.1. The two stage ELTP

The proposed transconductor is mainly based on the usage of two simple differential pairs as shown in Fig. 2. The difference between the two input voltages is divided equally over two matched differential pairs.

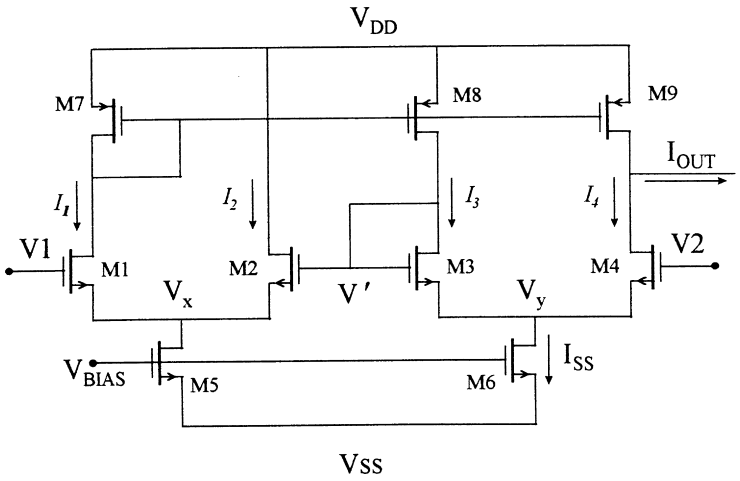


Fig. 2. The two stage ELTP CMOS transconductor.

Consider the matched differential pair shown in Fig. 2. The currents I_1, I_2, I_3 and I_4 are related by:

$$I_1 + I_2 = I_{SS}, \tag{13}$$

$$I_3 + I_4 = I_{SS}. \tag{14}$$

By mirror action of transistors M7 and M8 therefore:

$$I_1 = I_3. \tag{15}$$

From Eqs. (13)–(15), therefore:

$$I_2 = I_4. \tag{16}$$

As the sources of M1 and M2 are connected to each other, and so are the sources of M3 and M4, therefore:

$$V_{T1} = V_{T2}, \tag{17}$$

$$V_{T3} = V_{T4}. \tag{18}$$

Substituting for currents I_1, I_2, I_3 and I_4 in Eqs. (15) and (16), thus:

$$\frac{K_n}{2}(V_1 - V_x - V_{T1})^2 = \frac{K_n}{2}(V' - V_y - V_{T3})^2 \tag{19}$$

and

$$\frac{K_n}{2}(V' - V_x - V_{T2})^2 = \frac{K_n}{2}(V_2 - V_y - V_{T4})^2. \tag{20}$$

By solving Eqs. (19) and (20) together, one obtains:

$$V' = \frac{V_1 + V_2}{2} \tag{21}$$

where V' is the gate voltage of M2 and M3 as shown in Fig. 2.

The output current is the given by:

$$I_{OUT} = \sqrt{K_n I_{SS}}(V' - V_2)\sqrt{1 - \frac{K_n(V' - V_2)^2}{4I_{SS}}}. \tag{22}$$

Substituting for V' from Eq. (21) in Eq. (22), one

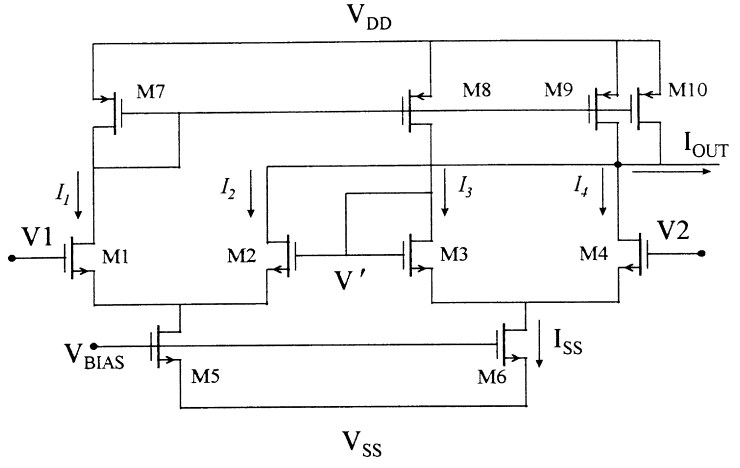


Fig. 3. The normalized two stage ELTP CMOS transconductor.

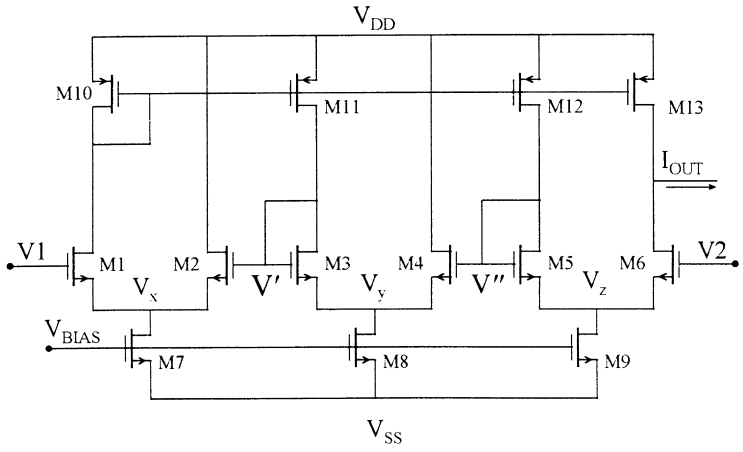


Fig. 4. The three stage ELTP CMOS transconductor.

obtains:

$$I_{OUT} = \frac{1}{2}\sqrt{K_n I_{SS}}(V_1 - V_2)\sqrt{1 - \frac{K_n(V_1 - V_2)^2}{16 I_{SS}}}. \quad (23)$$

Comparing the expressions in Eqs. (7) and (23), it is seen that the circuit of Fig. 2 has resulted in an output current with half the transconductance value but with a lower nonlinearity term by having the term $(4I_{SS})$ replaced by $(16I_{SS})$ and hence, the linearity is increased. Moreover, the operating range of the differential input voltage has increased to the following:

$$-2\sqrt{\frac{2I_{SS}}{K_n}} \le V_i \le 2\sqrt{\frac{2I_{SS}}{K_n}}. \quad (24)$$

Hence, for the same I_{SS} and K, the ELTP has wider linearity range than the LTP. It is noted that by using the ELTP the same linearity range for the differential input voltage as the LTP can be obtained but with less I_{SS}, hence the operating region for the common mode signal is increased.

In order to obtain the same transconductance value as the LTP (for the same I_{SS} and K_n), the circuit of Fig. 2 can be modified as shown in Fig. 3, where M9 and M10 are matched. The output current in this case is given by:

$$I_{OUT} = \sqrt{K_n I_{SS}}(V_1 - V_2)\sqrt{1 - \frac{K_n(V_1 - V_2)^2}{16 I_{SS}}}. \quad (25)$$

Thus, better linearity and wider range are obtained without the need for limiting the operating range.

2.2.2. The three stage ELTP

By cascading differential pairs as shown in Fig. 4, the factor of $(16I_{SS})$ can be increased significantly to obtain more linearity and wider range.

In a way similar to that used in Section 2.2.1, it can be proven that:

$$V' = V_1 - \frac{(V_1 - V_2)}{3}, \quad (26)$$

$$V'' = V_2 + \frac{(V_1 - V_2)}{3} \quad (27)$$

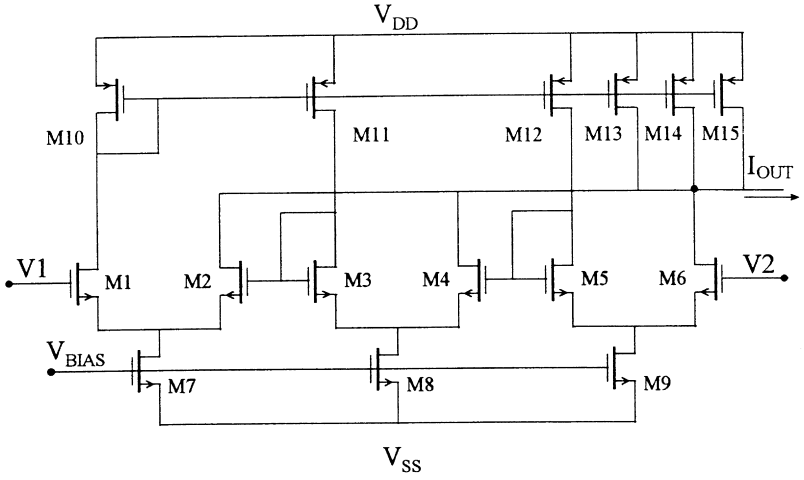


Fig. 5. The normalized three stage ELTP CMOS transconductor.

Table 2
The aspect ratios of the transistors used in Fig. 1

Transistor	Aspect ratio
M1, M2	14/1.4
M3, M4, M5	49/2.8

Where V' and V'' are as shown in Fig. 4. Hence:

$$I_{OUT} = \frac{1}{3}\sqrt{K_n I_{SS}}(V_1 - V_2)\sqrt{1 - \frac{K_n(V_1 - V_2)^2}{36 I_{SS}}}. \quad (28)$$

The circuit in Fig. 4 can be modified as shown in Fig. 5, where the transistors M13, M14 and M15 are matched, to obtain the same transconductance value as in the LTP for the same aspect ratios of the NMOS transistors. The output current in this case is given by:

$$I_{OUT} = \sqrt{K_n I_{SS}}(V_1 - V_2)\sqrt{1 - \frac{K_n(V_1 - V_2)^2}{36 I_{SS}}} \quad (29)$$

and the operating range for the differential input voltage then becomes:

$$-3\sqrt{\frac{2I_{SS}}{K_n}} \le V_i \le 3\sqrt{\frac{2I_{SS}}{K_n}}. \quad (30)$$

PSpice simulation results for the LTP versus the ELTP of two stages and three stages were carried out with the transistor aspect ratios as given in Tables 2, 3 and 4 respectively and ±2.5 V supply voltages.

Fig. 6 represents the *I–V* characteristics of the three transconductors shown in Figs. 1, 2 and 4. Fig. 7 represents the *I–V* characteristics of the three transconductors after the modification to obtain the same transconductance value (Figs. 1, 3 and 5). *V*1 was scanned from −2.5 to 2.5 V keeping *V*2 at 0 V. The THD was less than 0.18% at 100 kHz for 0.5 V peak to peak sinusoidal input.

3. Balanced output transconductance amplifier (BOTA)

The BOTA is an analog building block, which has many applications in the field of analog signal processing specially in the area of filter design [9]. A new BOTA, shown in Fig. 8, can be obtained by modifying the circuit of Fig. 2. The current flowing in the transistor is used to obtain the opposite replica of the output current I_{OUT}. One advantage of this circuit is the fact that there are two replicas of each current, which makes it convenient for the design of a BOTA without the need of adding more transistors.

Table 3
The aspect ratios of the transistors used in Fig. 2

Transistor	Aspect ratio
M1–M4	14/1.4
M5–M9	49/2.8

Table 4
The aspect ratios of the transistors used in Fig. 4

Transistor	Aspect ratio
M1–M6	14/1.4
M7–M13	49/2.8

PSpice simulation results for the BOTA were carried out with the same transistor aspect ratios as given before and with ±2.5 V supply voltages.

Fig. 9 represents the *I–V* characteristics of the BOTA. *V*1 is scanned from −1 to 1 V keeping *V*2 at 0 V.

4. Voltage-controlled balanced output transconductor

The circuit shown in Fig. 10(a) which was introduced in [1], is a folded CMOS *Gilbert's cell* [2]. This circuit can be considered as the voltage-controlled version of the LTP. This was achieved using two NMOS matched differential pairs as well as another PMOS differential pair onto which the control voltages are applied.

From Fig. 10(b) the output current of the circuit is given by:

$$I_{OUT} = (I_1 + I_3) - (I_2 + I_4). \quad (31)$$

The given circuit consists of two LTP transconductors with different current tails I_{SS1} and I_{SS2} as shown in Fig. 10(c). The output current is given by:

$$I_{OUT} = (I_1 - I_2) + (I_3 - I_4). \quad (32)$$

Neglecting the nonlinearity term in Eq. (7), one obtains:

$$I_{OUT} = \sqrt{K_n}(\sqrt{I_{SS1}} - \sqrt{I_{SS2}})(V_1 - V_2). \quad (33)$$

From Fig. 10(b), one obtains:

$$I_{BIAS} - I_5 = I_{SS1}, \quad (34)$$

$$I_{BIAS} - I_6 = I_{SS2}, \quad (35)$$

$$I_5 + I_6 = I_{BIAS}. \quad (36)$$

Solving Eqs. (34)–(36), one obtains:

$$I_{SS1} = I_6, \quad (37)$$

$$I_{SS2} = I_5. \quad (38)$$

Therefore:

$$\left(\sqrt{I_{SS1}} - \sqrt{I_{SS2}}\right) = \left(\sqrt{I_6} - \sqrt{I_5}\right)$$

$$= \sqrt{\frac{K_p}{2}}((V_X - V_4) - (V_X - V_3)), \quad (39)$$

$$\left(\sqrt{I_{SS1}} - \sqrt{I_{SS2}}\right) = \sqrt{\frac{K_p}{2}}(V_3 - V_4). \quad (40)$$

Hence substituting in Eq. (33), the output current is then

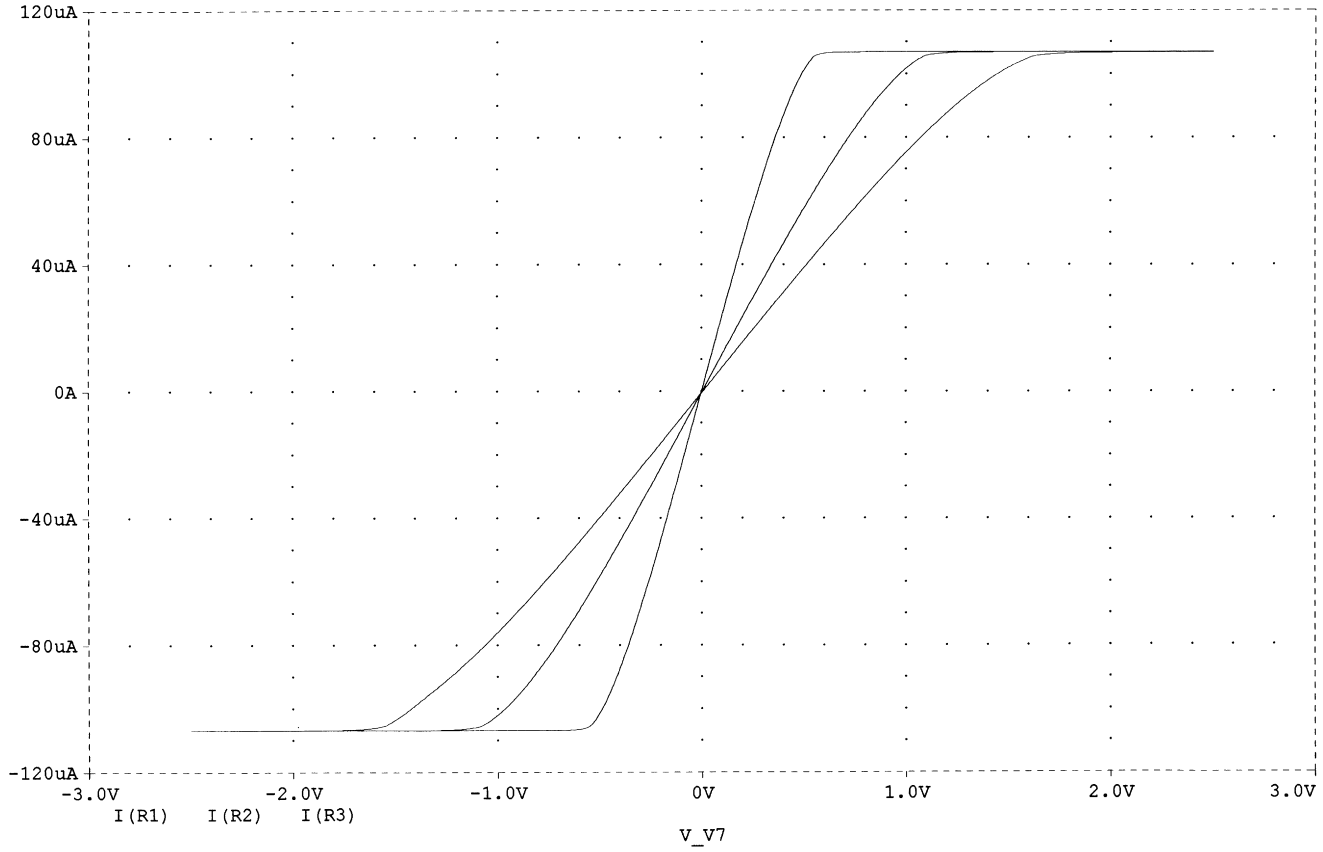


Fig. 6. The *I–V* characteristics of the ELTP of two and three stages versus the LTP.

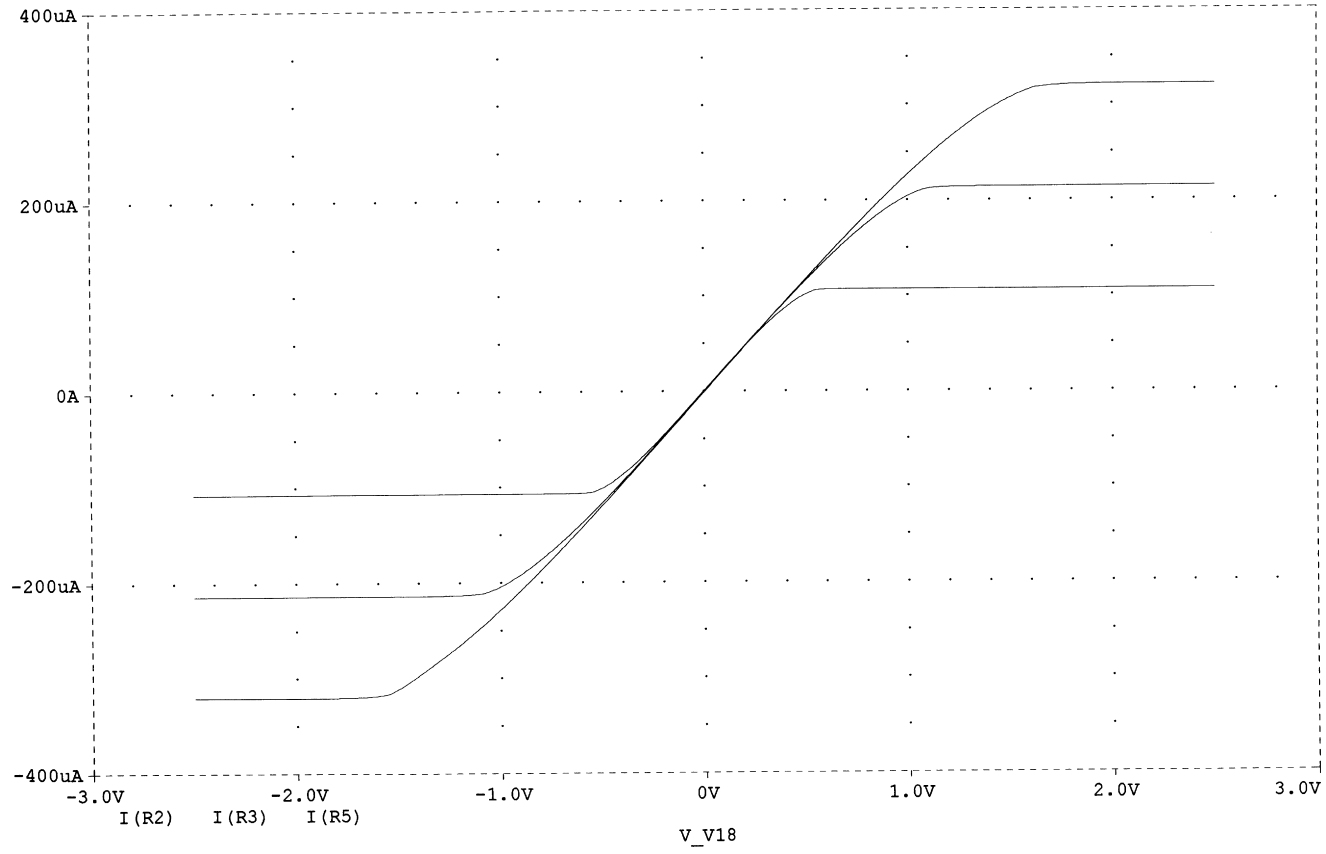


Fig. 7. The *I–V* characteristics of the ELTP of two and three stages after modification versus the LTP.

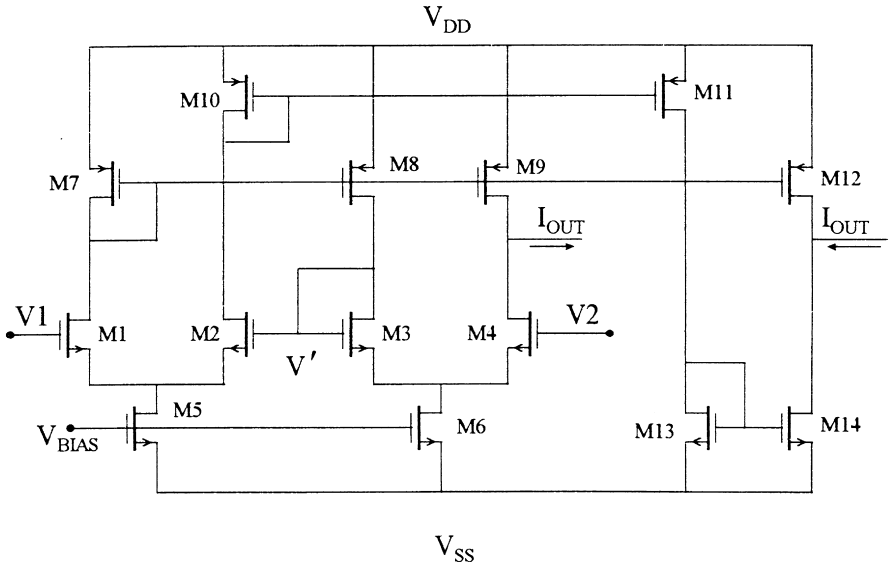


Fig. 8. The proposed CMOS BOTA.

given by:

$$I_{OUT} = \sqrt{\frac{K_n K_p}{2}}(V_1 - V_2)(V_3 - V_4)(1 + \Delta_1) \qquad (41)$$

where Δ_1 represents the nonlinearity factor in the expression of the output current resulting from the exact expression of Eq. (7). Based on the circuit reported in [1] and following the same approach, each NMOS pair can be replaced by two NMOS pairs in order to transform the two equivalent LTPs

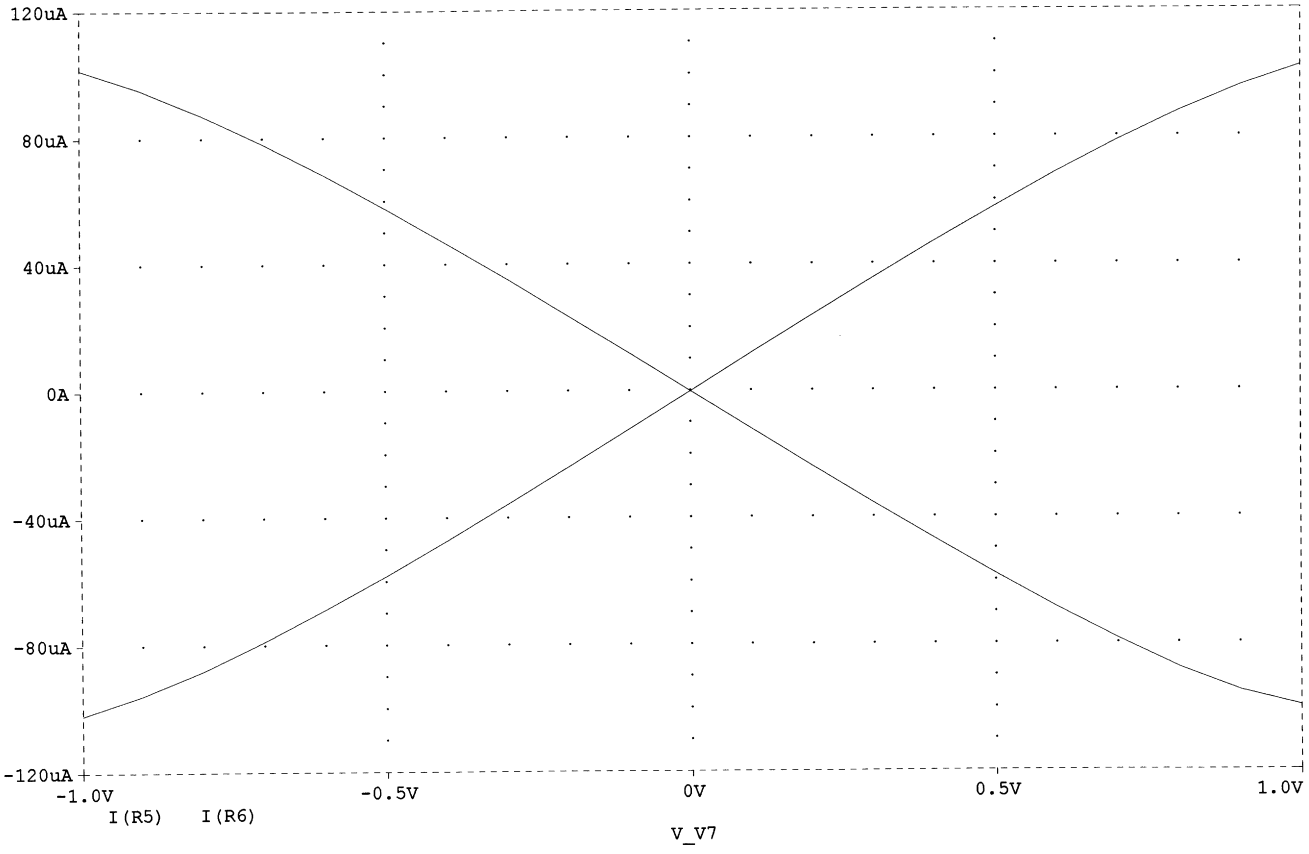


Fig. 9. The *I–V* characteristics of the CMOS BOTA.

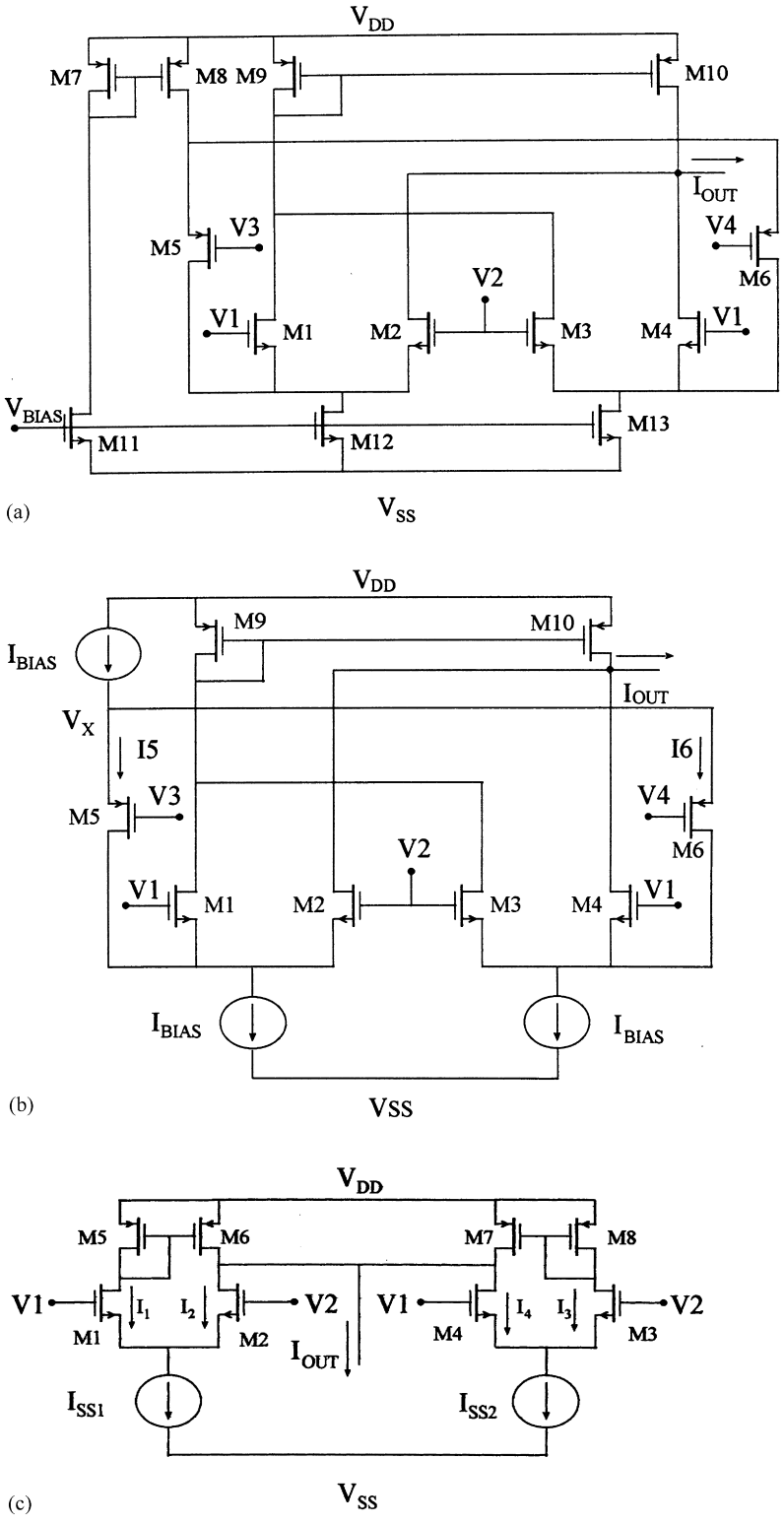
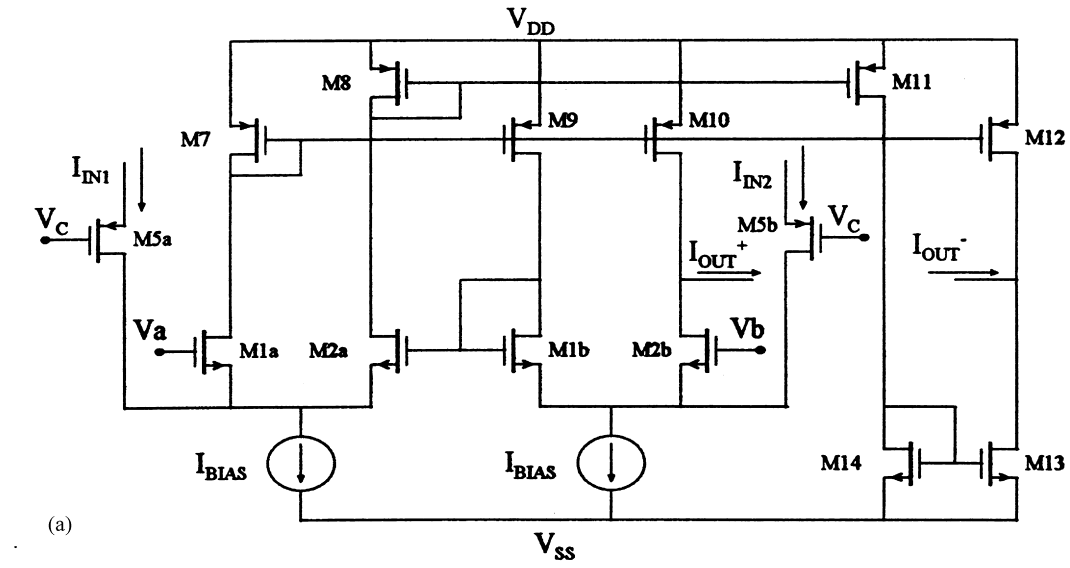


Fig. 10. (a) The voltage-controlled transconductor proposed in [1]. (b) The modified transconductor (a) showing the equivalent biasing currents. (c) The equivalent LTP circuit of the circuit in (a).

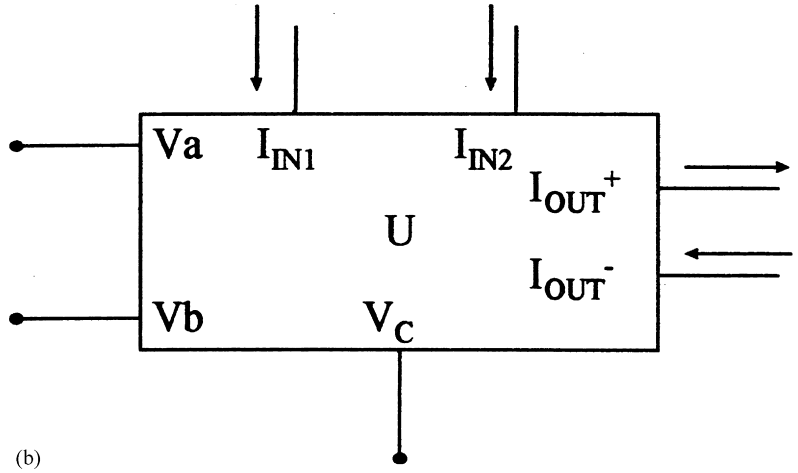
to two equivalent ELTPs. The output current will then be:

$$I_{\mathrm{OUT}} = \frac{1}{2}\sqrt{\frac{K_{\mathrm{n}}K_{\mathrm{p}}}{2}}(V_1 - V_2)(V_3 - V_4)(1 + \Delta_2) \qquad (42)$$

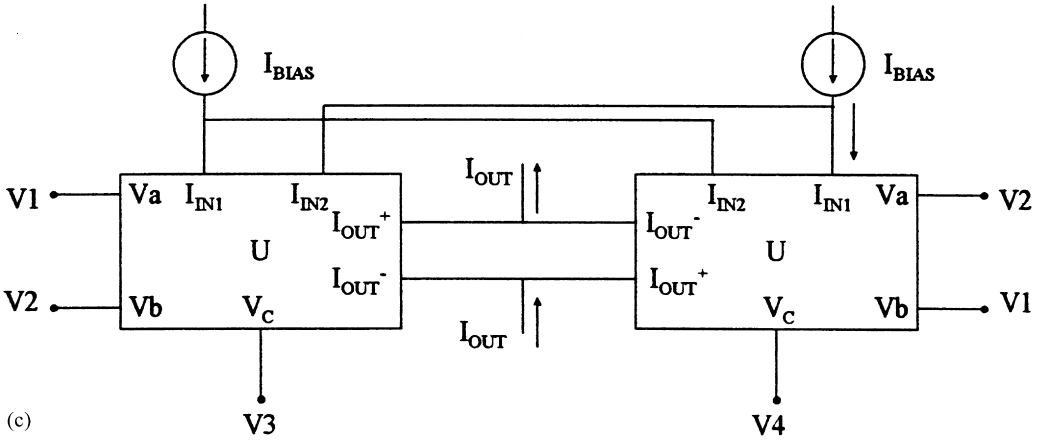
where Δ_2 represents the nonlinearity factor in the expression of the output current resulting owing to the exact expression of Eq. (23). It can be easily seen that $\Delta_2 < \Delta_1$, thus better linearity is obtained. Fig. 11(a) represents the circuit after



(a)

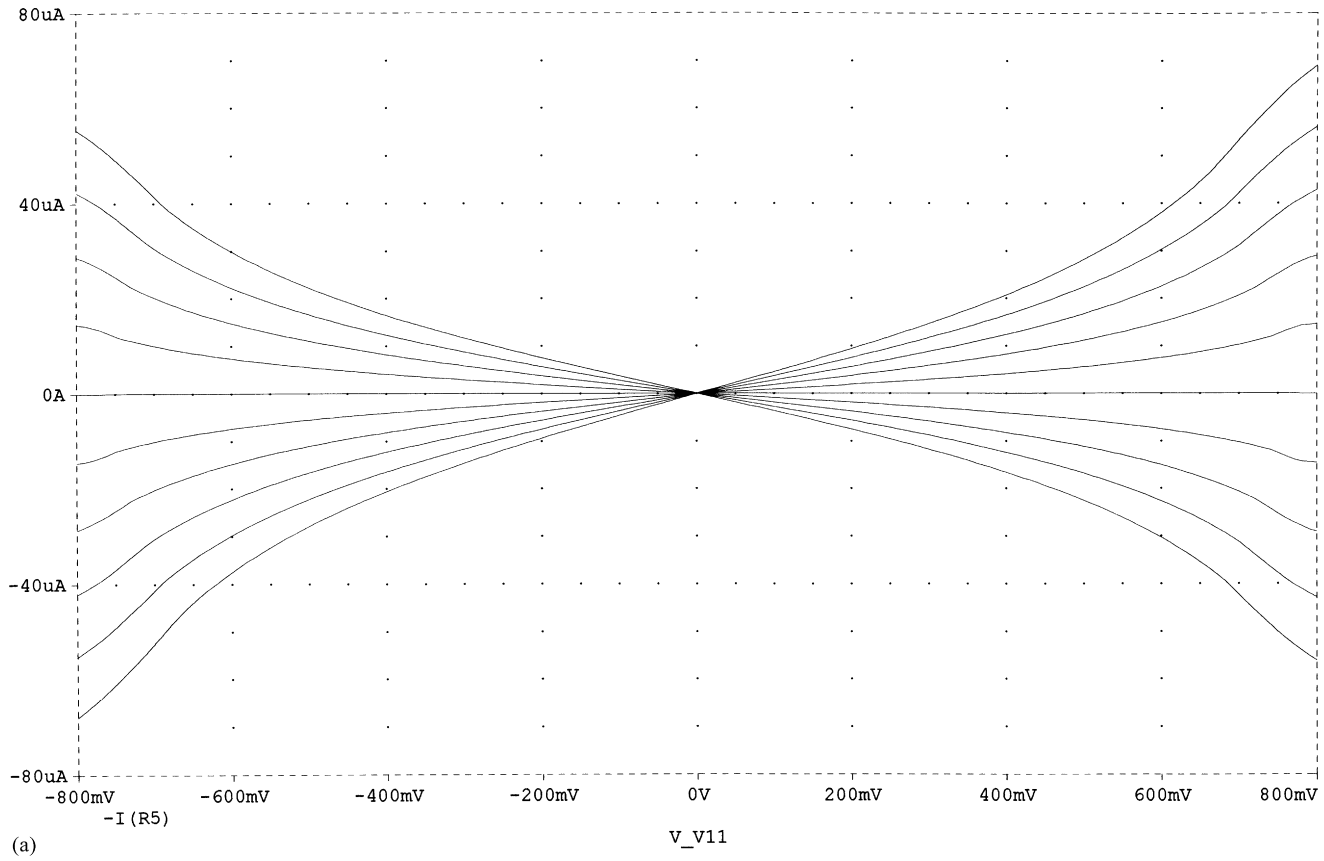


(b)

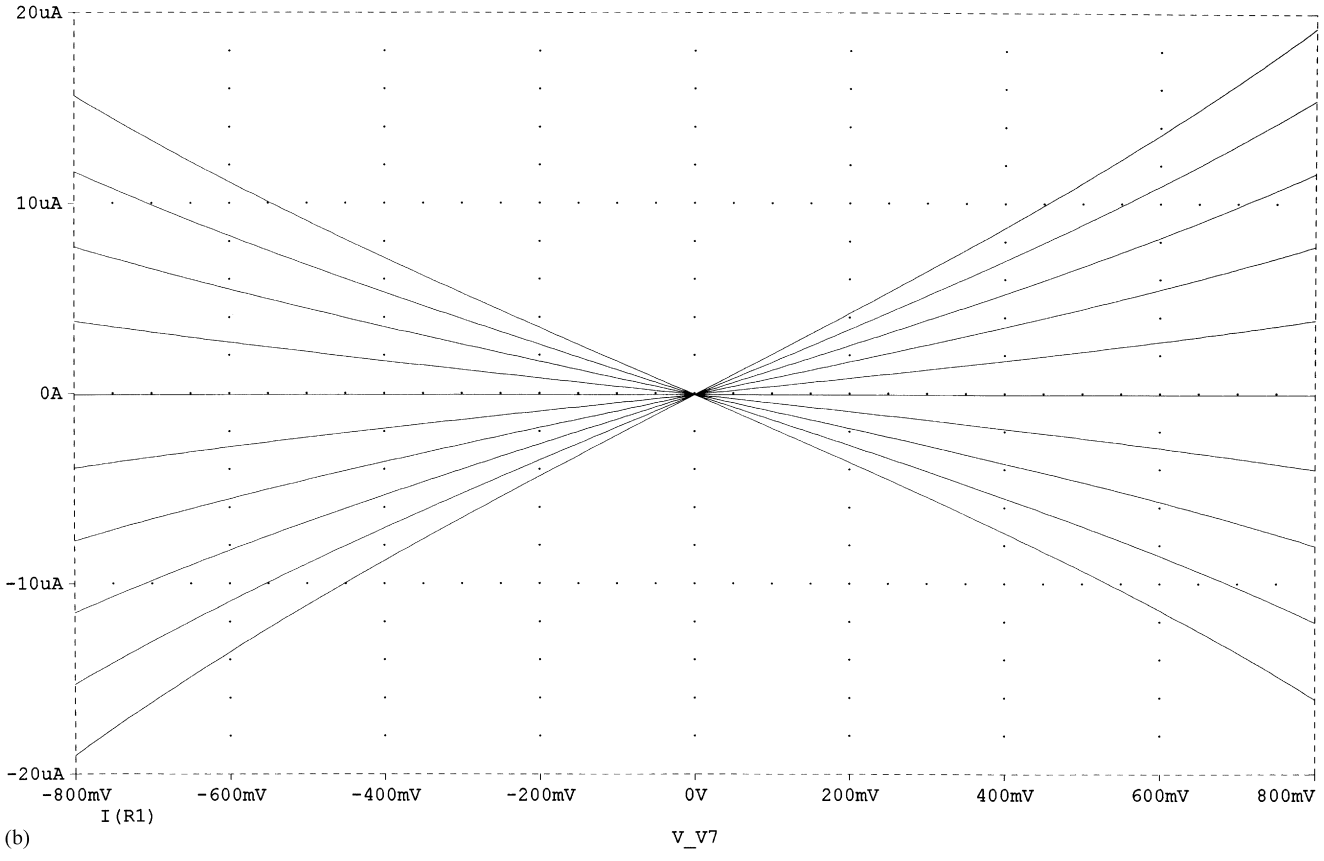


(c)

Fig. 11. (a) The equivalent LTP circuit of one pair of NMOS transistors of voltage-controlled transconductor proposed in [1]. (b) The equivalent building block of (a). (c) The proposed voltage-controlled CMOS BOTA.



(a)



(b)

Fig. 12. (a) The *I–V* characteristics of the voltage-controlled CMOS transconductor proposed in [1] for different values of the control voltage. (b) The *I–V* characteristics of the voltage-controlled CMOS BOTA for different values of the control voltage.

Table 5
The aspect ratios of the transistors used in Fig. 10(a)

Transistor	Aspect ratio
M1–M4	3.5/3.5
M5, M6	7/3.5
M11–M13	14/2.8
M7–M10	21/3.5

Table 6
The aspect ratios of the transistors used in Fig. 11(a)

Transistor	Aspect ratio
M1a, M2a, M1b, M2b	3.5/3.5
M5a, M5b	10.5/3.5
M7–M14	21/3.5

the substitution of the LTP by the ELTP. Fig. 11(b) represents the equivalent building block standing for the circuit in Fig. 11(a).

A highly linear voltage-controlled transconductor is obtained by using two of these blocks connected as shown in the Fig. 11(c), which can be also used as a multiplier. The balanced output current obtained has many applications in the filter design and in the implementation of voltage-controlled resistors [9].

PSpice simulation results for both the voltage-controlled transconductor proposed in [1] and the voltage-controlled BOTA of Fig. 11(c) were carried out with the transistors aspect ratios as given in Tables 5 and 6 respectively and with $\pm$ 2.5 supply voltages.

Fig. 12(a) represents the I–V characteristics of the circuit proposed in [1]. $V1$ is scanned from -0.8 to 0.8 V for different values of control voltage keeping $V2$ at 0 V.

Fig. 12(b) represents the I–V characteristics of the proposed BOTA of Fig. 11(c). $V1$ is scanned from -1 to 1 V for different values of control voltage keeping $V2$ at 0 V.

Fig. 13 represents the simulated output current of the proposed BOTA resulting from the multiplication of two differential input voltages of 10 MHz (sinusoidal) and 500 kHz (triangular) respectively.

5. Proposed multiplier divider

A voltage-controlled transconductor can also be used as a

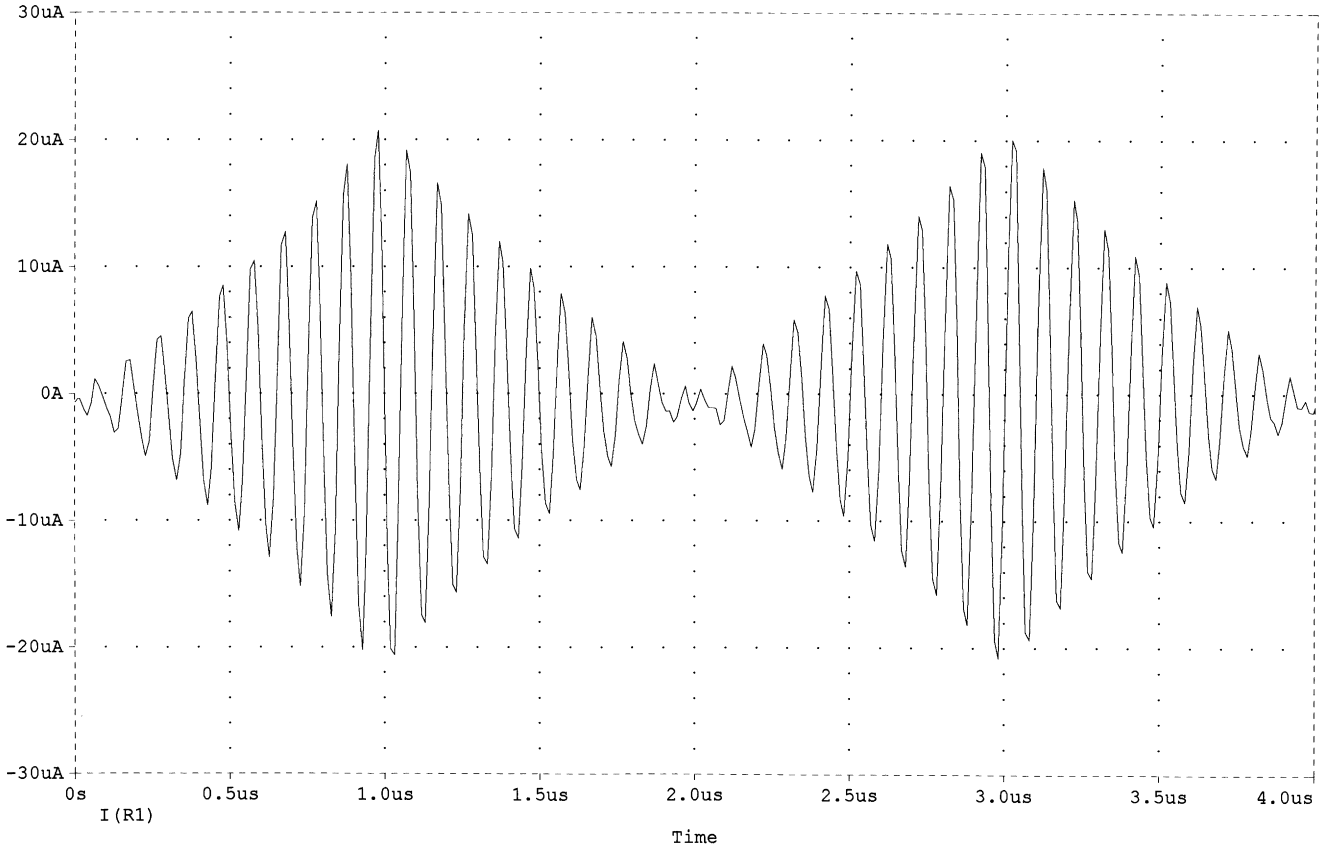


Fig. 13. The Transient analysis of the output current of the voltage-controlled CMOS BOTA resulting from the multiplication of two differential input voltages.

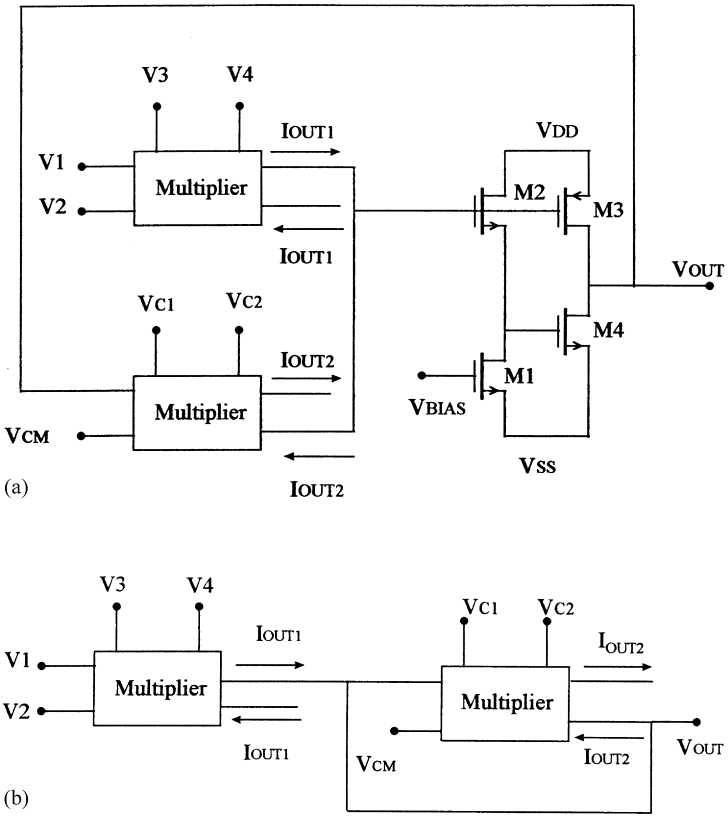


Fig. 14. The proposed multiplier divider based on CMOS voltage-controlled transconductor.

voltage multiplier whose output is proportional to the product of two differential input voltages. A multiplier divider can be also obtained where the output quantity is a voltage as shown in Fig. 14(a) (closed loop implementation)

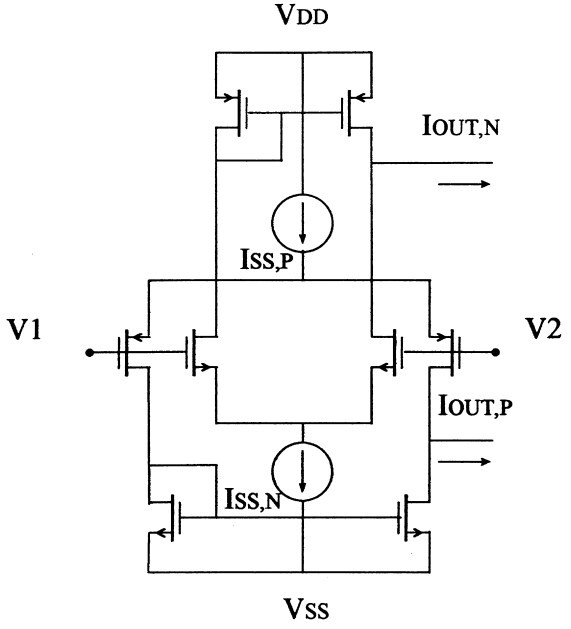


Fig. 15. The complementary differential input stage with active load.

as well as the one in Fig. 14(b) (open loop implementation) have the advantage of operating insensitively to the process parameters (no dependence on K_n or K_p) in the case of matched cells. In both circuits, an additional balanced output current that is proportional to the product of the two differential inputs $(V_1 - V_2)$ and $(V_3 - V_4)$ is also obtained:

$$I_{OUT1} - I_{OUT2} = 0, \tag{43}$$

$$\frac{1}{2}\sqrt{\frac{K_n K_p}{2}}(V_1 - V_2)(V_3 - V_4) - \frac{1}{2}\sqrt{\frac{K_n K_p}{2}}(V_{CM} - V_{OUT}) \times (V_{C1} - V_{C2}) = 0, \tag{44}$$

$$V_{OUT} = V_{CM} + \frac{(V_1 - V_2)(V_3 - V_4)}{(V_{C1} - V_{C2})}. \tag{45}$$

The voltage V_{CM} represents a controllable shift in the DC level of V_{OUT} and can be taken equal to zero:

$$I_{OUT1} = I_{OUT2} = \frac{1}{2}\sqrt{\frac{K_n K_p}{2}}(V_1 - V_2)(V_3 - V_4). \tag{46}$$

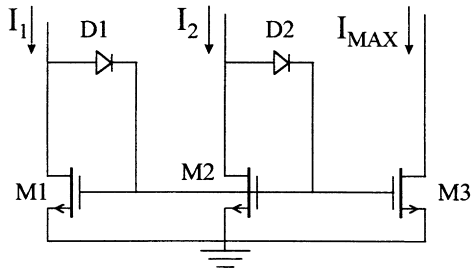


Fig. 16. The maximum circuit used to extract the maximum of two currents [12].

6. Low voltage rail-to-rail highly linear transconductor

A simple CMOS complementary stage is shown in Fig. 15. If the body effect is ignored, the input voltage common mode range is limited to [7]:

$$V_{\mathrm{CM,min}} = V_{\mathrm{SS}} + \sqrt{\frac{I_{\mathrm{SS,n}}}{K_n}} + V_{\mathrm{T_n}} - |V_{\mathrm{T_p}}|, \tag{47}$$

$$V_{\mathrm{CM,max}} = V_{\mathrm{DD}} + \sqrt{\frac{I_{\mathrm{SS,p}}}{K_{\mathrm{p}}}} + V_{\mathrm{T_n}} - |V_{\mathrm{T_p}}|. \tag{48}$$

Therefore, almost rail-to-rail operation can be achieved. However, to improve the common mode input voltage range and thereby achieve full rail-to-rail input range, folded cascode configuration for the input stage may be used. The input stage transconductance is defined as:

$$g_{\mathrm{mn}} = \sqrt{K_{\mathrm{n}} I_{\mathrm{SS,n}}}, \tag{49}$$

$$g_{\mathrm{mp}} = \sqrt{K_{\mathrm{p}} I_{\mathrm{SS,p}}} \tag{50}$$

which is a function of the bias current and common-mode input voltage. If the input complementary differential pairs have an overlapping constant g_{m} region, a constant g_{m} can be obtained simply by picking the maximum g_{m} at any given V_{CM} [7]. To this end, a circuit that compares the amplitudes of the signals at the output of the NMOS and PMOS differential pairs and redirects the larger one to the output is needed. For this purpose, the maximum circuit shown in Fig. 16, which is a modified replica of the circuit reported in [12] although being simple gives very good performance. Its action can be described by the following:

The gate voltage, being common among all the shown matched transistors, will follow the value of the maximum current of the given two inputs, in this case (assuming that I_1 is greater than I_2), the diode D1 will be on, the transistor M2 will be forced to operate in the ohmic region (the current I_2 being lower than I_1, will force the transistor M2, to leave the saturation region). The voltage V_{DS} of the transistor M2 being in the ohmic region will be low, thus the diode D2 will be off, and the transistor M3 will conduct the maximum current (I_1). The diodes, in Fig. 15, being unavailable in the CMOS technology, can be replaced by diode connected MOS transistors.

The proposed rail-to-rail transconductor is shown in Fig. 17. Two NMOS pairs (M1–M2 and M3–M4), and two PMOS pairs (M5–M6 and M7–M8) are used. The NMOS pair operates till the positive supply rail, while the PMOS pair operates till the negative supply rail. Every two pairs of the same type form an ELTP transconductor. It is noted that the number of these pairs can be increased in order to obtain higher linearity and wider range. The currents in the NMOS pairs are compared to the currents in the PMOS pairs using two maximum circuits. One of them is NMOS maximum circuit (M15, M16, M17, M18 and M19), while the other one is PMOS maximum circuit (M20, M21, M22, M23 and M24). The comparison is performed on each branch of the

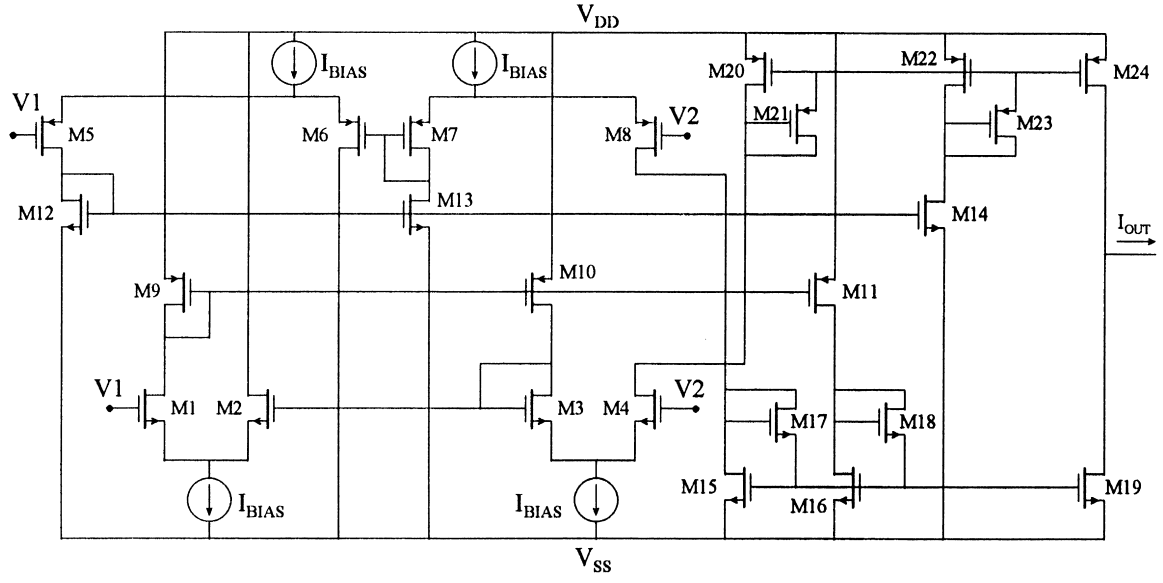


Fig. 17. The proposed rail-to-rail CMOS transconductor.

Table 7
The aspect ratios of the transistors used in Fig. 17

Transistor	Aspect ratio
M1–M4	3.5/3.5
M5–M8	10.5/3.5
M9–M11	21/3.5
M12–M14	7/1.4
M15, M16, M19	9.8/1.4
M20, M22, M24	21/3.5
M21, M23, M17, M18	1.4/1.4

pair instead of comparing the output of each pair in order to minimize the circuit, i.e. the current in one branch in the NMOS pair is compared to the current in another branch in the PMOS pair. The result is the same as in the case of the comparison of currents in the NMOS pairs and PMOS pairs separately. The output currents from the maximum circuits are subtracted to obtain the output current I_{OUT}. A fine adjustment of the aspect ratios for the PMOS and NMOS pairs is necessary to obtain a constant value for the transconductance.

To show that the proposed input stage operates from rail-to-rail, the minimum and maximum input common voltages should be found. When calculating the $V_{CM,max}$ and $V_{CM,min}$ and neglecting the body effects, one obtains:

$$V_{CM,min} = V_{SS} + V_{DS,sat,n} - |V_{T_p}|, \tag{51}$$

$$V_{CM,max} = V_{DD} - V_{SD,sat,p} + V_{T_n} \tag{52}$$

where $V_{DS,sat,n}$ and $V_{SD,sat,p}$ are the minimum drain-source voltages of the single-transistor NMOS current sink and PMOS current source, respectively.

As a consequence, the common mode input voltage can even extend above the positive rail by $(V_{T_n} - V_{SD,sat,p})$ and below the negative rail by$(-|V_{T_p}| + V_{DS,sat,n})$ with a constant g_m.

Therefore, as the main advantage of the ELTP over LTP is the compromise between the input voltage common mode range and the input voltage differential mode range, there is no need to replace the LTP by an ELTP because the input voltage common mode range extends already from the positive rail to the negative rail. However, the usage of ELTP is still advantageous regarding the power consumption. Given that the power consumption is almost proportional to the current tail value, the ELTP needs twice the number of current tails when compared with the LTP. But from Eqs. (8) and (24), one obtains that the LTP needs four times the

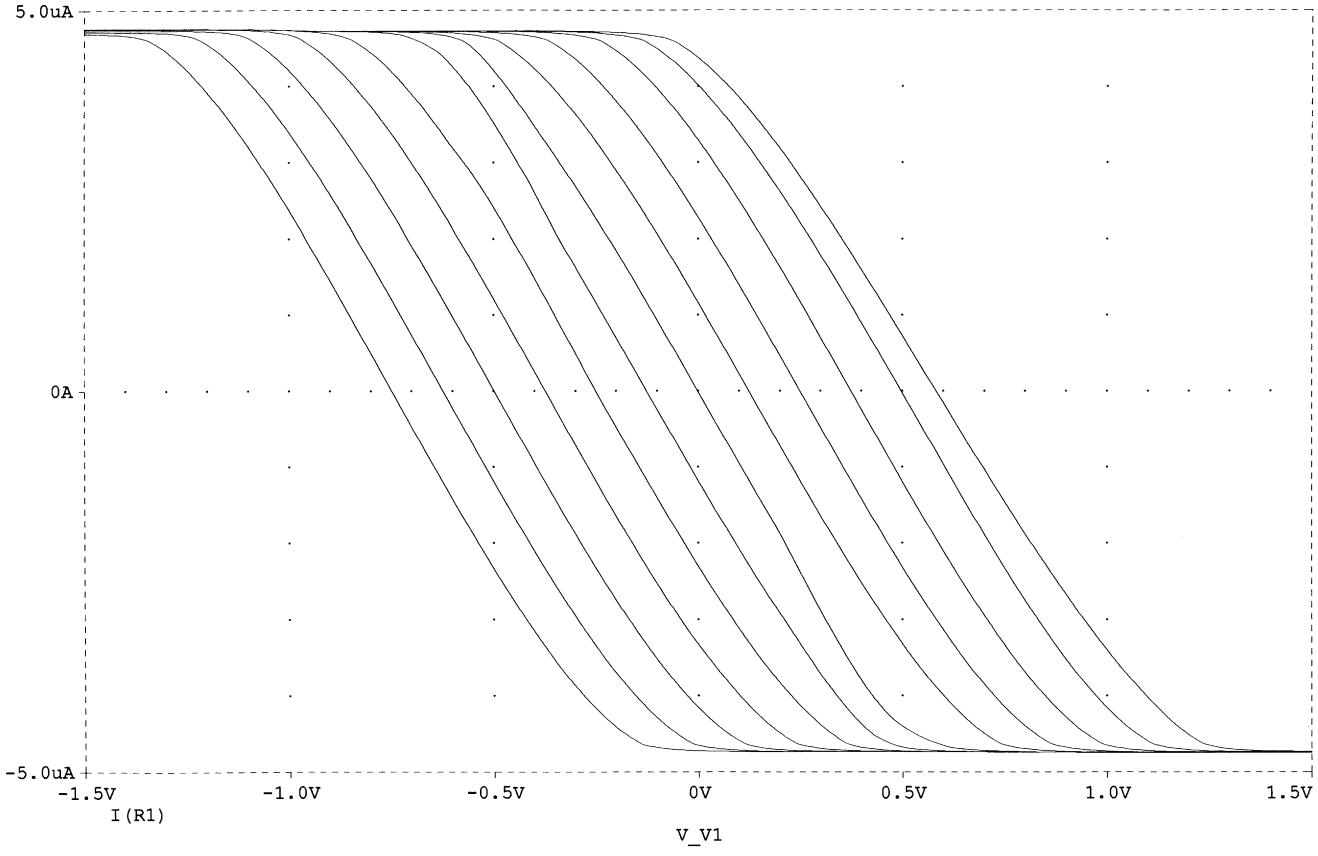


Fig. 18. The *I–V* characteristics of the CMOS rail-to-rail transconductor.

value of the current tail when compared with the ELTP in order to obtain the same input voltage differential mode range as the latter is proportional to $\sqrt{I_{SS}}$. Thus the power consumption in case of ELTP is reduced by around 50% for the same input voltage differential mode range.

P Spice simulation results for the low voltage low power rail-to-rail transconductor were carried out with the transistors aspect ratios as given in Table 7 and with ± 1.5 V supply voltages.

Fig. 18 represents the I–V characteristics of the low voltage rail-to-rail transconductor. $V1$ is scanned from -1.5 to 1.5 V for different values of $V2$.

7. Conclusion

A new family of transconductors based on the LTP was presented. The advantages of this family over the normal LTP family of transconductor were discussed.

It was shown that the ELTP is a very attractive solution to overcome the restrictions that limited the use of LTP in some applications. Also a voltage-controlled transconductor and a low voltage rail-to-rail transconductor as well as their simulated performances were presented. It was proven that the ELTP gives more freedom to compromise between the power consumption and the extent to which the linearity can be maintained.

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