

## Novel CMOS Wide-Linear-Range Transconductance Amplifier

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**Abstract**—In this brief, a novel technique for linearizing long tail differential pairs is proposed. It is shown that the proposed linearized transconductor offers excellent linearity and exceptionally wide operating range, which makes it suitable to operate in analog signal processing applications. PSpice simulation results are given.

**Index Terms**—CMOS transconductors.

### I. INTRODUCTION

Transconductance elements are useful building blocks in analog signal processing systems especially in continuous-time filters and four-quadrant multipliers [1]–[12]. Many implementations have been reported in the literature in order to obtain highly linear transconductors. Among these realizations are the ones that are based on the long tail differential pair (LTP), which have received a great interest since they offer a relatively low level of distortion because of the negligible second-order effects (mainly body-effect and mobility degradation). In addition, the power consumption of these structures are usually limited compared with other realizations. In the literature, several techniques have been described in order to extend the linearity range of the LTP [1]–[7], [12]. The cross-coupled technique has been first proposed by Khorramabadi [1] by properly scaling the aspect ratios of the differential pair and the bias current used. Then the adaptively biased CMOS differential pair has been introduced by Nedungadi *et al.* [2]. Recently, Kimura has proposed the dynamic bias current technique [3]. Other techniques have been reported in the literature [8]–[10].

In this brief, the analysis of the LTP is briefly summarized showing the limitations on its operating range. Using the adaptive biasing technique first proposed by Nedungadi *et al.* [2], a novel dynamically biased squaring circuit is used to linearize the LTP. Then the linearity range extension technique proposed in [12] is used to obtain a very wide operating range.

### II. ADAPTIVELY BIASED DIFFERENTIAL PAIR

The differential pair transconductor represents a useful analog building block due to its simplicity and its high frequency response [4]–[7]. However, the nonlinearity generated by the constant current operation always restricts the scope of this structure. Consider the matched adaptively biased differential pair proposed in [2], which is shown in Fig. 1. All the transistors used are assumed to be operating in the saturation region, where the drain current of the NMOS transistor operating in that region (neglecting the channel length modulation effect) is given by

$$I = \frac{K_n}{2} (V_{GS} - V_T)^2 \quad (1)$$

$$K_n = (\mu_n C_{ox}) \left( \frac{W}{L} \right) \quad (2)$$

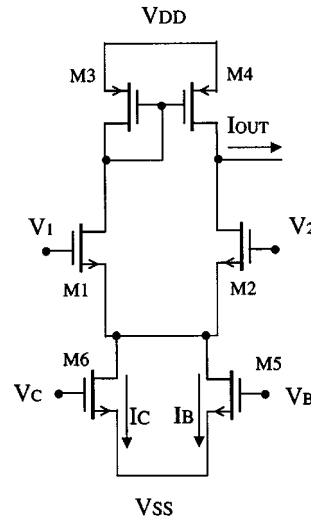


Fig. 1. The adaptively biased LTP transconductor circuit.

where

- $V_T$  is the threshold voltage,
- $K_n$  is the transconductance parameter,
- $\mu_n$  is the effective carrier mobility,
- $C_{ox}$  is the gate oxide capacitance per unit area,
- $W$  is the channel width, and
- $L$  is the channel length.

Assuming that all body terminals are connected to the proper supply voltages and that transistor M6 is absent. The output current as a function of the two input voltages  $V_1$  and  $V_2$  is obtained as

$$I_{OUT} = \sqrt{K_n I_{SS}} (V_1 - V_2) \sqrt{1 - \frac{K_n (V_1 - V_2)^2}{4I_{SS}}} \quad (3)$$

Therefore, the differential input voltage is limited to the range

$$-\sqrt{\frac{2I_{SS}}{K_n}} \leq (V_1 - V_2) \leq \sqrt{\frac{2I_{SS}}{K_n}} \quad (4)$$

While the common-mode voltage is given by

$$V_{CM} = V_{S \min} + V_T + \sqrt{\frac{I_{SS}}{K_n}} \quad (5)$$

which usually limits the differential-mode operating range since the ratio  $I_{SS}/K_n$  cannot be raised high enough without limiting the common-mode operating range. In addition, the output current is only linear within approximately half of this range due to the effect of the nonlinearity term given by (3), which makes the circuit unsuitable for many applications. Consequently, an adaptive biasing technique was proposed in [2] in order to cancel the nonlinearity term and extend the operating region, which is achieved by adding the transistor M6 to the circuit. From (3), it is seen that the current tail will be given by

$$I_{SS} = I_B + I_C \quad (6)$$

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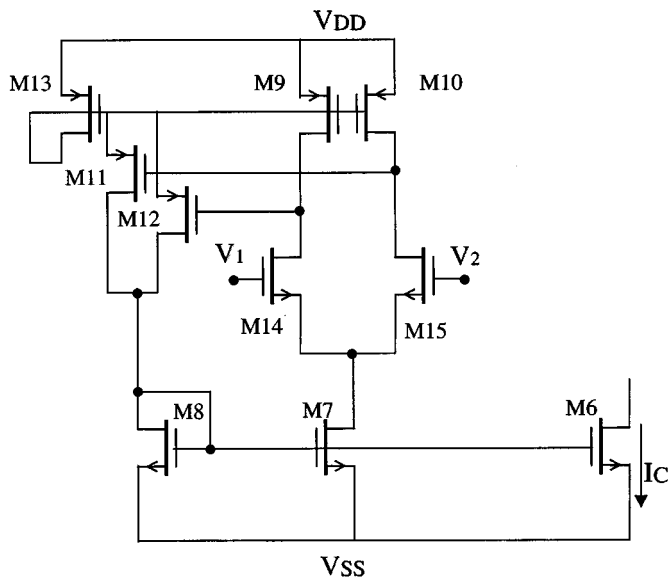


Fig. 2. The proposed squaring circuit.

where

$$I_C = \frac{K_n}{4} (V_1 - V_2)^2 \quad (7)$$

where  $I_{SS}$  is the effective current tail value delivered to the differential pair,  $I_C$  is the compensating current tail that extends the linearity range of the differential pair, and  $I_B$  is the uncompensated current tail of the differential pair. In this case, the output current is given by

$$I_{OUT} = \sqrt{K_n I_B} (V_1 - V_2). \quad (8)$$

It is noted that for M1 and M2 to be ON, the linearity range is limited to the value

$$-2\sqrt{\frac{I_B}{K_n}} < (V_1 - V_2) < 2\sqrt{\frac{I_B}{K_n}}. \quad (9)$$

It is clear that a squarer circuit that performs the relation given by (7) is needed. Many implementations of the squarer circuit have been given in the literature [2]–[6], but the major problem that faced them is the limitations on the operating range of the squarer circuits themselves that consequently leads to limitations on the operating range given by (9). In the following section, a novel squaring circuit based on a modified LTP with a wide differential mode range is presented.

### III. THE PROPOSED SQUARING CIRCUIT

The main idea is to use negative feedback in order to transform the LTP into a squaring circuit. By taking the absolute value of the output current of the LTP, one obtains:

$$|I_{OUT}| = \sqrt{K_{n1} I_C} |V_1 - V_2| \sqrt{1 - \frac{K_{n1} (V_1 - V_2)^2}{4I_C}} \quad (10)$$

where  $K_{n1}$  is the transconductance parameter of each of the matched transistors M14 and M15 and  $I_C$  is the current tail of the differential pair in Fig. 2.

The aim is to apply a negative feedback action such that this value can be adjusted to the value

$$|I_{OUT}| = \frac{I_C}{a} \quad (11)$$

where  $I_{OUT}$  is simply the difference between the current flowing in M14 and M15 (although it is not driven from the circuit).  $I_C$  in this

case is a variable that represents the degree of freedom in this feedback action. Accordingly, when substituting from (10) in (11), one obtains

$$4I_C^2 - 4K_{n1}a^2(V_1 - V_2)^2 I_C + K_{n1}^2 a^2 (V_1 - V_2)^4 = 0. \quad (12)$$

The result is an equation of the second degree whose unique solution is given by

$$I_C = \frac{1}{2} K_{n1} (V_1 - V_2)^2 \left( a^2 + \sqrt{a^4 - a^2} \right) \quad (13)$$

where the second solution for (12) is refused for inconsistency since it does not satisfy the condition on the operating range of the LTP defined by (4). In order to realize the negative-feedback action mentioned above, it is noted that the absolute value of the output current in the LTP is also given by

$$|I_{OUT}| = 2I_{MAX} - I_C \quad (14)$$

where  $I_{MAX}$  is the maximum of the two currents flowing in M14 and M15, respectively. Substituting for  $|I_{OUT}|$  in (11), one obtains:

$$\frac{I_C}{I_{MAX}} = \frac{2a}{a+1}. \quad (15)$$

So, by simply picking up the maximum current of the two branches of the LTP and feeding it back to the current tail  $I_C$  according to (15), the required squarer circuit can be obtained. It must be mentioned that a similar approach for adaptive biasing scheme has been introduced in [13] for the design of class AB operational amplifiers with high slew rates. However, up to the authors' knowledge, this scheme has not been previously used to obtain a linear transconductor.

Consider the circuit shown in Fig. 2, the current-mode maximum circuit (M9–M13) reported in [11] is applied to the LTP formed from (M14, M15, and M7) and picks up the maximum current of the two branches by means of one of the two transistors M11 and M12 that acts like a diode and forces the common gate of (M9, M10, and M13) to follow the maximum current between the ones flowing in M9 and M10. Consequently, the maximum current signal needed to produce the current tail  $I_C$  is extracted, feedback and scaled by adjusting the aspect ratios of M7–M13.

When using the proposed squaring circuit for the adaptive biasing of the LTP and in order to obtain the required value for the current tail as defined by (7) it is necessary to have

$$K_{n1} \left( a^2 + \sqrt{a^4 - a^2} \right) = \frac{K_n}{2}. \quad (16)$$

Therefore, defining

$$a^2 + \sqrt{a^4 - a^2} = m \quad (17)$$

where  $m$  is a rational number. Solving (17) for  $a$ , one obtains

$$a = \frac{m}{\sqrt{2m-1}}. \quad (18)$$

The aim is to obtain  $a$  as a rational number in order to realize (15) by using simple current mirrors. In order to do this,  $(\sqrt{2m-1})$  must be a real number.

This is realized by taking  $m = 5/2$ . In this case, one obtains

$$a = \frac{5}{4}. \quad (19)$$

Substituting in (13), the current flowing in M6 (or M7) is given by

$$I_C = \frac{5K_{n1}}{4} (V_1 - V_2)^2. \quad (20)$$

Substituting in (15), one obtains

$$\frac{I_C}{I_{MAX}} = \frac{2a}{a+1} = \frac{10}{9} \quad (21)$$

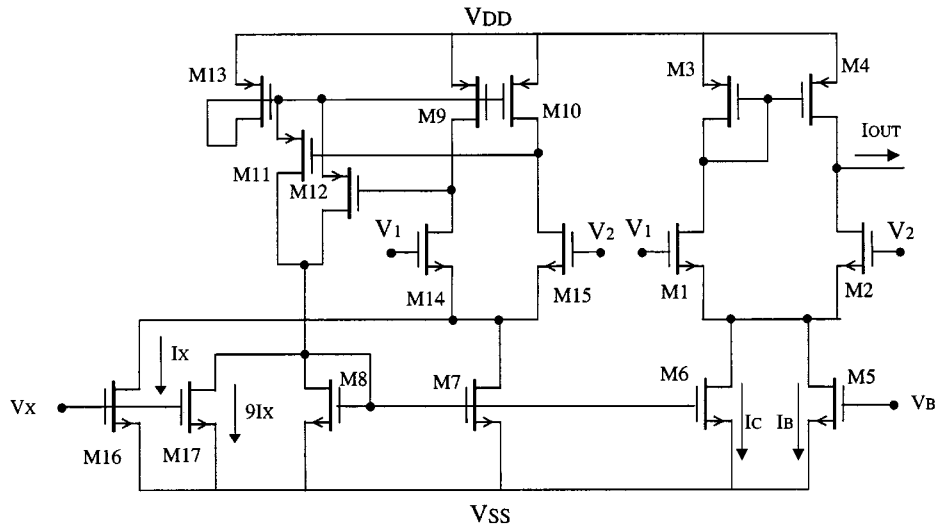


Fig. 3. The complete adaptively biased LTP circuit.

which can be realized by choosing appropriate values of the aspect ratios of the transistors M7–M13 in such a way that the multiplication by 10 is performed through M9–M13 and the division by 9 through M7–M8. Finally, from (20), by choosing  $K_n = 5K_{n1}$ , one can realize the condition stated in (7) in order to obtain the required linearization action. One limitation on the circuit is that in the case of no signal (i.e.,  $V_1 = V_2$ ), transistors M14 and M15 are off and also the maximum circuit has to switch between drain currents of the differential pair, which cause cross-over distortion at high frequencies. To avoid this problem, a bias current is necessary but in a way not to violate the square law identity obtained previously. In the circuit given in Fig. 3, transistor M16 has been added to prevent the circuit from switching off. In order to compensate for this change, transistor M17 has been also added such that the ratio between the aspect ratio of M17 and M16 is the same as between M7 and M8, respectively, which is equal to 9. Therefore, since  $(I_{C1} + I_X)$  is the new biasing current tail to the differential pair, (21) will be modified in order to obtain the new feedback condition as follows:

$$\frac{I_{C1} + I_X}{I_{MAX}} = \frac{10}{9}. \quad (22)$$

Consequently, the required feedback action will be realized at the gate node of M8 by satisfying the following equation:

$$I_{C1} = \frac{1}{9}(10I_{MAX} - 9I_X) \quad (23)$$

which demonstrates the usefulness of M17 in preserving the square law relation obtained previously.  $I_X$  is chosen to a very small value since it is only necessary to keep M14 and M15 ON. Substituting in (20) by  $(I_{C1} + I_X)$  instead of  $I_{C1}$ , it is noted that for  $|V_1 - V_2| < 2\sqrt{I_X/K_n}$ , the current  $I_{C1}$  drops to zero since the later cannot be practically negative. But fortunately, in this narrow range, the output current of the linearized LTP is already near zero so the effect of the absence of  $I_{C1}$  on the linearity is negligible as shown later in the simulations. The output current will therefore be given by

$$I_{OUT} = \sqrt{K_n(I_B - I_X)}(V_1 - V_2) \quad (24)$$

with the linearity range given by

$$-2\sqrt{\frac{(I_B - I_X)}{K_n}} \leq (V_1 - V_2) \leq 2\sqrt{\frac{(I_B - I_X)}{K_n}}. \quad (25)$$

It is clear that the value of  $I_X$ , which is practically chosen very small (less than  $1 \mu A$ ) can be compensated by an equivalent increase in the

value of  $I_B$ , since  $I_X$  is of constant value. Simulation results in Section V verify the analysis.

#### IV. THE EXTENDED ADAPTIVELY BIASED SOURCE-COUPLED DIFFERENTIAL PAIR (EALTP)

The main idea is to try to extend the linearity range of the simple differential pair by the usage of more than one differential pair resulting in transconductors with higher linearity and wider input voltage differential mode range [12]. By applying this technique on the proposed adaptively biased transconductor, it is obvious that the linear range will be largely widened.

The extended long tail differential pair (ELTP) transconductor reported in [12] is mainly based on the usage of two simple differential pairs as shown in Fig. 4. The difference between the two input voltages is divided equally over two matched differential pairs. By analyzing the given circuit, one obtains

$$V' = \frac{V_1 + V_2}{2} \quad (26)$$

where  $V'$  is the gate voltage of M3 and M4 as shown in Fig. 4. Hence, in the case of the absence of transistors M17 and M19, the output current  $I_{OUT}$  would be given by [12]:

$$I_{OUT} = \sqrt{K_n I_{SS}}(V_1 - V_2) \sqrt{1 - \frac{K_n(V_1 - V_2)^2}{16I_{SS}}}. \quad (27)$$

The operating range is thus given by

$$-2\sqrt{\frac{2I_B}{K_n}} \leq (V_1 - V_2) \leq 2\sqrt{\frac{2I_B}{K_n}}. \quad (28)$$

Hence, for the same  $I_{SS}$  and  $K_n$ , the ELTP has wider linearity range than the LTP. Therefore, it is noted that in order to obtain a certain differential-mode input range, the ELTP needs a lower value for the ratio  $(I_{SS}/K_n)$  than the LTP, hence the common-mode operating range is increased which is suitable for low supply voltage operation.

In order to obtain better performance, both techniques are used to obtain the EALTP shown in Fig. 4 (taking in account the effect of transistors M17 and M19). Using (28), it is easy to obtain that the compensating current  $I_C$  in this case is given by

$$I_C = \frac{K_n}{16}(V_1 - V_2)^2. \quad (29)$$

Comparing (29) and (7), the factor of four can be obtained by simply adjusting the aspect ratios of M17 and M19 to be four times lower than

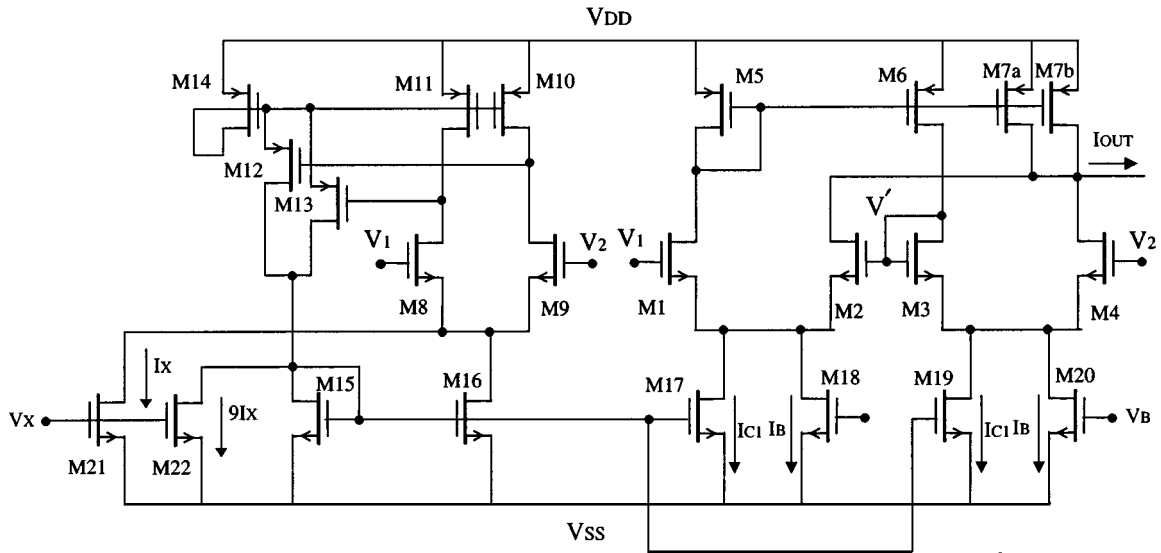
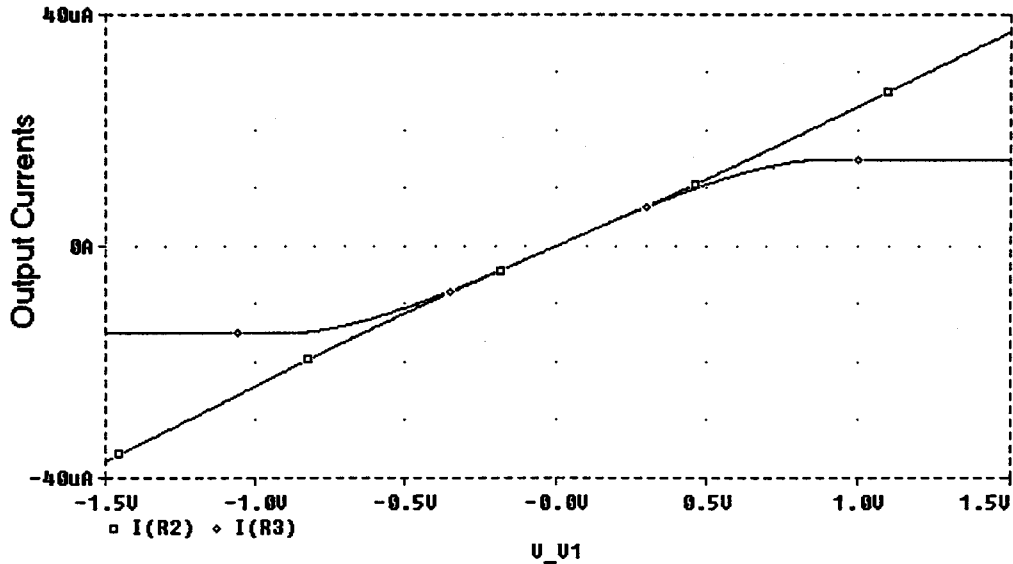


Fig. 4. The proposed wide-linear range transconductor circuit.


 Fig. 5. The  $I$ - $V$  characteristics of the proposed EALTP versus the ordinary LTP.

the aspect ratio of M16. Following to the same approach of the previous section, the compensating current  $I_{C1}$  is given by

$$I_{C1} = \frac{K_n}{16} (V_1 - V_2)^2 - \frac{1}{4} I_X. \quad (30)$$

Consequently, the output current  $I_{OUT}$  is given by

$$I_{OUT} = \sqrt{K_n (I_B - \frac{1}{4} I_X)} (V_1 - V_2) \quad (31)$$

and the linearity range is finally given by

$$-4 \sqrt{\frac{(I_B - \frac{1}{4} I_X)}{K_n}} \leq (V_1 - V_2) \leq 4 \sqrt{\frac{(I_B - \frac{1}{4} I_X)}{K_n}}. \quad (32)$$

Thus when compared to an ordinary LTP of the same differential-mode input range, the required  $(I_{SS}/K_n)$  factor is very small which implies that a reasonable common-mode input range can be obtained. However, the common-mode input range is still limited by the minimum

 TABLE I  
 THE ASPECT RATIOS OF THE TRANSISTORS USED IN FIG. 6

Transistor	Aspect Ratio
M1-M4	2.5/1.5
M5-M7b	5/3
M8-M9	0.5/1.5
M10-M11	1/1
M12-M13	5/3
M14	15/1.5
M15	54/1.5
M16	6/1.5
M17,M19	3/3
M18,M20	6/1.5
M21	1/9
M22	1/1

voltage of the common source of the differential pair [noted  $V_{S \min}$  in (5)] because of the current tail  $I_B$ .

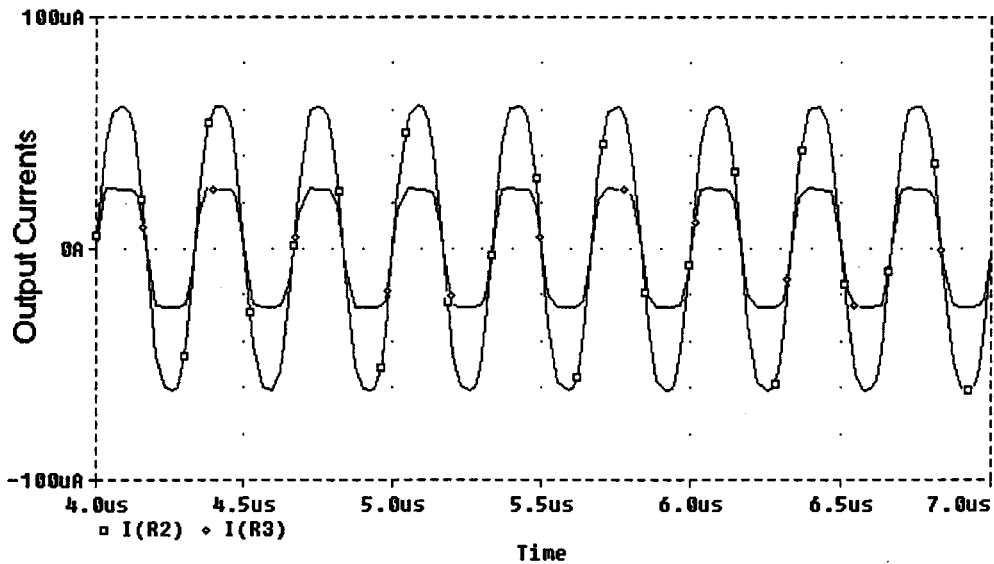


Fig. 6. The transient analysis of the output current of the EALTP when a sinusoidal voltage signal is applied at the input.

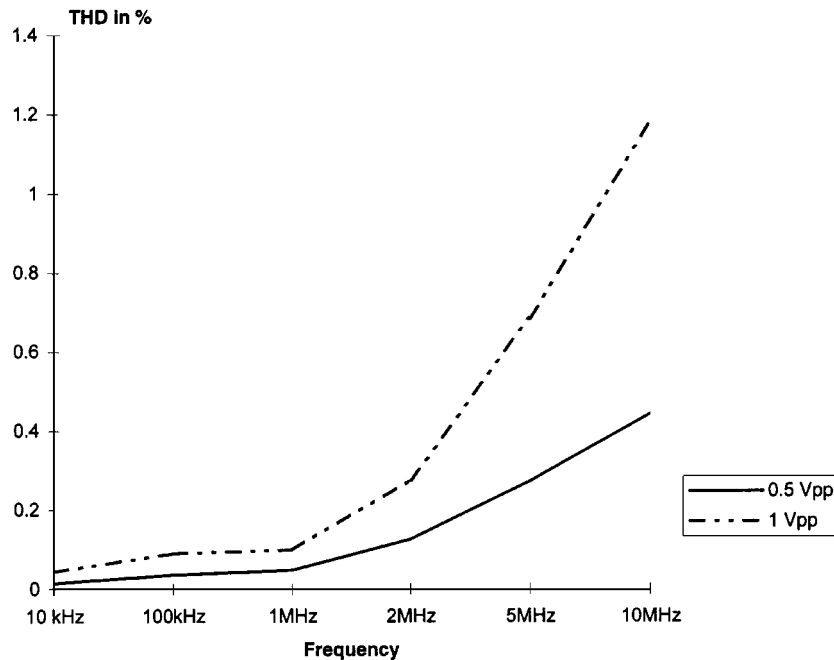


Fig. 7. THD of the output current of the EALTP versus frequency for the cases of  $0.5 V_{pp}$  and  $1 V_{pp}$ .

## V. PSPICE SIMULATIONS

Performances of both the squaring circuit shown in Fig. 2 and the linearized LTP shown in Fig. 3 are simulated using PSPICE. Transistors aspect ratios of the EALTP circuit shown in Fig. 4 are given in Table I and  $0.5 \mu\text{m}$  MIETEC CMOS process are assumed. Supply voltages used are given by:  $V_{DD} = -V_{SS} = 1.5 \text{ V}$ ,  $I_B$  is set to  $15 \mu\text{A}$  and  $I_x$  to  $0.5 \mu\text{A}$ .

Simulation results show that the squarer circuit gives a maximum percentage error with respect to the ideal value of about 2%. The main source of this error is the mobility reduction effect on transistors M14 and M15 which is technology dependent.

Fig. 5 shows the output current  $I_{OUT}$  for the linearized EALTP and for the ordinary LTP versus  $(V_1 - V_2)$ , which is scanned from  $-1.5 \text{ V}$

to  $1.5 \text{ V}$ . It is seen that the linearity range becomes very wide due to the new linearization technique and that the transconductance of the linearized LTP seems constant over a wide range.

Fig. 6 shows the transient response of the output current of the EALTP when a sinusoidal voltage signal of  $3 \text{ MHz}$  is applied at the input. Also simulation results showed that the  $-3\text{dB}$  frequency is about  $140 \text{ MHz}$ . Fig. 7 shows the THD of the output current of the EALTP versus frequency for the cases of  $0.5 V_{pp}$  and  $1 V_{pp}$ . Fig. 8 shows the THD of the output current of the EALTP and the ordinary LTP versus input voltage magnitude at  $1 \text{ MHz}$ . Simulation results show that the distortion level in the proposed EALTP is very low. This is obvious since the compensating technique clamps the voltage  $V_S$  to a level tracking the common-mode level of the signal. Hence, the mobility reduction factor is of very low value and a very low distortion level is obtained which characterizes antiphase common-source topologies [6].

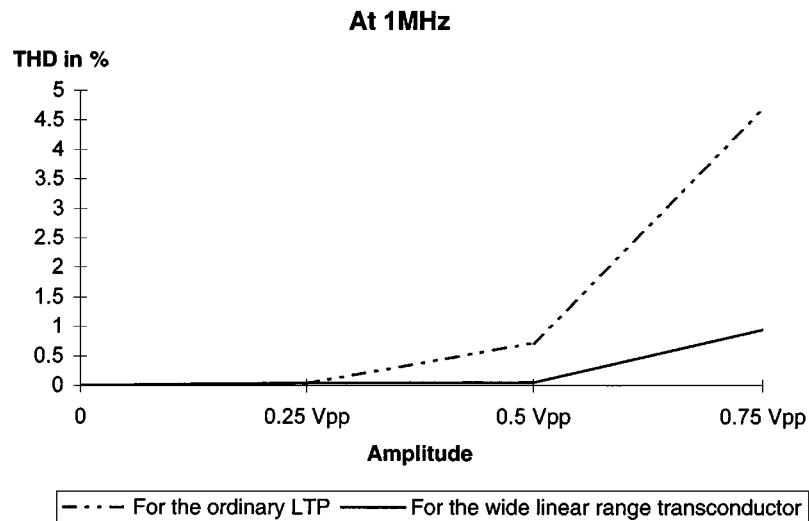


Fig. 8. THD of the output current of the EALTP and the ordinary LTP versus input voltage magnitude at 1 MHz.

## VI. CONCLUSION

A new linearization technique for the LTP has been proposed. The advantages of this new transconductor have been discussed. It has been shown that this circuit is a very attractive solution to overcome the restrictions that limited the use of LTP in many applications. Simulations results confirm the analysis, which makes this technique very suitable for analog signal processing.

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