

Generalized, Floating and Self Adjoint Differential Voltage Current Conveyor

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ABSTRACT

A new building block defined as the Generalized Differential Voltage Current Conveyor (GDVCC) with three Y inputs and three Z outputs is defined. The new building block has the simultaneous properties of being floating as well as a self-adjoint. The pathological representation of the GDVCC with its Nodal Admittance Matrix (NAM) stamp is given. The CMOS circuit realizing the GDVCC is also included. It is founded that among all the current conveyor (CCII) family included in this study the CCII- and the GDVCC are the only two elements that are floating as well as self adjoint.

Key words: Current conveyor, floating element, adjoint circuit theorem

INTRODUCTION

Over the last few years, the advantages of using current mode circuits have made the current-mode approach very attractive to analog circuit designers. One of the most versatile current-mode building blocks is the second-generation current conveyor (CCII) introduced in 1970 (Sedra and Smith, 1970). The inverting second-generation current conveyor (ICCI) was introduced in 1999 (Awad and Soliman, 1999) as a new block to complete the current conveyor family. Several CMOS realizations of the CCII and the ICCI are available in the literature. The simultaneous use of the CCII and ICCI has demonstrated high capabilities in analog circuit design (Soliman, 2010a, b).

The differential difference current conveyor with three Y inputs and one Z+ output was introduced by Chiu *et al.* (1996) as a universal building block. The differential voltage current conveyor with two Y inputs and balanced Z outputs (DVCC) has been independently introduced by Elwan and Soliman (1997). The DVCC includes the CCII with its two types CCII+ and CCII- as special cases. The DVCC includes also the ICCI with its two types ICCI+ and ICCI- as special cases. Due to the importance of floating elements in active circuits new floating CCII and ICCI have been introduced recently by Soliman and Saad (2009). The pathological representation of the DVCC and of the balanced output CCII (BOCCII) using nullor and mirror elements (Awad and Soliman, 2002) was given by Saad and Soliman (2010a). The adjoint network theorem (Bhattacharyya and Swamy, 1971) is applied to different types of CCII and ICCI as demonstrated by Awad and Soliman (1999). The NAM stamp (Haigh and Redmore, 2006; Haigh *et al.*, 2006) of the DVCC and of the BOCCII was given by Saad and Soliman (2010b) and the adjoint relations and the floatation status of different building blocks was given by Soliman (2009a, b).

In this study a review of different types of the DVCC is given with their pathological realizations. The NAM stamp and floatation status are also included.

DVCC WITH TWO Y INPUTS

Three types of the DVCC with two Y inputs are considered in this section.

Single Z-output DVCC (DVCC-): The DVCC-is shown symbolically in Fig. 1a and is defined by:

$$\begin{bmatrix} V_x \\ I_{Y1} \\ I_{Y2} \\ I_{Z-} \end{bmatrix} = \begin{bmatrix} 0 & 1 & -1 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ -1 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_x \\ V_{Y1} \\ V_{Y2} \\ V_{Z-} \end{bmatrix} \tag{1}$$

The DVCC-includes both the CCII- and ICCII- as special cases and they are all floating elements. The NAM stamp of the DVCC- is given by:

$$\begin{matrix} & X & Y_1 & Y_2 \\ X & \left[\begin{matrix} \infty_i & -\infty_i & \infty_i \end{matrix} \right] \\ Z- & \left[\begin{matrix} -\infty_i & \infty_i & -\infty_i \end{matrix} \right] \end{matrix} \tag{2}$$

The pathological representation of the DVCC-using two Voltage Mirrors (VM) and two norators is shown in Fig. 1b.

Table 1 includes the definition and the symbol of each of the four pathological elements that are used throughout the study.

Balanced Output DVCC (BODVCC): The BODVCC is shown symbolically in Fig. 2a and is defined by:

$$\begin{bmatrix} V_x \\ I_{Y1} \\ I_{Y2} \\ I_{Z+} \\ I_{Z-} \end{bmatrix} = \begin{bmatrix} 0 & 1 & -1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 \\ -1 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_x \\ V_{Y1} \\ V_{Y2} \\ V_{Z+} \\ V_{Z-} \end{bmatrix} \tag{3}$$

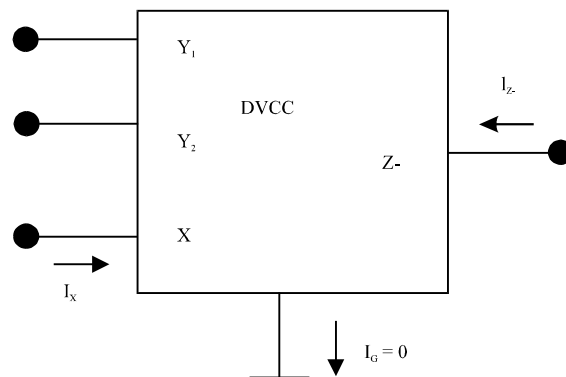
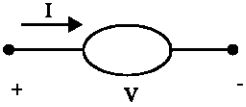
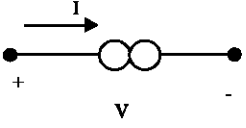
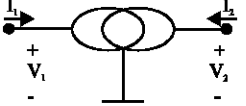
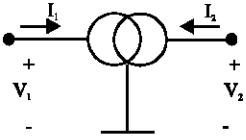


Fig. 1a: DVCC; symbol

Table 1: Summary of the definitions and symbols of the pathological elements

Symbol	Definition	Pathological element
	$V = I = 0$	Nullator
	V and I are arbitrary	Norator
	$V_1 = -V_2, I_1 = I_2 = 0$	Voltage mirror
	V_1 and V_2 are arbitrary $I_1 = I_2$ and they are also arbitrary	Current mirror

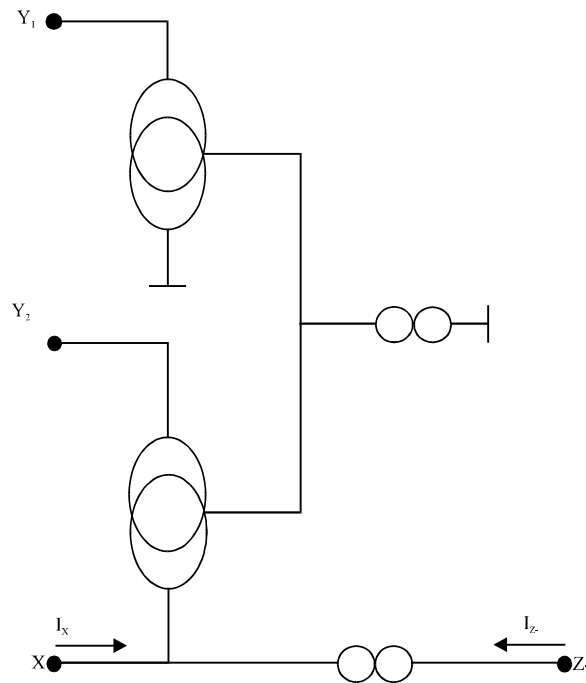


Fig. 1b: DVCC; Pathological representation

The pathological representation of the BODVCC using two-Current Mirrors (CM), two VM, one nullator and one norator is shown in Fig. 2b. It should be noted that the nullator and the norator used are dummy.

The NAM stamp for the BODVCC is given by:

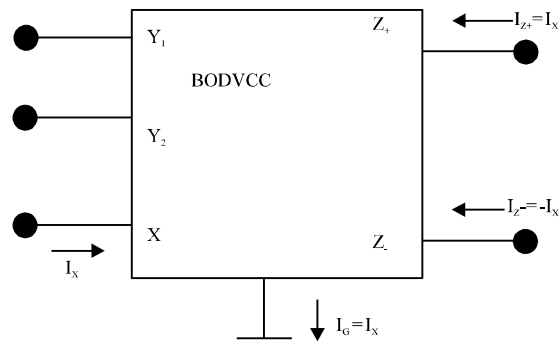


Fig. 2a: Symbolic representation of BODVCC

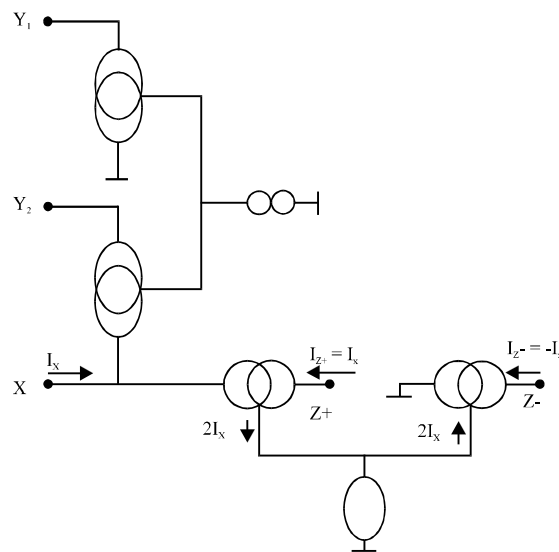


Fig. 2b: Pathological representation of the BODVCC

$$\begin{array}{c}
 \begin{array}{ccc}
 & X & Y1 & Y2 \\
 X & \left[\begin{array}{ccc}
 \infty_i & -\infty_i & \infty_i \\
 -\infty_i & \infty_i & -\infty_i \\
 \infty_i & -\infty_i & \infty_i
 \end{array} \right] \\
 Z- \\
 Z+
 \end{array}
 \end{array} \quad (4)$$

The above NAM is symmetrical indicating that the BODVCC is self-adjoint. It is seen however that the BODVCC is not a floating building block.

Floating DVCC (FDVCC): The FDVCC is shown symbolically in Fig. 3a and is defined by:

$$\begin{bmatrix} V_X \\ I_{Y1} \\ I_{Y2} \\ I_{Z+} \\ I_{Z1-} \\ I_{Z2-} \end{bmatrix} = \begin{bmatrix} 0 & 1 & -1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 & 0 \\ -1 & 0 & 0 & 0 & 0 & 0 \\ -1 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_X \\ V_{Y1} \\ V_{Y2} \\ V_{Z+} \\ V_{Z1-} \\ V_{Z2-} \end{bmatrix} \quad (5)$$

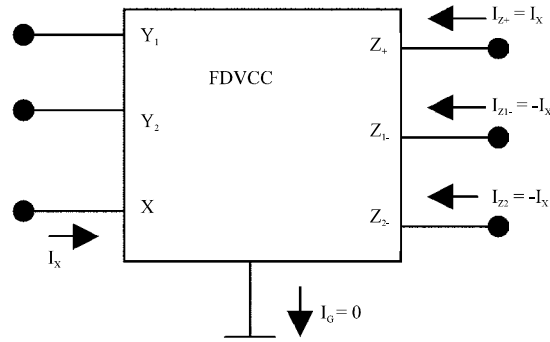


Fig. 3a: Symbolic representation of the floating DVCC

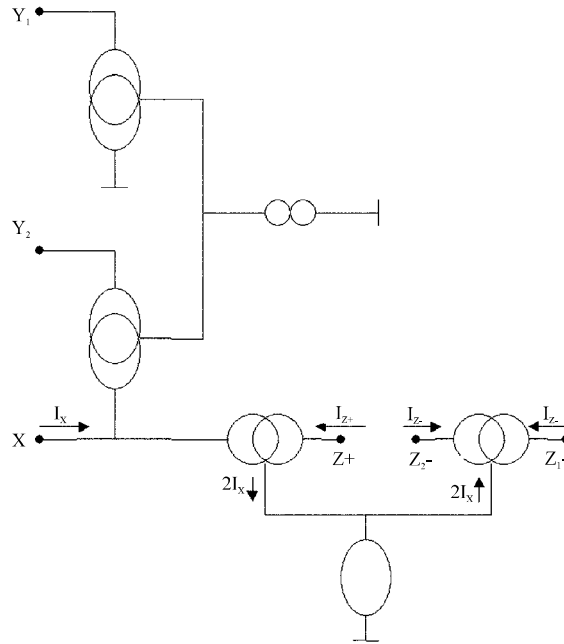


Fig. 3b: Pathological representation of the floating DVCC

The pathological representation of the FDVCC, which differs slightly from that of the BODVCC, is shown in Fig. 3b. The NAM stamp for the FDVCC is given by:

$$\begin{array}{c}
 \begin{array}{ccc}
 & X & Y1 & Y2 \\
 X & \left[\begin{array}{ccc}
 \infty & -\infty & \infty \\
 -\infty & \infty & -\infty \\
 \infty & -\infty & \infty \\
 -\infty & \infty & -\infty
 \end{array} \right] \\
 Z1- & & & \\
 Z+ & & & \\
 Z2- & & &
 \end{array}
 \end{array} \quad (6)$$

The above NAM indicates that the FDVCC is not self-adjoint. It is seen however that the sum of the elements in each column is zero indicating that the FDVCC is a floating building block.

GDVCC WITH THREE Y INPUTS

The GDVCC is shown symbolically in Fig. 4a and is similar to Fig. 3a except that it has a third noninverting Y input. The voltage at terminal X is related to the three inputs at terminals Y by:

$$V_X = V_{Y1} - V_{Y2} + V_{Y3} \tag{7}$$

The currents at the Z terminals are related to the current at terminal X by:

$$I_{Z+} = I_X, I_{Z1-} = I_{Z2-} = -I_X \tag{8}$$

The NAM of the floating GDVCC is given by:

	X	Y ₁	Y ₂	Y ₃
X	∞	$-\infty$	∞	$-\infty$
Z ₋	$-\infty$	∞	$-\infty$	∞
Z ₊	∞	$-\infty$	∞	$-\infty$
Z ₋	$-\infty$	∞	$-\infty$	∞

(9)

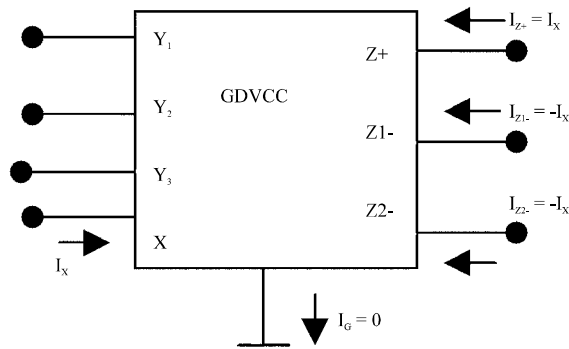


Fig. 4a: Symbolic representation of the floating GDVCC

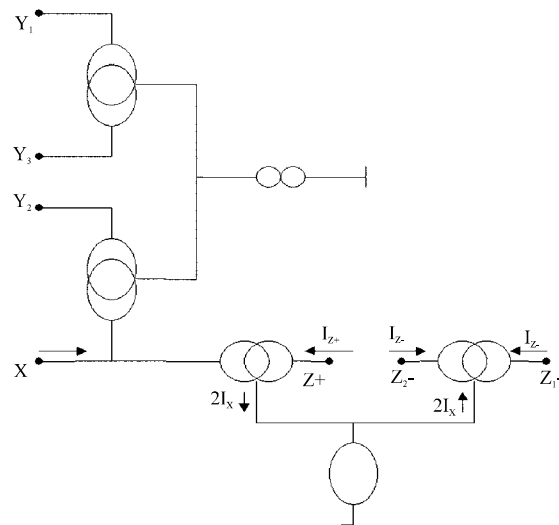


Fig. 4b: Pathological representation of the floating GDVCC

Table 2: Properties of different types of CCII, ICCII and DVCC

Floating	Self adjoint	Conveyor
Yes	Yes	CCII-
No	No	CCII+
Yes	No	Floating CCII
Yes	No	ICCII-
No	Yes	ICCII+
Yes	No	Floating ICCII
Yes	No	DVCC-
No	No	DVCC+
No	Yes	BODVCC
Yes	No	FDVCC
Yes	Yes	GDVCC

CCII is current conveyor, ICCII is inverting current conveyor and DVCC is differential voltage current conveyor, The + sign means positive and the - sign means negative

The above equation shows that the GDVCC is a self-adjoint and a floating building block.

The pathological realization of the GDVCC is shown in Fig. 4b and it includes two voltage mirrors and two current mirrors. The nullator and norator included are dummy elements as in Fig. 2b and 3b.

Table 2 summarizes the properties of different building blocks and it is seen that only the CCII- and the GDVCC shares being self-adjoint and floating at the same time.

CMOS REALIZATION OF FDVCC AND GDVCC

The CMOS circuit realizing both the FDVCC and the GDVCC as well is obtained directly from the well known DVCC (Elwan and Soliman, 1997) by adding the two MOS transistors M_{17} and M_{20} as shown in Fig. 5.

The transistor aspect ratios are given in Table 3 based on the 0.5 μm CMOS model from MOSIS. The supply voltages used are ± 1.5 V and $V_{B1} = -0.52$ V and $V_{B2} = 0.33$ V.

The FDVCC is obtained as special case from the GDVCC by grounding Y_3 .

APPLICATION

As an application of the FDVCC a floating gyrator is realized using two FDVCC and two resistors as shown in Fig. 6a. This circuit is a modification to the gyrator given (Elwan and Soliman, 1997) by using two FDVCC. The gyrator equations are given by:

$$V_1 = R_1 I_2 \quad \text{and} \quad V_2 = -R_2 I_1 \tag{10}$$

For equal resistors the gyrator will be ideal.

An alternative new floating gyrator is shown in Fig. 6b and is represented by the following equation:

$$V_1 = -R_1 I_2 \quad \text{and} \quad V_2 = R_2 I_1 \tag{11}$$

The gyrator circuit of Fig. 6b is used to realize a floating inductor of magnitude 0.253 m. H by taking $R_1 = R_2 = 1.59$ k Ω and terminating port 2 by a capacitor of 100pF. The floating inductor is

Table 3: Transistor aspect ratios of the GDVCC of Fig. 5

MOS transistors	W (μm)/L (μm)
M ₁ , M ₂ , M ₃ , M ₄	8/1
M ₅ , M ₆	8/1
M ₁₂ , M ₁₃ , M ₁₄ , M ₁₅ , M ₁₆ , M ₁₇	20/2.5
M ₇ , M ₈	10/1
M ₉ , M ₁₀ , M ₁₁ , M ₁₈ , M ₁₉ , M ₂₀	40/2

M_i : M is the Metal Oxide Semiconductor (MOS) transistor and i is its number in the CMOS circuit

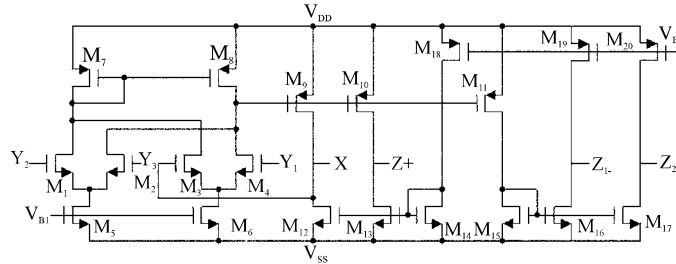


Fig. 5: CMOS circuit of the floating GDVCC; Y₁, Y₂ and Y₃ are the three high input impedance Y inputs. X is the low input impedance input. Z₊, Z₁₋ and Z₂₋ are the three Z output terminals. M₁ to M₂₀ are the MOS transistors

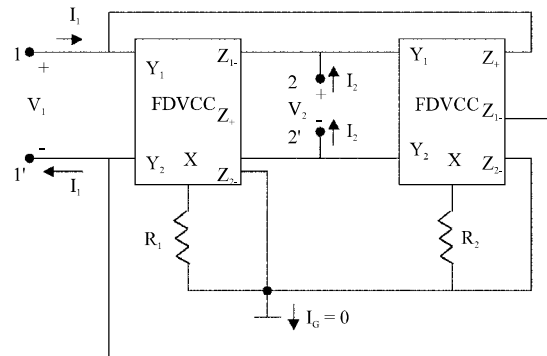


Fig. 6a: A floating gyrator using two FDVCC

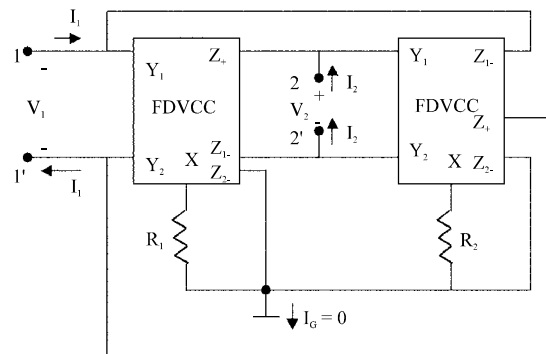


Fig. 6b: Alternative floating gyrator using two FDVCC

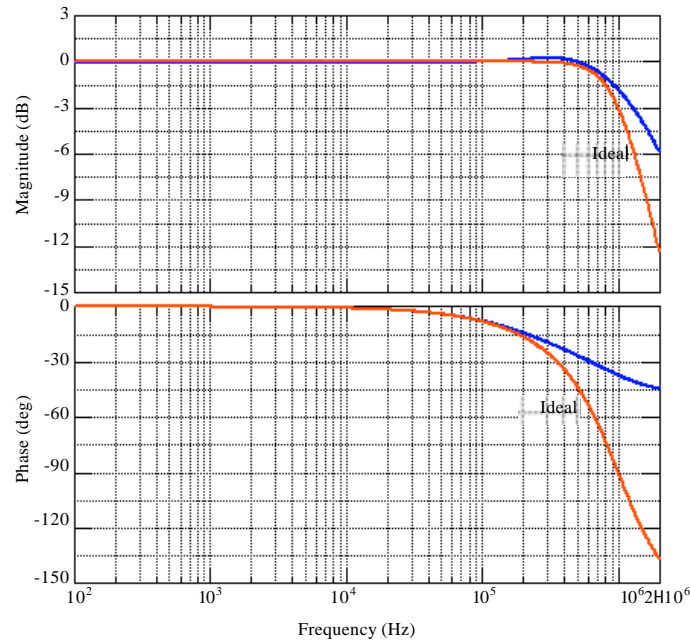


Fig. 7: Simulation results of a lowpass filter using gyrator of Fig. 6b. The red curve is the ideal response and the blue curve is the actual response

used to realize a maximally flat magnitude second order low-pass filter with cutoff frequency of 1 MHz using a series resistor of $R_s = 2.25 \text{ k}\Omega$ and C_s of 100 pF. Figure 7 represents the simulated magnitude and phase responses together with the ideal responses.

CONCLUSION

It is shown that the BODVCC introduced by Elwan and Soliman (1997) is a self adjoint building block but not floating. The FDVCC with two Y inputs and three Z outputs is defined as a new floating building block. The GDVCC with three Y inputs and three Z outputs is a self adjoint and a floating building block.

The pathological representation of the FDVCC and the GDVCC together with their NAM stamp is given. An application of the FDVCC in realizing a floating gyrator is included. The universal CMOS circuit realizing the FDVCC and the GDVCC is also included. Spice simulation results for the proposed floating inductor used in a lowpass filter is in good agreement with the ideal response. The NAM equations and the pathological realizations will be useful in the design automation of analogue integrated circuits (Amiri *et al.*, 2008; Chong *et al.*, 2007; Garcia-Ortega *et al.*, 2007; Masmoudi *et al.*, 2005; Tlelo-Cuautle *et al.*, 2010).

REFERENCES

- Amiri, M., N. Karimi and S.F. Jamshidi, 2008. A methodology for optimizing statistical multi-response problems using genetic local search algorithm through fuzzy goal programming. *J. Applied Sci.*, 8: 3199-3206.
- Awad, I.A., 1999. Inverting second generation current conveyors: The missing building blocks, CMOS realizations and applications. *Int. J. Electron.*, 86: 413-432.

- Awad, I.A. and A.M. Soliman, 2002. On the voltage mirrors and the current mirrors. *Analog Integrated Circuits Signal Proc.*, 32: 79-81.
- Bhattacharyya, B. and M. Swamy, 1971. Network transposition and its application in synthesis. *IEEE Trans. Circuit Theory*, 18: 394-397.
- Chiu, W., S.I. Liu, H.W. Tsao and J.J. Chen, 1996. CMOS differential difference current conveyors and their applications. *IEE Proc. Circuits Devices Syst.*, 143: 91-96.
- Chong, K.H., I.B. Aris, M.A. Sinan and B.M. Hamiruce, 2007. Digital circuit structure design via evolutionary algorithm method. *J. Applied Sci.*, 7: 380-385.
- Elwan, H.O. and A.M. Soliman, 1997. Novel CMOS differential voltage current conveyor and its applications. *IEE Proc. Circuits Devices Syst.*, 144: 195-200.
- Garcia-Ortega, J.M., E. Tlelo-Cuautle and C. Sanchez-Lopez, 2007. Design of current-mode Gm-C filters from the transformation of opamp-RC filters. *J. Applied Sci.*, 7: 1321-1326.
- Haigh, D.G. and P.M. Radmore, 2006. Admittance matrix models for the nullor using limit variables and their application to circuit design. *IEEE Trans. Circuits Syst.*, 53: 2214-2223.
- Haigh, D.G., T.J.W. Clarke and P.M. Radmore, 2006. Symbolic framework for linear active circuits based on port equivalence using limit variables. *IEEE Trans. Circuits Syst.*, 53: 2011-2024.
- Masmoudi, D.S., N.B. El Fek, S.B. Salem, M. Fakhfakh and M. Loulou, 2005. A high frequency CCII based tunable floating inductance and current-mode band pass filter application. *J. Applied Sci.*, 5: 1445-1451.
- Saad, R.A. and A.M. Soliman, 2010a. On the systematic synthesis of CCII based floating simulators. *Int. J. Circuit Theory Appl.*, 38: 935-967.
- Saad, R.A. and A.M. Soliman, 2010b. A new approach for using the pathological mirror elements in the ideal representation of active devices. *Int. J. Circuit Theory Appl.*, 38: 148-178.
- Sedra, A. and K. Smith, 1970. A second generation current conveyor and its applications. *IEEE Trans. Circuit Theory*, 17: 132-133.
- Soliman, A.M. and R.A. Saad, 2009. On the introduction of new floating current conveyors. *J. Circuits Syst. Comput.*, 18: 1005-1016.
- Soliman, A.M., 2009a. Adjoint network theorem and floating elements in the NAM. *J. Circuits Syst. Comput.*, 18: 597-616.
- Soliman, A.M., 2009b. On the DVCC and the BOCCII as adjoint elements. *J. Circuits Syst. Comput.*, 18: 1017-1032.
- Soliman, A.M., 2010a. Generation of CCII and ICCII based wien oscillators using nodal admittance matrix expansion. *AEU-Int. J. Electronics Communi.*, 64: 971-977.
- Soliman, A.M., 2010b. New CCII and ICCII based realizations of LC and LR mutators. *Circuits Syst. Signal Process*, 29: 1181-1191.
- Tlelo-Cuautle, E., I. Guerra-Gomez, M.A. Duarte-Villasenor, L.G. de la Fraga and G. Flores-Becerra *et al.*, 2010. Applications of evolutionary algorithms in the design automation of analog integrated circuits. *J. Applied Sci.*, 10: 1859-1872.