under a mismatch condition becomes $\lim_{t\to\infty} |\overline{x}'_R - \overline{x}_R| \leq \epsilon$ where ϵ is a vector of small numbers ($\epsilon_i \ll 1$ for all $i = 1, 2, \cdots, n$).

In this paper, instead of a formal mathematical study as outlined above, we examine the limits of parameter mismatch by computer simulations. Specifically, we keep the circuit parameters of the drive system unchanged and vary those of the response system one at a time. Table II shows the limits of parameter mismatch beyond which synchronization cannot be maintained. Both exact computer simulations and PSPICE simulations report the same findings.

VI. Conclusion

Power electronics circuits, due to their switching nonlinearity, exhibit a wide range of nonlinear and chaotic behavior. In recent years some results concerning bifurcations and chaos have been reported in power electronics systems and more are yet to be uncovered. In the nonlinear system literature, recent evidence of potential application in communication has aroused tremendous interest in chaos synchronization and dynamics of coupled systems. In this paper we consider, for the first time, power electronics circuits under a chaos synchronization context. We have shown in a simple drive-response connected system of chaotic power converters the possibility of synchronization. While any potential use of chaotic power converters remains uncertain, the present study provides a first evidence of synchronizing chaotic power converters. If power converters, apart from their normal power supply function, could be used to transmit messages, then future distributed power systems may serve the dual function of a power supply system and a medium of communication.

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Novel CMOS Current Feedback Op-Amp Realization Suitable for High Frequency Applications

Aly M. Ismail and Ahmed M. Soliman

***Abstract*—A novel CMOS current feedback operational amplifier (CFOA) is developed for wideband current-mode signal processing. The circuit has a very low input impedance over an exceptionally wide bandwidth and realizes an exact voltage-following action. Simulation results assuming 0.5-μm CMOS process shows that the impedance at the current input node is about 2 Ω and current and voltage transfer characteristics are extending beyond 180 MHz.**

***Index Terms*—CMOS circuits, current-feedback op amps.**

I. Introduction

In recent years, great interest has been devoted to the analysis and design of current-feedback and current-conveyor integrated circuits [1]–[9], mainly because these circuits exhibit better performance, particularly higher speed and better bandwidth, than classic voltage-mode operational amplifiers, which are limited by a constant gain-bandwidth product. The current-feedback operational amplifier (CFOA) is a four-port network with a describing matrix of the form

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \\ V_O \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \\ I_O \end{bmatrix} \tag{1}$$

Several CMOS realizations for the CFOA have been reported in the literature [1]–[4]. The CFOA has been always seen as an extension of the CCII, therefore, the design approach was to cascade a CCII+ with a voltage follower to realize the complete circuit [3]. The obtained bandwidth was always a degraded version of the CCII+ bandwidth. A very interesting analysis for CFOA stability in high-frequency application was given in [2] where the basic structure of the CFOA implemented in bipolar technology and shown in Fig. 1 is considered. It has been shown that the stability of the CFOA can be ensured by considering the two dominant poles due to the equivalent impedance at the node Z and due to the current mirror conveying the current from the node X to the node Z. Typically, the current mirror pole frequency is much higher than the pole frequency due to the transimpedance pole of the amplifier. However, because of economic constraints, the

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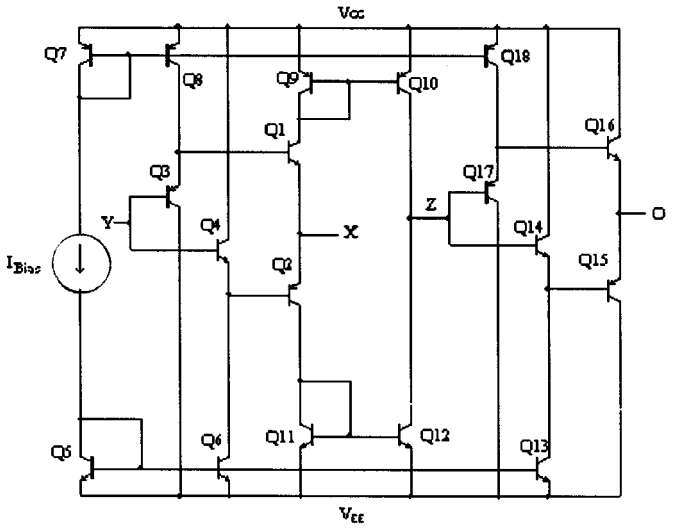

Fig. 1. The circuit configuration of the conventional CFOA in BJT reported in [1].

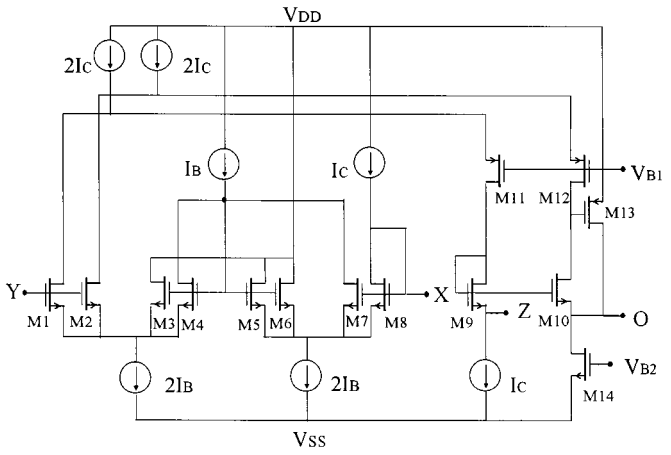

Fig. 2. The circuit configuration of the proposed CFOA.

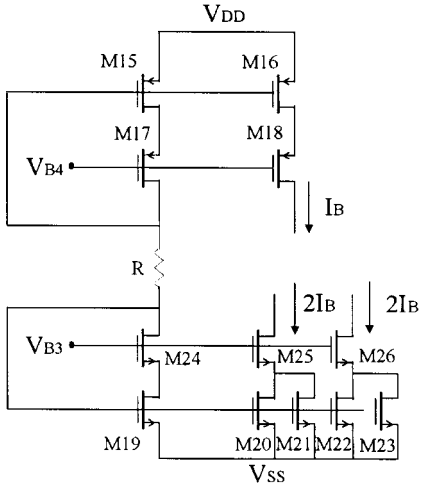

Fig. 3. The circuit configuration of the proposed biasing circuit.

standard digital CMOS technology is suited in implementing analog processing applications. When using the same architecture in CMOS technology, the current mirror pole frequency is significantly lowered due to the fact than the transconductance of the MOS transistor is relatively low and the capacitance seen at its gate is considerable. In addition, the voltage following action between node Y and node X, which is based on the translinear principle is not accurate enough when implemented in CMOS technology. To overcome this problem, several CMOS realizations for the CFOA have been reported in the literature based on an op amp-like architecture in the voltage following section between node Y and node X [3]. However, the use of a current mirror to convey the current from node X to node Z was unavoidable in these architectures. The floating current source proposed in [9] gives an elegant solution for this problem but only for the CCII$-$ circuits. So, as far as the authors know, no other realization that avoids current mirrors was reported for CCII$+$ and CFOA circuits. In this paper, a novel realization of the CFOA is presented. In this new architecture, current mirrors are completely avoided and high accuracy is obtained by merging all the terminals in one feedback-stabilized structure. Simulation results show the improvement gained from this new realization. In addition, a CFOA-based second-order notch filter is presented as an application.

II. The Circuit Description

The circuit configuration of the proposed CFOA is shown in Fig. 2. All transistors are assumed to be operating in the saturation region. M1–M8 are assumed to be matched as well as M9–M10. The negative feedback action on the gates of M3–M6 forces the sum of the currents flowing in M4 and M7 to equal I_B. Another negative feedback action applied from the drain to the gate of transistor M8 forces the two long tail structures M1–M4 and M5–M8 to follow the same differential voltage equivalent to the current driven from the node X. Therefore, the voltage at the node Y is reproduced successfully at the node X, irrespective of the driven input current. The high open loop gain obtained from the use of the two current tail structures with inherent local feedback minimizes significantly the input resistance at X as well as the offset voltage between v_Y and v_X [6]. It is therefore clear that the circuit provides the required high open loop gain in order to assure high voltage following action between node Y and node X by a feedback-stabilized topology. It should also be noted that the current flowing in transistors M1–M8 carry the information about the current flowing from node X, which can be of use to reproduce the current at node Z with no additional transistors. Indeed, the current flowing from X is reproduced on the source of M9 without the use of PMOS current mirrors, which improves the current following action between X and Z. Another replica of the current is forced to flow in M10 and the shunt-feedback transistor M13 is used in order to assure the voltage following action between Z and O. Transistors M11–M12 are used to isolate the drains of M1 and M2 from fluctuations of the voltages at the terminals Z and O. It is clear that the current following action is insensitive to the errors in the aspect ratios of M11–M12, which represents a major advantage over the use of conventional current mirrors. Also, it is noted that in the complete circuit, PMOS current mirrors are completely avoided since the PMOS mirrors gate and drain capacitances usually have a major role in bandwidth degradation. Therefore, the bandwidth extent is expected to be highly improved. Thus, the voltage-following action between Y and X, Z and O and the current-following action between X and Z are merged together in this special arrangement which makes the obtained bandwidth considerably wide since the current mirror pole mentioned before is replaced by other high –frequency poles. The major drawback in this topology is the need for several precise current sources, which represents the price paid for this bandwidth improvement. A proposed biasing circuit is shown in Fig. 3 that delivers the currents $2I_B$ and I_B. Similar circuits can be implemented to obtain the other required current sources in the circuit.

TABLE I
THE W/L OF THE TRANSISTORS OF THE CFOA CIRCUIT SHOWN IN FIG. 2

Transistor	Aspect Ratio
M1-M8,M9-M10	30/1
M11,M12	3/0.5
M13	6/0.5
M14	3/0.5

TABLE II
THE W/L OF THE TRANSISTORS OF THE BIASING CIRCUIT SHOWN IN FIG. 3

Transistor	Aspect Ratio
M15,M16	13/5.5
M17,M18	3.5/1
M19-M23	11/4.5
M24	3/1
M25-M26	3/.5

TABLE III
THE MODEL PARAMETERS SET OF 0.5 μm CMOS TECHNOLOGY
(OBTAINED THROUGH MIETEC)

```
**********************************************************
.MODEL NM NMOS LEVEL=3
+UO=460.5 TOX=1.0E-8 TPG=1    VTO=0.62  JS=1.08E-6
+XJ=0.15U RS=417       RSH=2.73  LD =0.04U  VMAX=130E3
+NSUB=1.71E17 PB=0.761 ETA=0.00 THETA=0.129  PHI=0.905
+GAMMA=0.69 KAPPA=0.10 CJ=76.4E-5 MJ=0.357  CJSW=5.68E-10
+MJSW=0.302 CGSO=1.38E-10 CGDO=1.38E-10     CGBO=3.45E-10
+KF=3.07E-28 AF=1 WD=+0.11U  DELTA=+0.42   NFS =1.2E11
+DELL =0U  LIS=2 ISTMP=10

.MODEL PM PMOS  LEVEL=3
+UO=100 TOX=1.0E-8  TPG=1 VTO=-0.58 JS=0.38E-6 XJ=0.10U
+RS=886 RSH =1.81     LD=0.03U VMAX=113E3 NSUB =2.08E17       +PB
=0.911 ETA=0.00  THETA=0.120 PHI =0.905 GAMMA=0.76
+KAPPA=2 CJ=85E-5 MJ=0.429 CJSW=4.67E-10  MJSW=0.631
+CGSO=1.38E-10 CGDO=1.38E-10  CGBO=3.45E-10 KF=1.08E-29
+AF=1    WD=+0.14U DELTA=0.81  NFS =0.52E11
+DELL=0U  LIS=2  ISTMP=10
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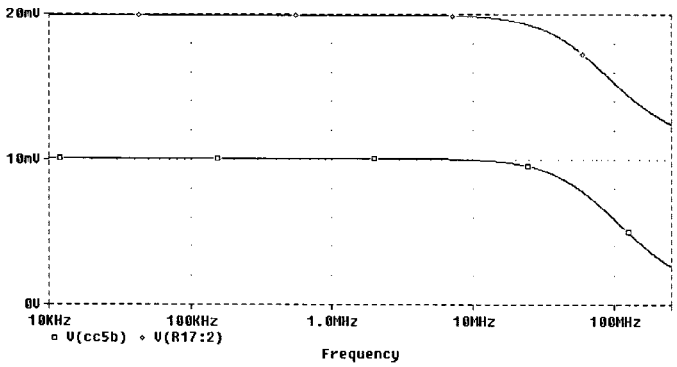

Fig. 4. The magnitude characteristics of the voltage transfer functions.

III. PSPICE SIMULATIONS

Performances of the CFOA shown in Fig. 2 are simulated using PSPICE. Transistor aspect ratios are given in Tables I and II and the 0.5-μm MIETEC CMOS process are assumed. The model parameters set of 0.5 μm CMOS Technology are given in Table III. The simulation work uses transistor-level current sources with the topology shown in Fig. 3. The supply voltages used are $V_{DD} = -V_{SS} = 2.5$ V, I_B and I_C are set to 60 μA and 10 μA, respectively.

The frequency characteristics of the voltage gain v_X/v_Y and v_O/v_Y when $R1 = 10$ kΩ is connected at X and $R2 = 40$ kΩ at Z is shown in Fig. 4. The performance of the proposed CFOA is excellent over a very wide range extending beyond 180MHz. Fig. 5 represents the simulated output voltage of the proposed CFOA resulting for an input voltage of magnitude 0.25 Vpp and of frequency 15 MHz (sinusoidal) with $R1 = 50$ kΩ and $R2 = 100$ kΩ.

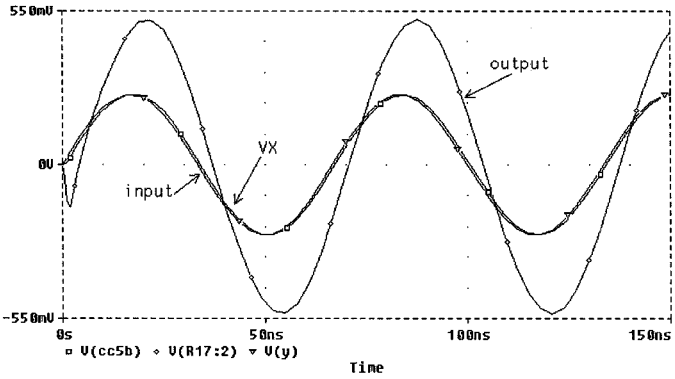

Fig. 5. The transient analysis of the output voltage when a sinusoidal signal is applied at the input.

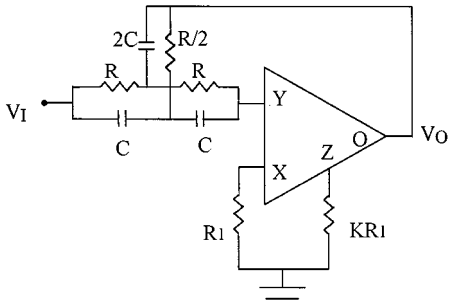

Fig. 6. The notch filter configuration.

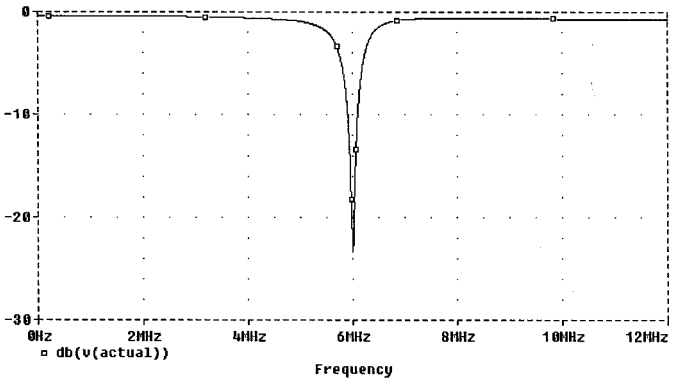

Fig. 7. The magnitude characteristics of the notch filter.

To demonstrate the practicality of the proposed CFOA in a circuit application, the notch filter shown in Fig. 6 [6] was designed for $Q = 5$ by taking $K = 0.95$ and $f_O = 6$ MHz. Fig. 7 represents the simulated magnitude response.

IV. CONCLUSION

A novel CFOA implementation with exceptional performance has been presented. The new circuit implemented in CMOS technology is designed in order to improve the frequency response. Simulation results have shown that their performances are excellent, which makes them very suitable to be used in high frequency analog signal processing applications.

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A Recurrent Neural Network for Online Design of Robust Optimal Filters

Danchi Jiang and Jun Wang

***Abstract*—A recurrent neural network is developed for robust optimal filter design. The purpose is to fill the gap between the real-time computation requirement in practice and the computational complexity of the filter design in the case that the statistical properties of noise are unknown. First, an H_∞ requirement and an L_2 requirement of filter design problem are formulated as a group of linear matrix inequalities. On this basis, an optimization problem is introduced to solve the robust optimal filter design problem. Then, a recurrent neural network is deliberately developed for solving the optimization problem in real time. The effectiveness and efficiency of the recurrent neural network is shown by use of theoretical and simulation results.**

***Index Terms*—Filter design, neural networks.**

I. Introduction

One fundamental problem in signal processing is the linear filter design. The objective is to retrieve the original signal source passing through a given linear channel corrupted by noise from its measured output. Such a channel can be modeled as a linear system. The celebrated Kalman filter gives an elegant solution to this problem by solving a Riccati equation in the case where the noise is known to be white. The Kalman filter is optimal in the sense that the energy of the estimation error is minimized. In the cases that the statistical property of the noise is unknown, such a design method cannot be applied. Instead, an H_∞ optimal filter design method is desirable to minimize the H_∞ norm of the filter from the noise to the estimation error over any possible noise with a finite energy. Such a filter is guaranteed to have a good performance with respect to the worst exogenous noise.

An H_∞ optimal filter is, however, conservative because a good performance with respect to the worst case noise does not imply a good performance in other cases. In many cases, the L_2 gain is required to be bounded by a prescribed positive real number instead of being minimized in the filter design [1]–[5]. For a given bound of the L_2 gain, a filter can be constructed by solving an appropriate Riccati equation involving this bound, as known in the literature such as [1]–[4]. However, an appropriate H_∞ bound is generically difficult to determine. It is of interest to develop a method that does not depend on a given H_∞ bound. Other methods may need the solution of a linear matrix inequality (see [5]) which involves extensive numerical computation and can only be computed off line. In many real-time applications, such as the mobile telephone or some other remote receivers of communication systems, a strong computation power is not equipped. In such circumstances, it is desirable to design satisfactory filters in real time using limited computation resources.

In recent years, neural networks become powerful tools for real-time computation of many optimization problems. Especially after Tank and Hopfield applied a neural network for linear programming [6], many results have been reported using recurrent neural networks for solving optimization problems, e.g., [7]–[11]. One of the main ideas is to build a recurrent neural network such that the state of the neural network represents the decision vector of the optimization problem and the dynamics of the neural network follows certain descent direction of the corresponding objective function. Furthermore, a recurrent neural network can be implemented using hardware such as an analog circuit, in which the steady state of the dynamics can be reached rapidly.

The objective of this paper is to develop a recurrent neural network for the filter design so that it has a good performance with respect to the worst case noise as well as to the noises in other cases. The present design method does not depend on a prescribed H_∞ bound. As the computation is carefully modulated to be realizable using a recurrent neural network, the proposed design method can be implemented on line with limited computation power. Specifically, an auxiliary cost function is introduced as the first step to combine the requirements on the H_∞ norm and H_2 norm with an adjustable weight. Then, a recurrent neural network is deliberately developed to minimize this cost function. Based on the optimal solution, a satisfactory filter can be easily designed. It is shown that the proposed recurrent neural network is convergent globally. The effectiveness and efficiency are analyzed theoretically and demonstrated using simulation results.

II. Preliminaries and Problem Formulation

Consider the following linear system:

$$\dot{x} = Ax + Ew \tag{1}$$

$$y = C_1x + D_1w \tag{2}$$

$$z = C_2x + D_2w \tag{3}$$

where $x \in \Re^n$ is the system state, w is the exogenous noise of the system which cannot be measured, y is the measured output, z is the signal to be estimated, and A, E, C_1, C_2, D_1, D_2 are known constant matrices. In the case where $C_2 = I$ and $D_2 = 0$, the estimation of the output z becomes the problem of state estimation.

The filter for this system is another linear system given as

$$\dot{\hat{x}} = A\hat{x} + K(C_1\hat{x} - y) \tag{4}$$

$$\hat{z} = C_2\hat{x}. \tag{5}$$

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