Analog Integrated Circuits and Signal Processing, 24, 141–152, 2000


# Current Operational Amplifier (COA): CMOS Realization and Active Compensation

**INAS A. AWAD AND AHMED M. SOLIMAN***

*Department of Electronics and Communications, Cairo University, Egypt*

Received April 28, 1998; Revised April 28, 1999; Accepted June 17, 1999

**Abstract.** A new COA-CMOS realization suitable for low-power designs is presented. The proposed design features a high performance in terms of input impedance, current tracking accuracy, DC offset and AC response. A new class AB output stage is used in order to enhance the slew rate as well as increase power efficiency. The active compensation of the COA based amplifiers is also discussed and the adjoint network theorem is used to generate the compensated circuits from their voltage mode counterparts.

**Key Words:** current mode circuits, current operational amplifier, active compensation

## 1. Introduction

Recently, a great importance has been placed on designing high performance current mode signal processing circuits [1]. These current mode circuits are receiving much attention for their potential advantages such as wide dynamic range, inherent wide bandwidth, simple circuitry and low-power consumption. The current operational amplifier (COA) is one of the useful current mode integrated building blocks. The attractive feature of the COA is its ability to replace the voltage operational amplifier (VOA) when applying the adjoint network theorem in voltage mode to current mode transformation [2,3]. The COA as the adjoint element to the VOA must be a single input differential output device as shown in Fig. 1(a), and it is defined as a floating current controlled current source (CCCS) with a high current gain, i.e., a current amplifier with a single low impedance current input and a complementary high impedance floating current output [4]. The same device definition was given in [5] but with another name: the operational current amplifier (OCA). A fully integrated version of the COA was given in [6] making use of current conveyors in order to implement the current buffer at the input of the COA and the floating output stage. A simple COA architecture was presented in [4] and was implemented using a current conveyor (CCII + ) input stage followed by a transconductance output stage with complementary outputs as shown in Fig. 1(b). In the previous design, a high output current tracking accuracy is achieved using the differential floating current source (FCS) output stage described in [7].

In this paper, a new COA-CMOS realization is presented. The proposed design uses a class AB floating output transconductor, hence, providing high power efficiency, enhanced slew rate and a high voltage swing at the output terminals. The performance of the proposed COA is evaluated and PSpice simulations are included. As in the voltage mode case, when the current mode amplifier is realized using the COA, the assumption of an ideal response is not valid except at low frequencies. The finite and complex open loop gain nature of the operational building block results in magnitude and phase errors. These errors are evaluated and the active compensation of the COA based amplifiers is discussed. Finally, phase compensated current mode amplifiers are presented.

## 2. The Proposed COA CMOS Realization

### *2.1. Circuit Description*

The proposed COA realization is based on the architecture shown in Fig. 2. This architecture is the same as that shown in Fig. 1(b) but after replacing the FCS output stage by a class AB floating transconductor (FT) in order to achieve a high-power efficiency and a low current consumption.

*Author for correspondence.

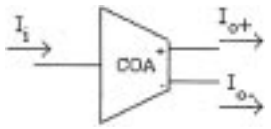



*Fig. 1(a).* The COA symbol.

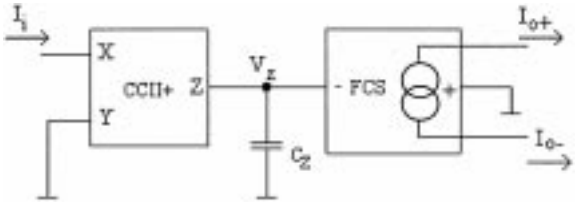



*Fig. 1(b).* The COA architecture presented in [4].

*2.1.1. The Input Stage.* Since the COA implementation uses a CCII + connected as a current follower, a simple CCII + realization is needed. However, the CCII + design must provide a high current tracking accuracy, low input impedance at port $X$ as well as high output impedance at port $Z$. The input and the output dynamic range of the CCII + are of less importance, since it will actually operate within a very small range when connected as the input stage of the COA. A possible class A CCII + CMOS realization is shown in Fig. 3(a). High voltage tracking accuracy between the Y and the X terminals is achieved by equating the currents flowing through the two matched CMOS pairs $M_1$–$M_2$ and $M_3$–$M_4$. These currents are given by:

$$I_{D1} = I_{D2} = K_{eff\,1,2}(V_{G1} - V_Y - V_{Teff})^2 \tag{1}$$

$$I_{D3} = I_{D4} = K_{eff\,3,4}(V_{G3} - V_Y - V_{Teff})^2 \tag{2}$$

where

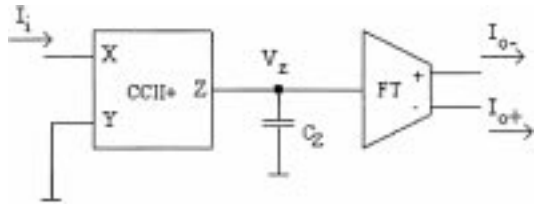
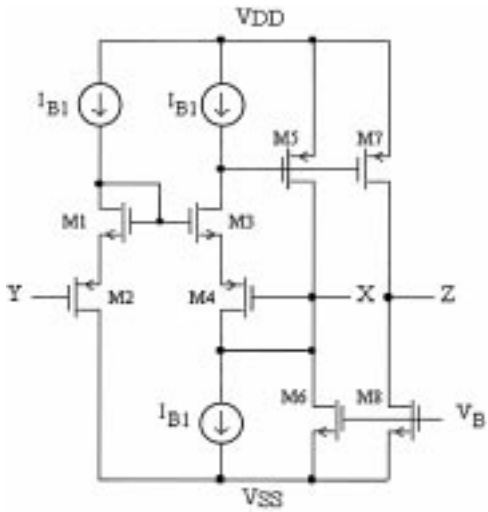



*Fig. 2.* The proposed COA architecture.



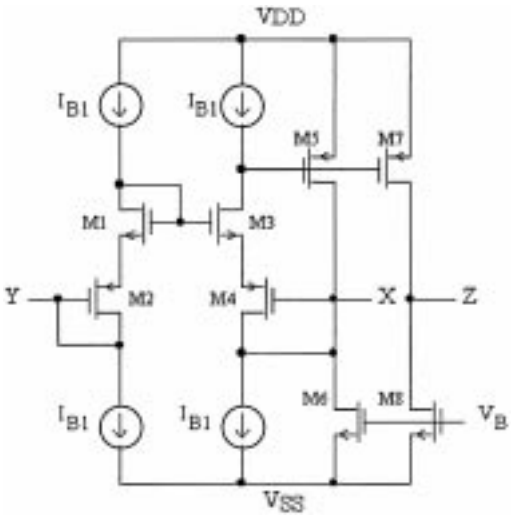




*Fig. 3.* Possible CMOS realizations of the CCII + forming the input stage of the proposed COA.

$$K_{eff\,i,j} = \frac{K_i K_j}{(\sqrt{K_i} + \sqrt{K_j})^2}$$

$$i = 1 \text{ or } 3,\ j = 2 \text{ or } 4 \tag{3}$$

$$K_i = \mu_n C_{ox}(W/L)_i \tag{4}$$

$$K_j = \mu_p C_{ox}(W/L)_j \tag{5}$$

and

$$V_{Teff} = V_{Tn} + |V_{Tp}| \tag{6}$$

$$I_{D1} = I_{D3} = I_{B1} \tag{7}$$

From equations (1)–(7) and since the gate voltages of $M_1$ and $M_3$ are equal, any voltage applied at the Y terminal will be transferred to the X terminal. The voltage buffering is achieved by connecting the gate of $M_4$ to its drain and by adding $M_5$, hence, any change in the input current to the node X will result into a change in the voltage at the drain of $M_3$ causing $M_5$ to supply this current change. The current buffering between the X and the Z terminals is provided using the matched transistors $M_5$–$M_7$ and $M_6$–$M_8$.

The proposed CCII+ realization features a small input impedance at the X terminal, which is dependent on the output impedance of the current source, connected at the drain of $M_3$. Neglecting the body effect, the small signal value of this impedance is given by:

$$r_X = \frac{g_B}{(g_{m4} + g_{d4})\,(g_{m5} + g_{d5})} \tag{8}$$

where $g_{di}$ is the output conductance, $g_{mi}$ is the transconductance with respect to $V_{gsi}$ of the $i$th transistor respectively, $g_B$ is the output conductance of the current source $I_{B1}$.

The DC voltage offset between the Y and the X terminal depends on the matching between the two CMOS pairs as well as their two biasing currents. Moreover, the channel length modulation results in a voltage offset as long as the drains of the two CMOS pairs have different voltages. This additional offset can be minimized by connecting the drain of $M_2$ to its gate as shown in Fig. 3(b). In order to make the input current to the Y terminal in the modified CCII+ circuit equal to zero, a current source equal to $I_{B1}$ is added at the Y terminal.

*2.1.2. The Output Stage.* The proposed COA realization uses a single input floating output transconductor as an output stage. This transconductor is responsible of providing two balanced output currents irrespective of its input voltage and with large voltage swing at the output terminals. The proposed realization is shown in Fig. 4. The current following property between the two output terminals is achieved using the four matched CMOS pairs $M_{13}$–$M_{14}$, $M_{15}$–$M_{16}$, $M_{17}$–$M_{18}$ and $M_{19}$–$M_{20}$. In order to satisfy Kirchhoff's current law at the drain of $M_{16}$, the two output currents must be equal. This is derived as follows:

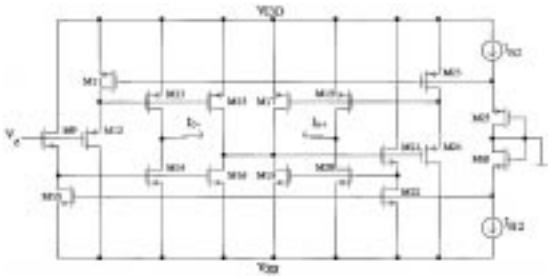


*Fig. 4.* The class AB floating transconductor used as the output stage of the proposed COA.

$$I_{D15} - I_{D16} = I_{D18} - I_{D17} \tag{9}$$

$$I_{o-} = I_{D13} - I_{D14} = I_{D15} - I_{D16} \tag{10}$$

$$I_{o+} = I_{D19} - I_{D20} = -(I_{D18} - I_{D17}) \tag{11}$$

From equations (9) to (11), it can be easily seen that $I_{o+}$ is equal to the negative of $I_{o-}$. This relation is valid as long as the four CMOS pairs are in saturation region. Referring to Fig. 4, the small signal current transfer gain between the two output currents is given by:

$$\frac{i_{o+}}{i_{o-}} = \frac{(g_{m_{19}} + g_{m_{20}})(g_{m_{15}} + g_{m_{16}})}{(g_{m_{13}} + g_{m_{14}})(g_{m_{17}} + g_{m_{18}})}$$

$$\left(\frac{-1}{1 + ((g_{d15} + g_{d16} + g_{d17} + g_{d18})/(g_{m_{17}} + g_{m_{18}}))}\right) \tag{12}$$

As given by equation (12), the current transfer gain depends on the equality of the transconductance gains of the four output CMOS pairs, and the ratio of the output impedance at the drain of $M_{15}$ to the transconductance gain of the CMOS pair formed by $M_{17}$–$M_{18}$. The matching between the output transistors can be achieved by using a careful layout technique. In this case, the current transfer gain is equal to:

$$\frac{i_{o+}}{i_{o-}} = \frac{-1}{1 + 2\Big((g_{d17} + g_{d18})/(g_{m_{17}} + g_{m_{18}})\Big)} \tag{13}$$

Since the output conductances of the transistors $M_{15}$ and $M_{16}$ can be made very small relative to their

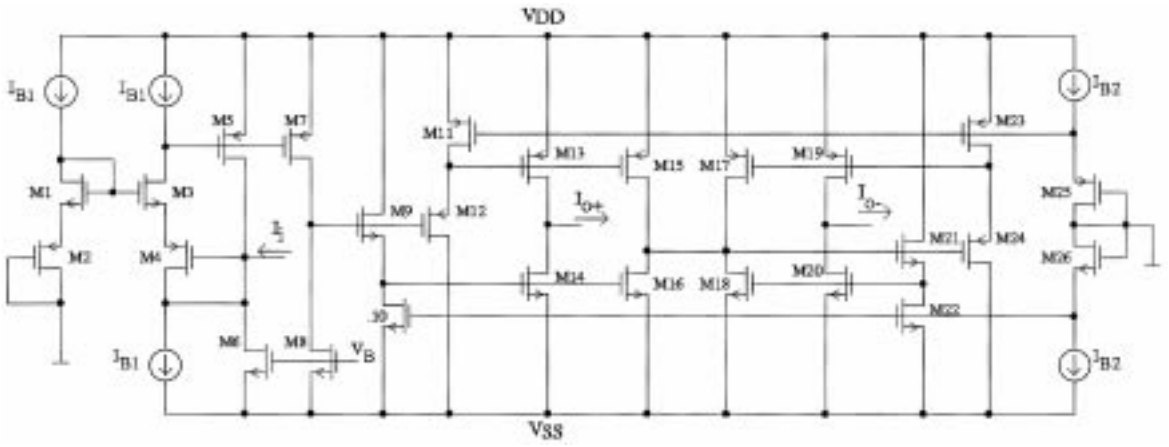



*Fig. 5.* The complete CMOS realization of the proposed COA.

transconductances, a current transfer gain very close to unity can be obtained.

In order to provide class AB operation, the difference between the two gate voltages of each CMOS pair is made constant and independent of the input voltage of the transconductor. This is achieved using the level shift transistors $M_9$–$M_{10}$, $M_{11}$–$M_{12}$, $M_{21}$–$M_{22}$ and $M_{23}$–$M_{24}$. The standby currents in the output transistors is controlled using $M_{23}$–$M_{24}$ and two current sources equal to $I_{B2}$. When the output current is equal to zero, the current flowing through $M_{13}$ is equal to that flowing through $M_{14}$ and it is given by:

$$I_{SB13} = I_{SB14} = \frac{K_{eff\ 13,14}}{K_{eff\ 25,26}}\ I_{B2} \tag{14}$$

Similarly, the standby current flowing through $M_{17}$ and $M_{18}$ is given by:

$$I_{SB17} = I_{SB18} = \frac{K_{eff\ 17,18}}{K_{eff\ 25,26}}\ I_{B2} \tag{15}$$

As given by equations (14) and (15), the standby currents are controlled by the aspect ratios of two different CMOS pair and a biassing current which can be chosen very small and hence reducing the power consumption.

For proper class AB operation, all output transistors must be ON at the standby point. This implies the following supply voltage condition:

$$V_{DD} - V_{SS} \geq 2V_{Tn} + 2|V_{Tp}| + \sqrt{\frac{I_{B2}}{K_{eff\ 25,26}}} \tag{16}$$

*2.1.3. The COA Parameters.* The input impedance of the COA is equal to that of the CCII+ used in the input stage and is given by equation (8). The two output impedances of the COA are given by:

$$R_{o+} = \frac{1}{g_{d13} + g_{d14}} \tag{17}$$

$$R_{o-} = \frac{1}{g_{d17} + g_{d18}} \tag{18}$$

The low frequency small signal open loop gain is given by:

$$A_o = \frac{i_{o+}}{i_i} = \frac{g_{m_{13}} + g_{m_{14}}}{g_{d7} + g_{d8}} \tag{19}$$

The common mode gain of the COA is evaluated using equation (13) and its low-frequency value is given by:

$$A_{o,cm} = \frac{i_{o+} + i_{o-}}{2\,i_i} = \frac{(g_{d17} + g_{d18})}{(g_{d7} + g_{d8})\,(1 + 2((g_{d17} + g_{d18})/(g_{m_{17}} + g_{m_{18}})))} \tag{20}$$

Equations (19) and (20) are used to calculate the common mode rejection ratio which is equal to:

$$\text{CMRR} = \frac{A_o}{A_{o,cm}} = 2 + \frac{g_{m_{13}} + g_{m_{14}}}{g_{d17} + g_{d18}} \tag{21}$$

The proposed configuration has one high impedance node which is the conveyor output node, hence, creating one dominant pole at the radian frequency:

$$\omega_p = \frac{g_{d7} + g_{d8}}{C_Z} \tag{22}$$

where $C_Z$ is the parallel combination of the CCII+ output capacitance at port Z and the floating transconductor input capacitance.

Hence, the gain-bandwidth product is given by:

$$\text{GBW} = \frac{g_{m_{13}} + g_{m_{14}}}{C_Z} \tag{23}$$

### 2.2. *Simulation Results*

PSpice simulations were carried out for the COA realization shown in Fig. 5 and realized using the CCII+ of Fig. 3(b) after removing the bias current between the Y terminal and the negative supply. The Y terminal is grounded in order to keep the COA input at a virtual ground. The COA output stage is realized using the floating transconductor of Fig. 4. The supply voltages were equal to $\pm$ 2.5 V, $I_{\text{B1}} = 3\,\mu$A and $I_{\text{B2}} = 4\,\mu$A. The transistors aspect ratios and circuit specifications are given in Table 1. The simulations were performed using model parameters of 1.2-$\mu$m n-well CMOS process provided by MOSIS (AMI) with $V_{Tn} = 0.64$ V, $V_{Tp} = -0.82$ V.

Fig. 6(a) shows the open loop DC transfer characteristics of the COA. The bias currents are realized using simple current mirrors, hence resulting in input offset current of 73 nA due to the channel length modulation effect. The input resistance is equal to 57 Ω. The variation in the output current offset $(I_{o+} + I_{o-})$ and the DC current gain $(I_{o-}/I_{o+})$ with respect to $I_{o+}$ are given in Fig. 6(b) and (c), respectively. A unity gain and a small current offset are shown over a wide range of the output currents. Fig. 6(d) and (e) illustrate the class AB operation by drawing the two components of each output current, a standby output current of 10 $\mu$A is obtained. Fig. 6(f) shows the open loop AC transfer characteristics of the proposed COA, a 3 dB frequency of 13 kHz and a unity gain frequency of 10 MHz were obtained. The plots of both the positive and the negative power supply rejection ratios ($\text{PSRR}_{V_{\text{DD}}}$ and $\text{PSRR}_{V_{\text{SS}}}$) are shown in Fig. 6(g). The compensation capacitor is connected to the negative supply voltage and so the dominant pole of the $\text{PSRR}_{V_{\text{SS}}}$ is placed much lower than the pole of the $\text{PSRR}_{V_{\text{DD}}}$.

The simulations have been carried out with the sources of the NMOS transistors connected to the negative supply while the sources of the PMOS transistors were connected to their corresponding bodies. This resulted in standby currents slightly larger than that given by equations (15) and (16) due to the body effect. However, this change is in the biasing circuit and causes no distortion on the class AB circuit.

*Table 1.* The transistors aspect ratios and circuit specifications of the proposed COA.

| Dimensions | | Specifications (at $\pm$ 2.5 V, $V_B = -1.8$ V, $I_{B1} = 3\,\mu$A $I_{B2} = 4\,\mu$A and $C_Z = 2.2$ pF). | | |
|---|---|---|---|---|
| Transistor | $W$ ($\mu$m)/$L$ ($\mu$m) | Parameter | Value | Unit |
| $M_1$, $M_3$ | 60/3.6 | $A_o$ | 62 | dB |
| $M_2$, $M_4$ | 120/3.6 | GBW | 10 | MHz |
| $M_5$, $M_7$ | 90/3.6 | $f_p$ | 13 | kHz |
| $M_6$, $M_8$ | 90/4.8 | Phase margin | 60 | degree |
| $M_9$, $M_{10}$, $M_{21}$, $M_{22}$ | 15/9.6 | $R_X$ | 58 | Ω |
| $M_{11}$, $M_{12}$, $M_{23}$, $M_{24}$ | 48/9.6 | Input current offset | 73 | nA |
| $M_{13}$, $M_{15}$, $M_{17}$, $M_{19}$ | 160.8/3.6 | Input voltage offset | − 2.4 | mV |
| $M_{14}$, $M_{16}$, $M_{18}$, $M_{20}$ | 42/3.6 | Standby current $I_{SB}$ | 10 | $\mu$A |
| $M_{25}$ | 80.4/3.6 | $R_{o+}$, $R_{o-}$ | 4 | MΩ |
| $M_{26}$ | 21/3.6 | $PSRR_{V_{dd}}$ | 151 | dB(Ω) |
| | | $PSRR_{V_{ss}}$ | 158 | dB(Ω) |

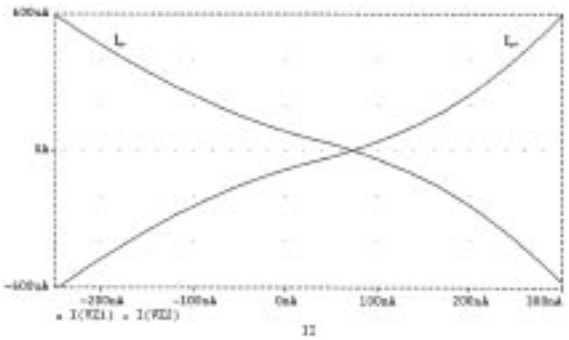


*Fig. 6(a).* The open loop DC transfer characteristics of the COA.

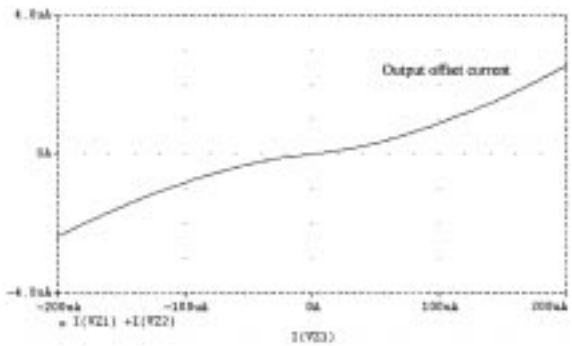



*Fig. 6(b).* The variation in the output current offset $(I_{o+} + I_{o-})$ versus $I_{o+}$.

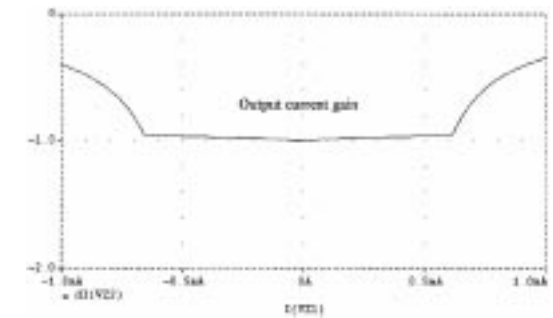



*Fig. 6(c).* The DC output current gain $(I_{o-}/I_{o+})$ versus $I_{o+}$.

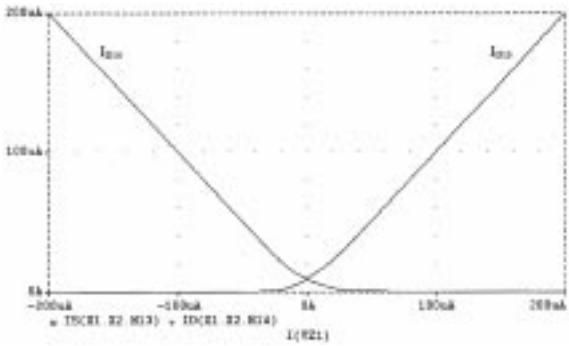


*Fig. 6(d).* The two current components forming $I_{o+}$ and flowing through $M_{13}$ and $M_{14}$.

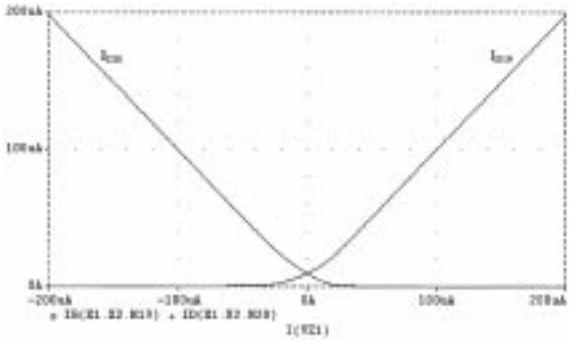


*Fig. 6(e).* The two current components forming $I_{o-}$ and flowing through $M_{19}$ and $M_{20}$.

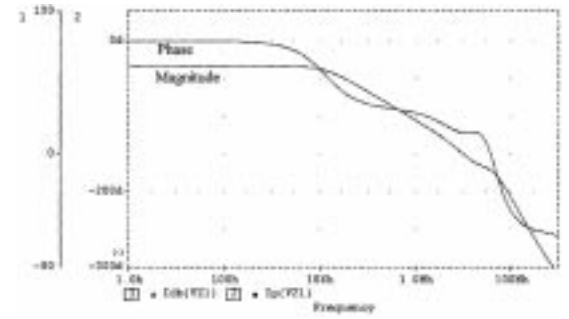



*Fig. 6(f).* The open loop AC transfer characteristics of the proposed COA.

The body effect also resulted in a voltage offset of-2.4 mV due to the inequality in the threshold voltages of $M_1$ and $M_3$. The channel length modulation also contributes to this offset, due to the difference between the voltages at the drains of $M_1$ and $M_3$, which results in a difference between the two bias currents flowing through the two transistors.

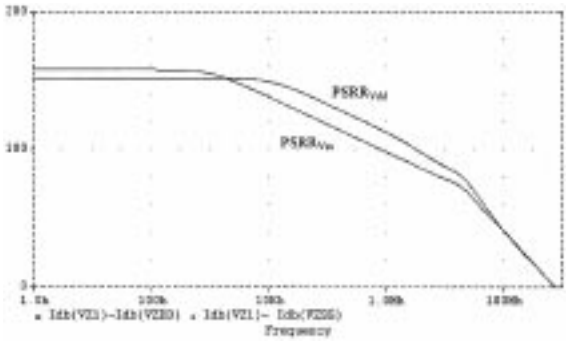



*Fig. 6(g).* The positive and the negative power supply rejection ratios of the COA.

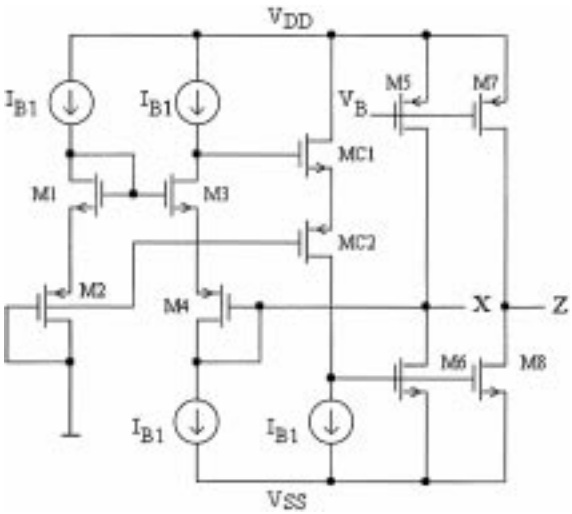



*Fig. 7(a).* Voltage offset compensated current follower.

### *2.3. The Modified COA Realization*

In order to cancel the voltage offset at the input of the COA, a compensation circuit is added to the current follower as shown in Fig. 7(a). The objective of this circuit is to maintain the drain of $M_3$ at the same level as that of $M_1$, hence, canceling the error between the two currents flowing through $M_1$ and $M_3$ due to the channel length modulation effect. This is achieved by matching the two CMOS pairs $MC_1$–$MC_2$ and $M_1$–$M_2$, and equating the two bias currents flowing through them. Since $M_2$ and $MC_2$ have the same gate voltage, the gate of $MC_1$ will be equal to that of $M_1$ using negative feedback. Hence, the drain of $M_1$ and $M_3$ will be equal for any value at the gate of $M_2$. Since $M_1$ and $M_3$ are matched transistors having the same gate and drain voltages as well as equal bias currents, their sources will be equal, hence, their threshold voltage will be equal and the voltage offset due to the body effect will be canceled.

Fig. 7(b) shows a modified version of the proposed COA with the compensation circuit. The biasing currents are obtained using high-swing cascode current mirrors [8] in order to minimize the offset currents. The same cascoding technique is used with $M_5$ and $M_7$ in order to increase the output impedance of the current follower and hence increasing the open loop gain of the COA.

The simulation results of the modified COA circuit are given in Table 2. Low-offset current is obtained, while the input resistance is reduced to 66 mΩ due to the gain added by the compensation circuit. Fig. 8(a) shows a comparison between the voltage offsets of the circuits of Figs. 5 and 7(b). The AC characteristics of

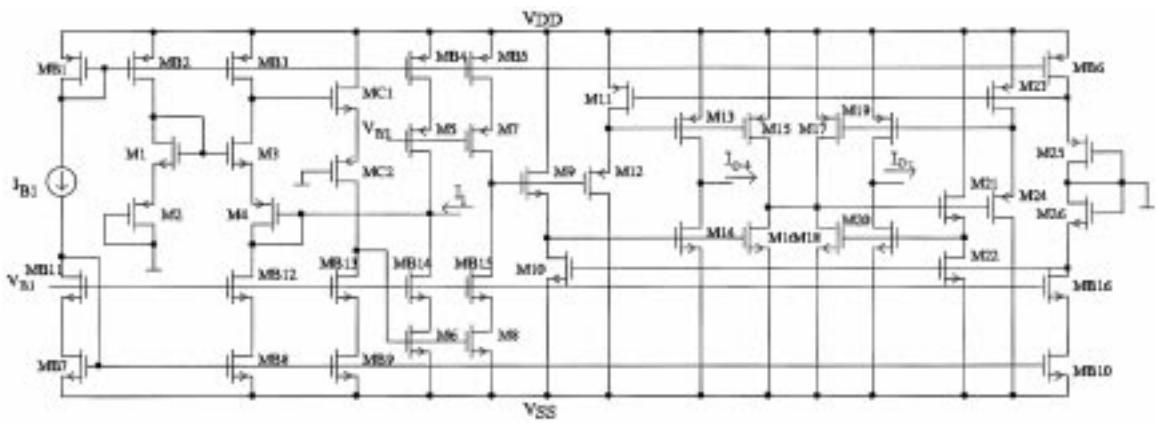



*Fig. 7(b).* The modified COA realization.

*Table 2.* The transistors aspect ratios and circuit specifications of the modified COA.

| Dimensions | | Specifications (at $\pm$ 2.5 V, $V_{Bi} = 3\,\mu$A, $V_{Bi} = -1.5$ V, $V_{B2} = 0$ V and $C_Z = 1$ pF). | | |
|---|---|---|---|---|
| Transistor | $W$ ($\mu$m)/$L$ ($\mu$m) | Parameter | Value | Unit |
| $M_1$, $M_3$, $MC_1$ | 60/3.6 | $A_o$ | 89 | dB |
| $M_2$, $M_4$, $MC_2$ | 120/3.6 | GBW | 19.9 | MHz |
| $M_5$, $M_7$, $MB_{14}$, $MB_{15}$ | 21/2.4 | $f_p$ | 1.3 | kHz |
| $M_6$, $M_8$, $MB_4$, $MB_5$ | 45/2.4 | Phase margin | 60 | degree |
| $M_9$, $M_{10}$, $M_{21}$, $M_{22}$ | 15/9.6 | $R_X$ | 66 | m$\Omega$ |
| $M_{11}$, $M_{12}$, $M_{23}$, $M_{24}$ | 48/9.6 | Input current offset | 0.3 | nA |
| $M_{13}$, $M_{15}$, $M_{17}$, $M_{19}$ | 160.8/3.6 | Input voltage offset | $-9$ | $\mu$V |
| $M_{14}$, $M_{16}$, $M_{18}$, $M_{20}$ | 42/3.6 | Standby current $I_{SB}$ | 10 | $\mu$A |
| $M_{25}$, $MC_{14}$ | 80.4/3.6 | $R_{o+}$, $R_{o-}$ | 4 | M$\Omega$ |
| $M_{26}$ | 21/3.6 | $PSRR_{V_{dd}}$ | 167 | dB($\Omega$) |
| $MB_1$, $MB_2$, $MB_3$ | 90/4.8 | $PSRR_{V_{ss}}$ | 169 | dB($\Omega$) |
| $MB_6$ | 90/3.6 | | | |
| $MB_7$, $MB_8$, $MB_9$ | 6/2.4 | | | |
| $MB_{10}$ | 12/3.6 | | | |
| $MB_{11}$, $MB_{12}$, $MB_{13}$ | 3/2.4 | | | |
| $MB_{16}$ | 6/3.6 | | | |

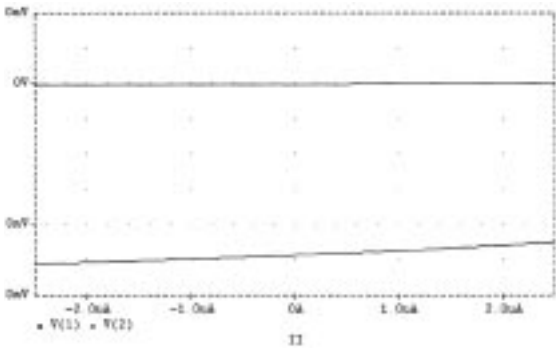


*Fig. 8(a).* The voltage offset cancellation obtained in the modified COA.

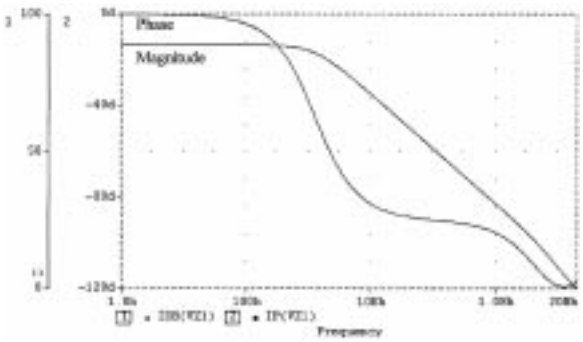



*Fig. 8(b).* The open loop gain of the modified COA.

the modified COA are shown in Fig. 8(b). The modified COA has higher open loop gain of 89 dB as well as higher unity gain frequency of 19.9 MHz.

## 3. Active Compensation of COA-Based Amplifiers

COA-based amplifiers can be obtained from their voltage mode counterpart using voltage mode to current mode transformation [2,3] as shown in Fig. 9. As in the VOA case, the assumption of an ideal COA response is not valid except at low frequencies. When the finite and complex open loop gain nature of each operational building block is considered, the transfer function of the COA-based noninverting amplifier shown in Fig. 9(b) is found to be similar to that of the VOA based noninverting amplifier shown in Fig. 9(a) as given by equations (24) and (25).

$$\frac{I_o}{I_i} = \frac{1+K}{1+(K+1)\,s/\omega_t} \tag{24}$$

$$\frac{V_o}{V_i} = \frac{1+K}{1+(K+1)\,s/\omega_t} \tag{25}$$

where $\omega_t$ is the unity gain radian frequency and $K$ is given by

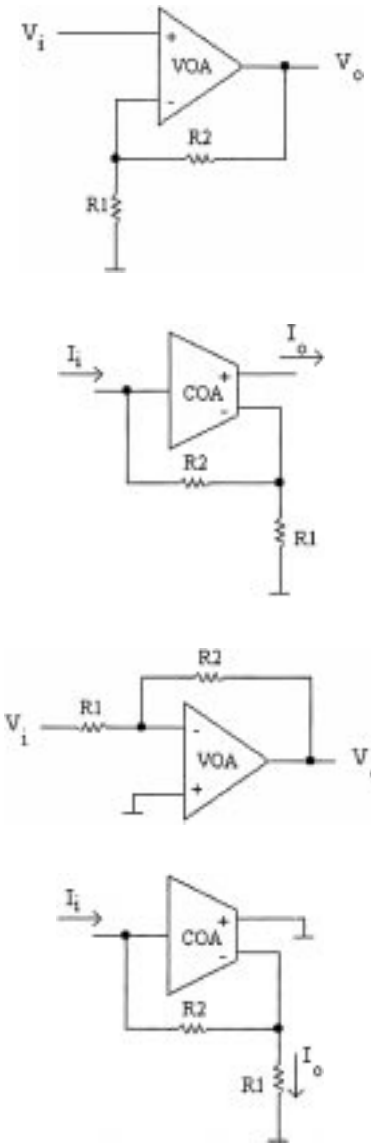



*Fig. 9.* The VOA-based amplifiers and their adjoint current mode amplifiers implemented using the COA.

$$K = \frac{R_2}{R_1} \tag{26}$$

Both the VOA and the COA noninverting amplifiers feature a constant gain-bandwidth property; i.e. the bandwidth is lowered when the DC gain is increased. Moreover, they suffer from phase and magnitude errors, which are given by:

$$\phi = -(K+1)\frac{\omega}{\omega_t} \tag{27}$$

$$\gamma = -\frac{1}{2}\left[(K+1)\frac{\omega}{\omega_t}\right]^2 \tag{28}$$

Many authors have investigated the active compensation of VOA-based amplifiers [9,10] in order to minimize these errors over a wide bandwidth and many high performance compensated circuits have been reported. In order to generate active compensated COA-based amplifiers, the adjoint transformation is applied to active compensated VOA based amplifiers. Since both circuits share the same transfer functions, the phase compensation condition is the same in both cases as well as the phase and magnitude errors and bandwidth. Hence, the generalized COA based active compensated noninverting amplifier is derived from the generalized VOA based active compensated noninverting amplifier given in [9] as shown in Fig. 10. The generated

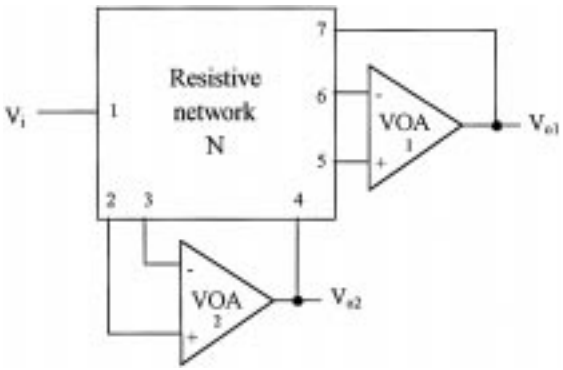



*Fig. 10(a).* The generalized VOA-based active compensated noninverting amplifier given in [9].

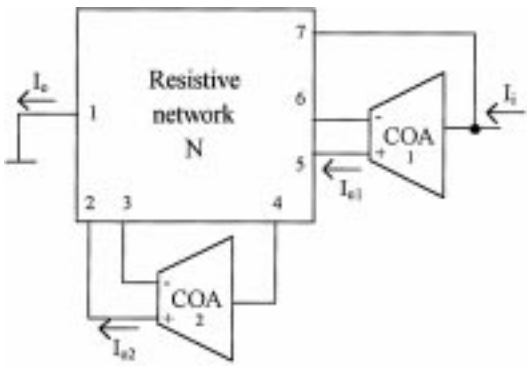



*Fig. 10(b).* The proposed generalized COA-based active compensated noninverting amplifier.

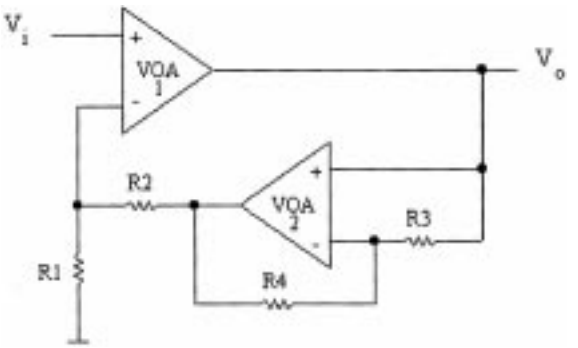



*Fig. 11(a).* The VOA-based active compensated noninverting amplifier given in [10].

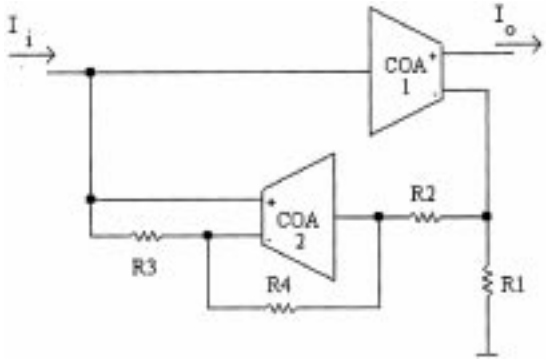



*Fig. 11(b).* The proposed COA-based active compensated amplifier.

current mode compensated amplifiers follow the same voltage mode classification.

As an example, the active compensated VOA-based noninverting amplifier given in [10] is used to obtain the COA-based compensated noninverting amplifier as shown in Fig. 11. Assuming matched COAs, the current mode transfer function is equal to that in the voltage mode case and is given by:

$$\frac{I_o}{I_i} = \frac{(1+K_1)[1+((1+K_2)\,s)/\omega_t]}{1+((1+K_1)\,s/\omega_t)+((1+K_1)\,(1+K_2)\,s^2/\omega_t^2)} \tag{29}$$

where

$$K_1 = \frac{R_2}{R_1} \tag{30}$$

and

$$K_2 = \frac{R_4}{R_3} \tag{31}$$

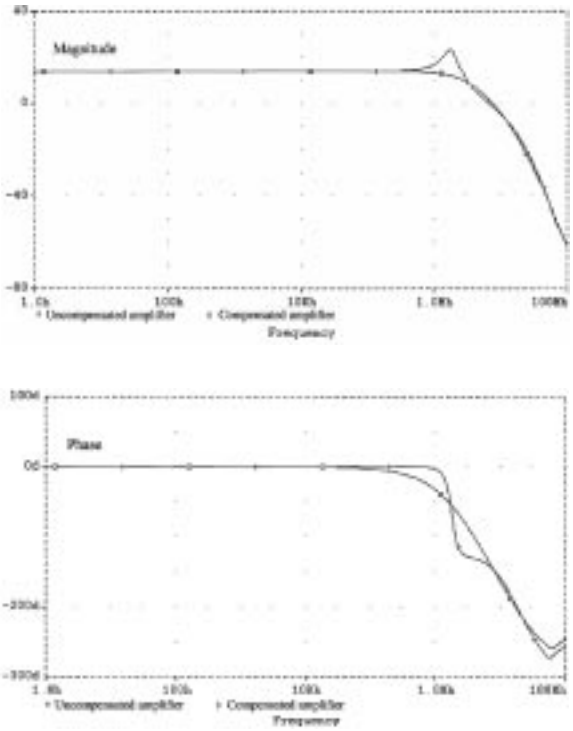



*Fig. 12.* The phase and magnitude responses of both the uncompensated COA-based noninverting amplifier shown in Fig. 9(b) and the compensated amplifier shown in Fig. 11(b).

The condition for phase compensation is given by:

$$K_1 = K_2 = K \tag{32}$$

The approximate phase and magnitude errors are given by:

$$\phi = -\left[(K+1)\frac{\omega}{\omega_t}\right]^3 \tag{33}$$

$$\gamma = \left[(K+1)\frac{\omega}{\omega_t}\right]^2 \tag{34}$$

Comparing equation (27) with (33), it is seen that the compensated amplifier features a significant reduction in the phase error.

PSpice simulations were carried out for both noninverting amplifiers; the uncompensated amplifier shown in Fig. 9(b) and the compensated amplifier shown in Fig. 11(b). The simulations are based on using the proposed COA-CMOS realization shown in Fig. 5. Resistors values of the compensated amplifier

are as follows: $R_1 = R_3 = 10\,\text{k}\Omega$ and $R_2 = R_4 = 40\,k\Omega$. The amplifier DC gain is equal to 5. The phase and magnitude responses are shown in Fig. 12. The phase correction achieved by the active compensated amplifier is shown in Fig. 12(a) while (b) illustrates the corresponding magnitude response.

Similarly, active compensated COA-based inverting amplifiers can be obtained by applying the adjoint transformation to their voltage mode counterparts and by satisfying the same compensation conditions.

## 4. Conclusion

New CMOS realization of the COA is presented. The proposed design is based on a current buffer followed by a balanced output transconductor. The output stage provides a class AB operation, hence, reducing the standby power and enhancing the slew rate of the COA. A modified version of the COA with enhanced performance is presented. A compensation circuit is used in order to cancel the voltage offset at the input of the COA. The active compensation of the COA-based amplifiers is discussed and it is shown that the active compensated current mode amplifiers can be obtained from their voltage mode counterparts using the adjoint transformation. This conclusion resulted from the similarity between the VOA and the COA in the gain nature and the constant gain-bandwidth feature. As an example a COA noninverting amplifier is presented and simulations results show the enhancement in phase response.

## References


1. G. W. Roberts and A. Sedra, ''All current mode frequency selective circuits.'' *Electron. Lett.* 5(12), pp. 759–761, 1989.
2. E. Bruun, ''A differential-input, differential-output current mode operational amplifier.'' *Int. J. Electronics* 7, pp. 1048–1056, 1991.
3. E. Bruun, ''A Constant-bandwidth current mode operational amplifier.'' *Electron. Lett.* 27, pp. 1673–1674, 1991.
4. E. Bruun, ''Bandwidth optimization of a low power, high speed CMOS current op amp.'' *Analog Integrated Circuits and Signals Processing* 7, pp. 11–19, 1995.
5. J. H. Huijsing, ''Design and applications of the operational floating amplifier (OFA): The most universal operational amplifier.'' *Analog Integrated Circuits and Signal Processing* 4, pp. 115–129, 1993.
6. T. Kaulberg, ''A CMOS current mode operational amplifier.'' *IEEE J. Solid-State Circuits* 28, pp. 849–852, 1993.
7. A. F. Arbel and L. Goldminz ''Output stage for current mode feedback amplifiers, theory and applications.'' *Analog Integrated Circuits and Signals Processing* 2, pp. 243–255, 1992.
8. M. Ismail and T. Fiez, *Analog VLSI: Signal and Information Processing*, McGraw-Hill, New York, pp. 254–255, 1994.
9. A. M. Soliman, ''Classification and generation of active compensated noninverting VCVS building blocks.'' *Int. J. Circuit Theory Applic.* 8, pp. 395–405, 1980.
10. A. M. Soliman and M. Ismail, ''Active compensation of op-amps.'' *IEEE Trans. Circuit. Syst.* CAS-26, pp. 112–117, 1979.


**Inas Awad** was born in Cairo, Egypt, in 1971. She received the Bachelor, the M.Sc. and the Ph.D. degrees in Electronics and Communications from Cairo University in 1994, 1997 and 2000, respectively. In 1995, she joined the department of Electronics and Communications, Cairo University, Fayoum-Campus as a teaching assistant and now she is an assistant lecturer at the same department. Her primary research interest is in analog circuits with particular emphasis on current-mode approach and low-voltage low-power CMOS designs.

**Ahmed M. Soliman** was born in Cairo, Egypt, on November 22, 1943. He received the B.Sc. degree with honors from Cairo University, Egypt, in 1964, the M.Sc. and Ph.D. degrees from the University of Pittsburgh, Pittsburgh, PA, U.S.A., in 1967 and 1970, respectively, all in electrical engineering.

He is currently Professor and Chairman Electronics and Communications Engineering Department, Cairo University, Egypt. From 1985 to 1987, Dr. Soliman served as Professor and Chairman of the Electrical Engineering Department, United Arab Emirates University, and from 1987 to 1991 he was the Associate Dean of Engineering at the same University.

He has held visiting academic appointments at San Francisco State University, Florida Atlantic University and the American University in Cairo.

He was a visiting scholar at Bochum University, Germany (Summer 1985) and with the Technical University of Wien, Austria (Summer 1987).

In 1977, Dr. Soliman was decorated with the First Class Science Medal, from the President of Egypt, for his services to the field of Engineering and Engineering Education.