A CMOS Norton Amplifier-Based Digitally Controlled VGA for Low-Power Wireless Applications

Hassan Elwan, Ahmed M. Soliman, and Mohammed Ismail, *Fellow, IEEE*

***Abstract*—A CMOS variable-gain amplifier (VGA) for use in the baseband section of integrated wireless receivers is presented. The VGA circuit is based on a new CMOS realization of the Norton transresistance amplifier. The proposed CMOS realization operates from a 3-V supply voltage with rail-to-rail swing and class AB input and output stages. The standby current of the class AB stages employed can be accurately controlled, leading to a low power consumption, nonslew-rate-limited response. The VGA circuit provides a precise process-independent gain control range of 30 dB with 1-dB gain step. The circuit uses current division techniques to provide an area-efficient 6-bit digital offset trimming capability. Experimental results from a test chip fabricated through MOSIS are provided.**

***Index Terms*—Low-power, Norton amplifier, VGA, wireless communications.**

I. Introduction

VARIABLE-GAIN amplifiers (VGAs) are employed in many applications in order to maximize the dynamic range of the overall system [1]–[3]. The VGA is typically employed in a feedback loop to realize an automatic gain control loop (AGC). An AGC is a key element in any portable communication system [4]. The function of the AGC loop is to automatically adjust the gain of the receive path so that the signal processed by the baseband circuitry appears to be of a constant level regardless of the actual signal strength received at the antenna. Recently, the trend of developing a fully integrated receiver implies the elimination of regular off-chip high-frequency intermediate-frequency (IF) filters and amplifiers [5]. Alternatively, other receiver architectures like the zero IF, low IF, and wide-band double conversion receiver are gaining acceptance [6]. Transceiver chips employing the previous architectures demand a VGA stage at the baseband section to relax the dynamic range requirement on the analog-to-digital converter used. One important requirement for the VGA circuit is to provide good linearity for a wide range of signal swing. This is necessary to maintain a good IIP3 figure for the receiver circuit. Although traditional VGA topologies based on high open-loop gain op-amps or operational transconductance amplifiers (OTAs) provide good linearity, they suffer from slew-rate limitations and finite gain bandwidth product. Such circuit limitations hinder a power-efficient wide-control-range VGA circuit realization specially for higher signal bandwidth. Third-generation wireless communication systems to be employed in the near future utilize wide-band code-division multiple-access (WCDMA) techniques [7], [8]. Thus, the transmitted signal is to be spread over a wider range of bandwidth. It is thus necessary to investigate new CMOS amplifier-based VGA structures with properties more tailored for future low-voltage low-power wireless architectures.

In this paper, a digitally controlled VGA circuit based on a new CMOS Norton transresistance amplifier is investigated. The proposed amplifier circuit operates from a 3-V supply in a class AB mode that provides a nonslew-rate-limited gain bandwidth independent response with small standby power consumption. The amplifier is used to realize a digitally controlled VGA circuit with 30-dB gain control range. By using current division techniques, an area-efficient 6-bit digital offset trimming terminal is provided. In Section II, the VGA requirements and comparisons with other amplifier-based VGA structures are given. The proposed low-voltage Norton amplifier realization is given in Section III. The realization of the VGA is discussed in Section IV. Extension of the design for fully differential operation is discussed in Section V. In Section VI, experimental and simulation results are provided.

II. VGA Design Requirements

In this paper, a new VGA circuit based on the Norton amplifier is presented. The use of the proposed circuit in integrated wireless receivers is then investigated. Fig. 1 shows an example of an integrated wireless receiver chain. The VGA in the baseband section is preceded by a low-pass antialiasing filter (AAF) to remove the out-of-band blockers and relax the linearity requirements. This filter also serves as a bandlimiting filter for the analog-to-digital converter used. In many cases, the AAF provides 6–12 dB of gain, which helps in relaxing the required input-referred noise of the VGA circuit. The output of the VGA is loaded by the large sampling capacitor of the data converter. The AGC servo loop of the receiver employs the digital portion of the chip in the feedback loop. The use of digital circuits allows more complex and precise AGC loop processing using digital signal-processing (DSP) software techniques. It is clear that a digitally controlled VGA would simplify the interface circuitry between the analog and digital parts of the receiver. The VGA is thus required to exhibit a robust digitally controlled

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H. Elwan and M. Ismail are with the Analog VLSI Lab, Department of Electrical Engineering, The Ohio State University, Columbus, OH 43210 USA.

A. Soliman is with the Electronics and Communications Department, Cairo University, Cairo, Egypt.

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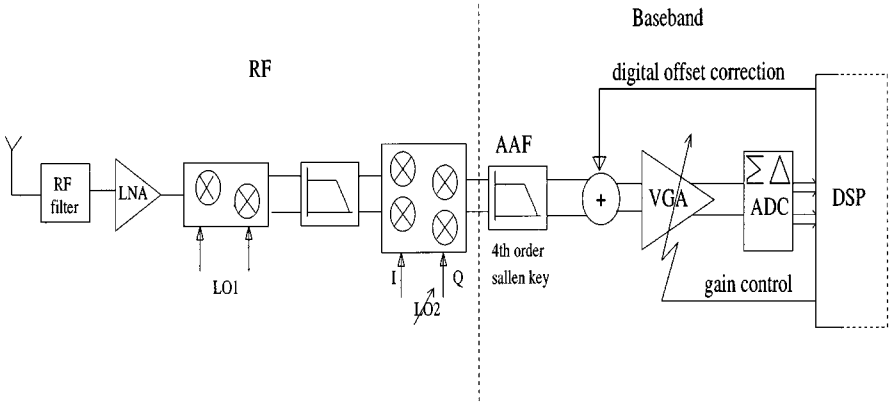

Fig. 1. Block diagram of a wide-band double conversion receiver.

dB-linear gain control characteristic with a precise gain step. An important consideration in VGA design is the dc offset compensation [10]. A small dc offset can be amplified by the VGA to a level that saturates the following stages or may cause the output signal to be clipped. Thus, dynamic compensation of the dc offset is an important part of the AGC loop design.

In the case of the receiver shown in Fig. 1, the digital portion of the chip determines the offset. This is accomplished by utilizing DSP algorithms that dynamically determines the dc offset associated with the signal. This is then fed back to the analog circuit and subtracted from the input signal before being amplified. Therefore, it is preferable for the VGA circuit to provide a digital offset trimming terminal as well. To achieve good linearity, a VGA circuit based on a high open-loop gain amplifier topology with a closed-loop gain set by a passive feedback network is usually preferred. The linearity of such VGA circuits can be increased by increasing the open-loop gain of the amplifier used. The VGA gain can then be programmed by changing the ratio of the feedback passive elements, resulting in an accurate and process-independent gain characteristic. A technique that utilizes the above principle is switched-capacitor amplifiers [11]. Those amplifiers provide high linearity and robust gain that is set by the ratio of the capacitors used. However, switched-capacitor-based VGA circuits suffer from a number of drawbacks. Being a sampled data system, the amplifier operates at a sampling frequency that is usually five to ten times higher than the bandwidth of the received signal; hence more power consumption is required. To prevent nonlinear distortion resulting from OTA slewing, a large biasing current is required that presents another factor that requires large standby power consumption. It can be shown that the power consumption of a regular folded cascode OTA increases linearly with sampling frequency and load capacitance. Furthermore, the finite gain bandwidth product of the OTA limits the gain control range achievable from a single stage and forces the use of a number of cascaded VGA stages to achieve the required gain control range. The problem of slew-rate limitation and finite gain bandwidth is also present in continuous-time op-amp-based VGA circuits. The drawbacks associated with classical amplifier-based VGA circuits will become more apparent when the receiver is required to process a wide-band signal in the baseband. Thus, it is required to find an amplifier-based VGA structure that is characterized by the following properties:

1) circuit properties that lend themselves naturally to low-voltage operation;
2) class AB operation to reduce the standby power consumption of the VGA;
3) gain that can be set independently of the bandwidth;
4) provide a voltage buffered output that can drive a large load capacitor without slewing.
5) rail-to-rail output swing capability to maximize the dynamic range;
6) digitally controlled gain and offset trimming;
7) fully differential operation.

As will be shown, a VGA circuit based on a low-voltage class AB Norton amplifier circuit realization satisfies the above requirements. It is worth noting that amplifier circuits based on the current feedback op-amp (CFOA) satisfies the gain-bandwidth and slew-rate requirements mentioned in points three and four. However, the CFOA is a four-terminal single-ended device with a voltage mode input stage based on single-ended buffers. Thus, the realization of fully differential VGA circuits using this technique is difficult. Furthermore, the voltage-based input stage design becomes much more complicated when low-voltage rail-to-rail operation is demanded.

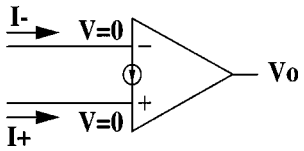

Fig. 2. The Norton amplifier symbol.

III. The CMOS Realization of the Norton Transresistance Amplifier

The Norton transresistance amplifier is a differential transresistance amplifier, as shown in Fig. 2. Its operation is described by

$$V_o = R_m(I_+ - I_-) \tag{1}$$

$$V_+ = V_- = 0 \tag{2}$$

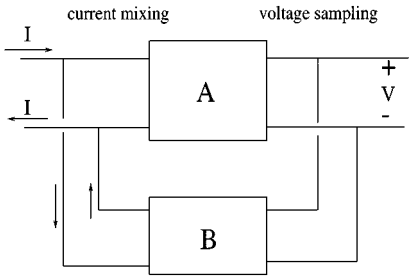

Fig. 3. Shunt–shunt amplifier feedback topology.

where R_m is the transresistance gain of the amplifier circuit and ideally should be infinite. By maintaining a larger transresistance gain and applying negative feedback, the amplifier circuit forces the two currents flowing through the input terminals to be equal. The voltage level of the input terminals is required to be held at virtual ground at all times (even without negative feedback). The input nodes should provide a low input resistance that is ideally equal to zero. The properties of the Norton amplifier circuit prove to be suitable for low-voltage circuit design. To illustrate this, consider the block diagram shown in Fig. 3. The diagram represents an amplifier circuit with gain A and a feedback network of gain B. For low-voltage operation, it is preferable to connect the two networks in parallel to get more headroom for signal swing [12]. Therefore, the most suitable feedback topology for low-voltage applications seems to be shunt–shunt, which leads to the conclusion that the amplifier circuit A should have a voltage signal at the output and current mixing at the input. Clearly, the Norton amplifier circuit satisfies this requirement. Although the Norton amplifier circuit definition was known for some time, problems with effective circuit realization prevented its use in integrated circuit design. Early commercial realizations of this amplifier used a class A input stage that utilizes the base emitter junction of bipolar transistors to realize the input virtual ground nodes of the amplifier [13]. This circuit realization requires an external dc biasing circuit to bias the input stage with the ac signal applied to the input terminal using coupling capacitors. The use of coupling capacitors and biasing circuits is not suitable for integration and leads to a complicated amplifier circuit. The class A input stage consumes large standby current and might limit the slew rate of the amplifier, as will be shown later. Furthermore, CMOS realization of the Norton amplifier using this concept results in a high-input-resistance virtual ground node because of the low MOS transconductance.

Recently, the developments in current-mode circuits [14], [15] led to a renewed interest in CMOS realization of the Norton amplifier [16]. While those circuit realizations are intended for use in CMOS integrated circuits, they require 5-V supply and provide a limited output voltage swing. Furthermore, the standby current of the input stage used is not controllable. The standby current is thus strongly process dependent and can be large. In some cases, the standby current can drop to zero, leading to crossover distortion. To realize an efficient VGA

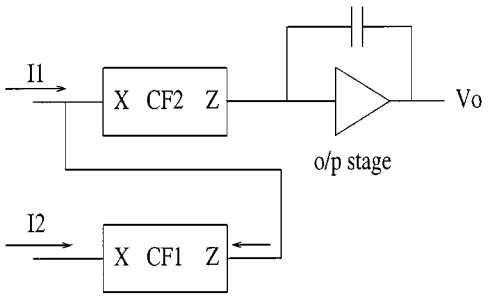

Fig. 4. Block diagram of the Norton amplifier circuit realization.

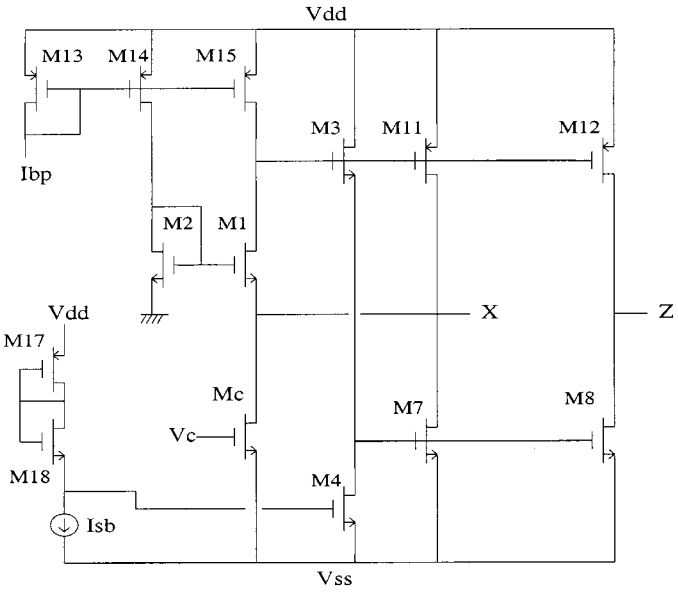

Fig. 5. The CMOS realization of the class AB current follower.

circuit based on a Norton amplifier, the CMOS realization of the amplifier should satisfy the following properties:

1) low-impedance accurate virtual ground input nodes;
2) class AB input stage with controllable standby current;
3) low-voltage operation with rail-to-rail output swing capability;
4) easy extension to handle fully differential signals.

The block diagram of the proposed Norton transresistance amplifier circuit is shown in Fig. 4. The circuit uses two cascaded current followers and an output stage. The current follower (CF) is a two-terminal block, described ideally as follows.

First, the output current I_Z always equals the input current I_X. Secondly, the input voltage V_X should always be zero, regardless of the magnitude of the input current. This implies that the input impedance looking into the x terminal should be zero. Finally, the output resistance of the current follower is ideally infinite. The input terminals of the current-follower circuit realize the two virtual ground low-impedance inputs of the Norton amplifier. The current from the output of the second current follower CF2 is the difference between the two input currents I_1 and I_2. This current is forced to flow through the high output resistance of the current follower circuit, and hence a high transresistance gain is realized. The buffered output of the amplifier is provided by an output stage. For stable operation, frequency compensation is necessary. Compensation is accomplished by

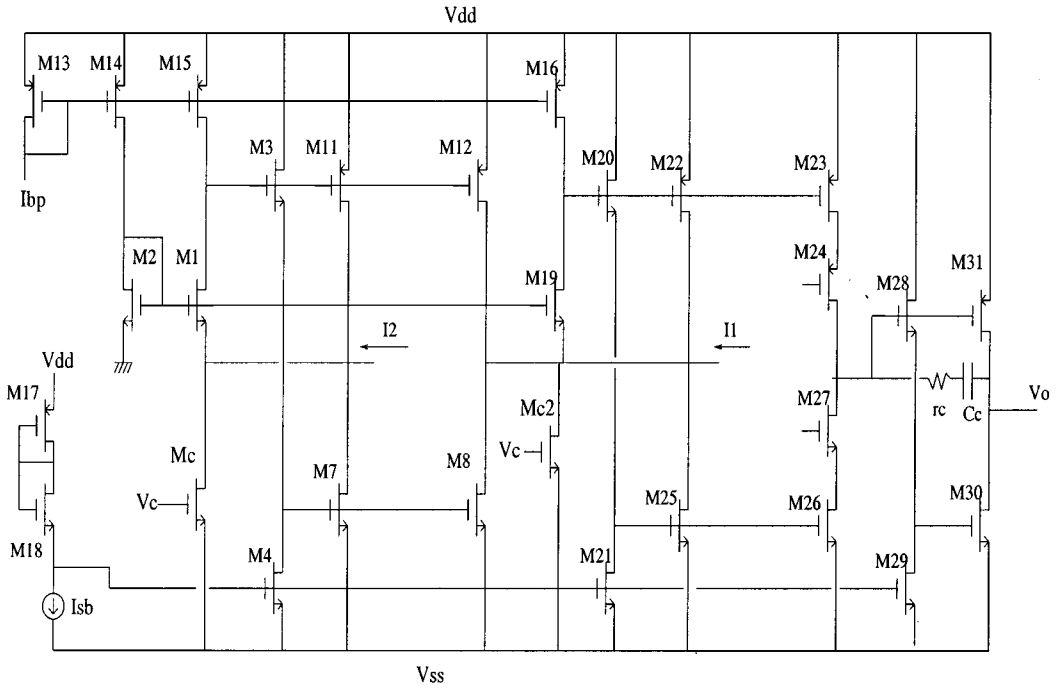

Fig. 6. Proposed circuit realization of the Norton amplifier.

using Miller compensation and an inverting rail-to-rail output stage. It is important to note that if a class AB current follower realization is used, a large current will be available to charge the compensation capacitance, leading to a nonslew-rate-limited response. Thus, the push–pull operation of the current follower is essential to provide a large current swing capability while maintaining a low standby power consumption.

The class AB current follower circuit used in realizing the Norton amplifier is shown in Fig. 5. The two biasing transistors M14 and M15 force an equal current through transistors M1 and M2. Since the gate voltages of transistors M1 and M2 are equal, the source voltage of transistor M1 equals the source voltage of M2, which results in a virtual ground node at the input terminal (the virtual ground voltage level is adjusted by V_b). The circuit utilizes a class AB loop to boost the transconductance of an MOS transistor operating in the saturation region. Hence, low input impedance can be achieved with low standby power consumption. The low input resistance of the current follower is provided by the action of the class AB negative feedback loop formed by transistors M3, M4, M7, and M11. The feedback loop operates in a class AB mode to minimize the standby power dissipation. The push–pull operation of the class AB input stage can be described by two translinear loop equations

$$V_{SG_{11}} + V_{GS_3} + V_{GS_7} = V_{dd} - V_{ss} \tag{3}$$

$$V_{SG_{17}} + V_{GS_{18}} + V_{GS_4} = V_{dd} - V_{ss}. \tag{4}$$

In standby mode, no current is withdrawn from the input terminal, and the current I_b is equal to the current flowing through Mc (which can be removed, as will be indicated later). Also, in standby mode, M7 and M11 have equal currents. Therefore

$$I_{M_7} = I_{M_{11}} = I_{sb}. \tag{5}$$

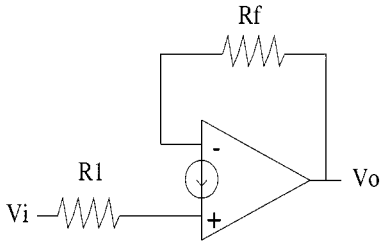

Fig. 7. Norton amplifier-based voltage amplifier.

The current from the input terminal is copied to the output terminal of the current follower by the mirroring action of transistors M7,M11 and M8,M12. The standby power consumption of the current follower circuit is thus

$$P_{SB} = V_{DD}\left(3I_{bp} + 3I_{sb} + \frac{K_4}{2}\left(V_{DD} - 2V_{Tn} + V_{Tp}\right)^2\right). \tag{6}$$

The last term in the previous equation is the current through the level shift transistors M3 and M4. This current can be kept small by choosing a small aspect ratio for M3 and M4. Transistor Mc can be removed, resulting in a shift in the standby operating point. Transistor M7 standby current is more than that of M11 by I_b. The small signal input resistance of the current follower circuit is approximately given by

$$r_x \simeq \frac{g_{d1} + g_{d15}}{g_{m1}(g_{m11} + g_{m7} + g_{ds1} + g_{d15})}. \tag{7}$$

The input resistance is reduced by the class AB negative feedback loop. Note that when the circuit is supplying current, the transconductance of M11 dominates and that of M7 is negligible. Similarly, when the circuit is sinking current, the transconductance of M7 dominates and M11 can be neglected.

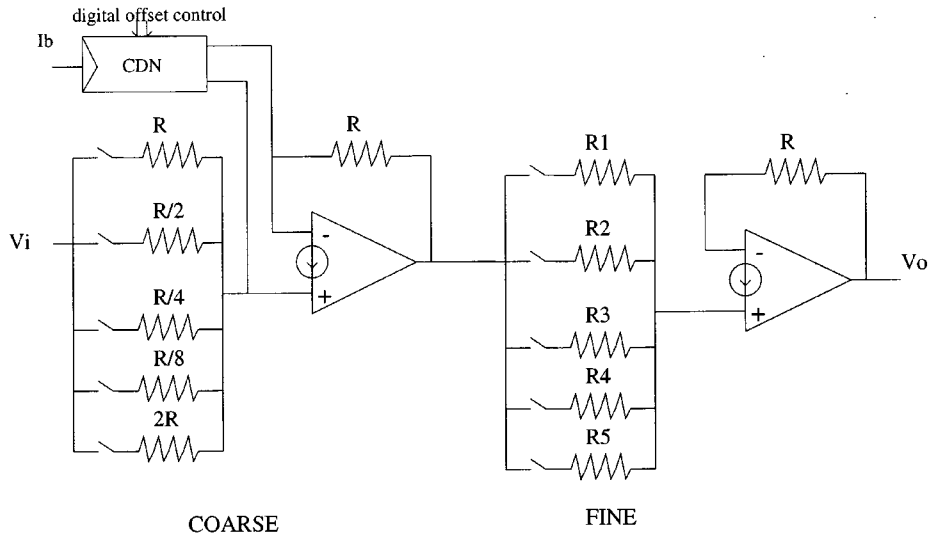

Fig. 8. Norton amplifier-based VGA with digital offset trimming.

The change of the input resistance will contribute negligible distortion if this change is kept reasonably low. Two current-follower circuits are used to realize the input terminals of the Norton amplifier. It is worth noting that for the current follower CF1, the drain voltage of the current mirroring transistors M7, M8 and M11, M12 of the input and output terminals are held at the same low-impedance virtual ground voltage level. Therefore, accurate current transfer, which is immune from channel length modulation errors, is maintained. Thus, the current mirroring transistors of this current follower do not need cascoding. On the other hand, the high output impedance terminal of the current-follower CF2 provides the required large transresistance gain of the Norton amplifier. The output stage of the amplifier uses a class AB push–pull circuit similar to that of the current follower. The complete Norton amplifier circuit is shown in Fig. 6. Miller compensation capacitance and resistance is connected between the input and output of this stage to compensate the Norton amplifier.

IV. The Digitally Controlled VGA Circuit

The Norton amplifier can be used to realize an amplifier circuit, as shown in Fig. 7. The gain of this amplifier is given by

$$\frac{V_o}{V_i} = \frac{R_f/R_1}{1+(R_f/R_M)}. \tag{8}$$

It is clear that by maintaining a high transresistance R_M, the gain of the amplifier will be determined by the ratio of the feedback resistor R_f and the input resistor R_1. At high frequencies, the transresistance is dominated by the Miller capacitance and the gain is given by

$$\frac{V_o}{V_i} = \frac{R_f/R_1}{1+(SC_{\rm eq}R_f)} \tag{9}$$

where $C_{\rm eq}$ is the total equivalent capacitance at the output of the current-follower CF2. The gain of the amplifier can be tuned independently of the bandwidth by changing the resistance R_1. A digitally controlled VGA can thus be obtained by using resistor arrays. The VGA circuit based on a Norton amplifier is shown in Fig. 8. To achieve the required gain control range and step, two VGA sections are cascaded. The first section operates in a 6-dB step wide gain control range while the other VGA section provides the precise 1-dB gain stepping. The VGA circuit is thus operating in a coarse and fine arrangement. The control word of the fine section is incremented up to a gain of 5 dB; then the coarse VGA gain is stepped up to give a 6-dB gain increment while simultaneously resetting the fine VGA section gain to 0 dB. The fine VGA section is then incremented again to precisely increase the overall VGA circuit gain. The choice of the resistor values is influenced by a number of factors. Smaller resistance values save area and reduce the input-referred noise. The resistors used can be decreased down to a certain limit, which is mainly influenced by two factors: the power consumption and current drive capability and the error resulting from the finite input resistance of the Norton amplifier. Taking into account the finite input resistance R_x of the virtual ground nodes, the amplifier gain is given by

$$\frac{V_o}{V_i} = \frac{R_f+R_x}{R_1+R_x}\left(\frac{1}{1+\dfrac{R_f+R_x}{R_m}}\right). \tag{10}$$

For high transresistance gain R_m and small R_x, the above equation can be approximated by

$$\frac{V_o}{V_i} = \frac{R_f}{R_1}\left(1+\frac{R_x}{R_f}\left(1-\frac{R_f}{R_1}\right)\right). \tag{11}$$

The worst case error results from the highest gain setting. In that case, a small input resistance R_1 is used, resulting in a high amplifier gain that is approximately given by

$$\frac{V_o}{V_i} = \frac{R_f}{R_1}\left(1+\frac{R_x}{R_1}\right). \tag{12}$$

The error will decrease if larger values of resistance R_1 and R_f are used. It is worth noting that a constant virtual ground resistance that is independent of the input signal will result in a

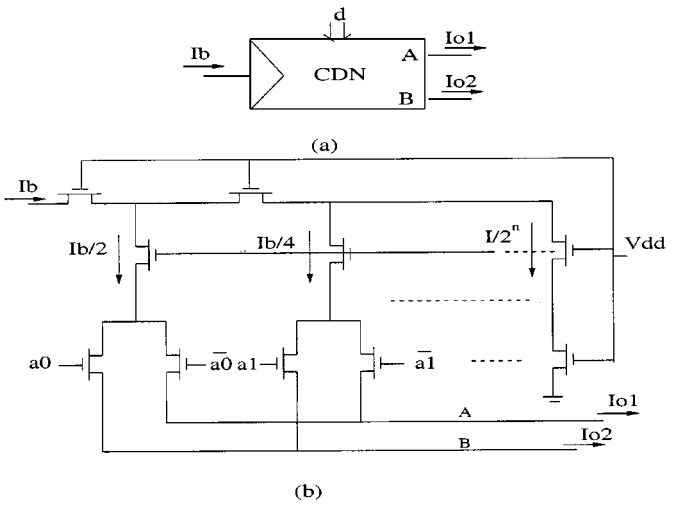

Fig. 9. The current division network: (a) symbol and (b) circuit realization.

gain error only with no impact on distortion. However, in reality, from a large signal perspective, the resistance R_x changes slightly with the input current of the Norton amplifier. This change is signal dependent and will result in harmonic distortion. If R_1 is chosen sufficiently high, the distortion resulting from the variation of R_x can be kept within acceptable limits. Another way to overcome the limitations resulting from R_x is to use a fully differential Norton amplifier, as will be described in the next section. The VGA circuit employs current division network (CDN) to realize a digital offset trimming control function. The current division network symbol is shown in Fig. 9(a). The circuit diagram of the CDN is given in Fig. 9(b). According to the current division principle [17], [18], the input current I_{in} of this network divides equally into two parts. The first part goes through transistor M2 and the other part flows through transistor M3. The current of transistor M3 is again divided into two equal parts. Hence one-fourth of the input current flows through transistor M4 and the other one-fourth continues across more stages of the CDN to be further divided. Transistors M5, M6, M7, M8, etc., are used as switches where the digital word d and its complement are applied to their gates to produce the following two output currents:

$$I_{o1} = I_{\text{in}} \sum_{i=1}^{n} a_i 2^{-i} \tag{13}$$

$$I_{o2} = I_{\text{in}} \sum_{i=1}^{n} \overline{a}_i 2^{-i}. \tag{14}$$

The CDN implementation has the advantage that the switch transistors are a part of the network. Thus they have the same aspect ratio and their finite resistance does not contribute any error to the current division. Therefore, all MOS transistors in the CDN can be selected small to save area, and the equivalent resistance can be small without degrading the division accuracy. This is not the case in $R-2R$ ladders, where the MOS switch resistance has to be kept much smaller than the resistance used in the ladder to maintain good accuracy. The current division principle only holds if the two output terminals A and B of the current division network are kept at a fixed voltage level. If the voltage levels of the two output terminals are equal, the current division network dissipates nearly no standby power. Hence, it is clear that for a circuit to utilize the current division network effectively, the two output terminals of the current divider should be kept at a fixed equal voltage level. This is easily achieved by connecting the two outputs of the CDN to the inputs of the Norton amplifier. Using the digital word and a constant input current to the CDN, the ratio of the output currents can be accurately tuned to provide the required offset cancellation current value at the amplifier input.

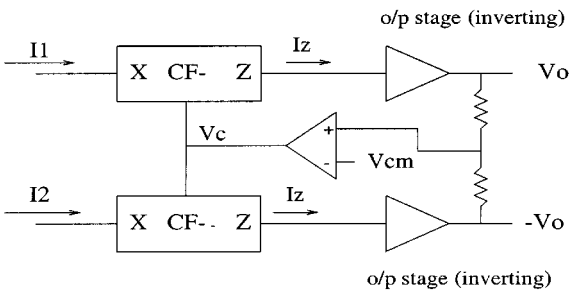

Fig. 10. Fully differential Norton amplifier block diagram.

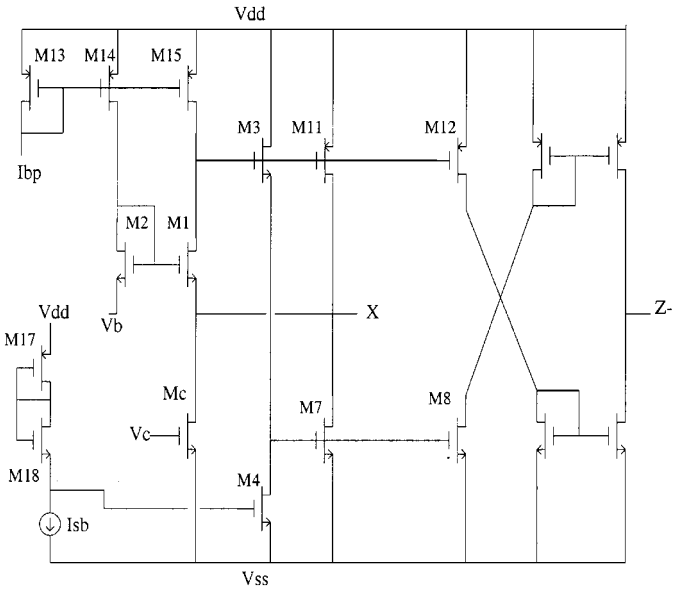

Fig. 11. The CMOS realization of the inverting current follower (CF-).

V. Fully Differential Norton Amplifier VGA

The Norton amplifier and VGA circuits described in the previous section can be used for single-ended signal processing. In many integrated circuit applications and especially wireless transceivers, the signal is present in a differential form and a fully differential mode of operation is required. Fully differential signal processing offers the advantage of improved dynamic range and higher supply-noise rejection. It is thus desirable to modify the Norton amplifier circuit to handle fully differential signals. Since the single-ended Norton amplifier already provides differential input processing, we only need to slightly modify the way the output signal is produced to provide a fully

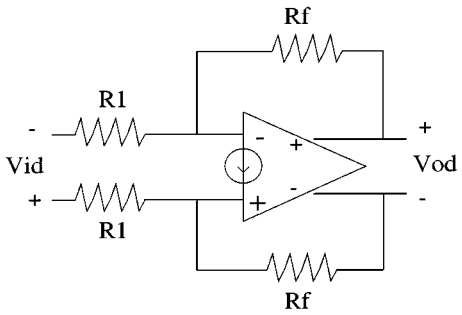

Fig. 12. Fully differential Norton-based amplifier.

differential output. Fig. 10 shows the block diagram of the fully differential Norton amplifier. The first modification is the use of a negative current follower (CF−). The CF− produces an inverted version of the input current at its output terminal. (It is worth noting that the positive direction of the output current is assumed to be flowing inwards through the output terminal.) The circuit diagram of the CF− is shown in Fig. 11, where the current inversion is achieved by the use of extra current mirrors. The use of CF− simplifies the negative feedback between the output of the Norton amplifier and its inputs. The other circuit modification is the addition of a common-mode feedback circuit. Two equal resistors are used to sense the common-mode output level, and a traditional differential pair comparator circuit is used to compare the sensed common mode with the desired value. The output of the comparator controls the common-mode level by adjusting the bias currents of the current-follower circuits through the gate voltage V_C of transistor M*c*. In some applications, pseudodifferential operation is sufficient and the common-mode feedback circuit can be removed. In that case, the errors in the common-mode voltage level at the output of the pseudodifferential amplifier will not be corrected. Thus, for applications requiring fully differential operation, the addition of the common-mode feedback circuit is essential. The VGA design with the fully differential Norton amplifier is straightforward. To show some advantages offered by the fully differential Norton amplifier, we consider the amplifier circuit shown in Fig. 12. It is important to note that the fully differential Norton amplifier realization will force the input voltage and input current to be zero. The voltage gain taking into account the finite input resistance R_X of the current follower circuit is given by

$$\frac{V_o}{V_i} = -\frac{R_f/R_1}{1+\dfrac{R_X + R_f(1+R_X/R_1)}{R_M}}. \tag{15}$$

One clear advantage is that errors resulting from the finite virtual ground input resistance of the current follower is reduced by the high transresistance gain R_M. In effect, the errors resulting from the finite input resistance R_X are now scaled down to the order of R_X/R_M. Hence the feedback in a fully differential Norton amplifier will force both input currents to the amplifier terminals to be zero and will reduce the input resistance of the CF as well. It is also worth noting that in the fully differential version of the amplifier, the current transfer errors of the current follower circuit will produce offset errors only with no impact on linearity. This is not the case for the single-ended realization, where an accurate and linear current transfer operation is required from the current follower circuit CF1 of Fig. 4. This requirement places a fundamental limit on the accuracy of the single-ended Norton amplifier governed by the matching of the current mirroring transistors used in CF1.

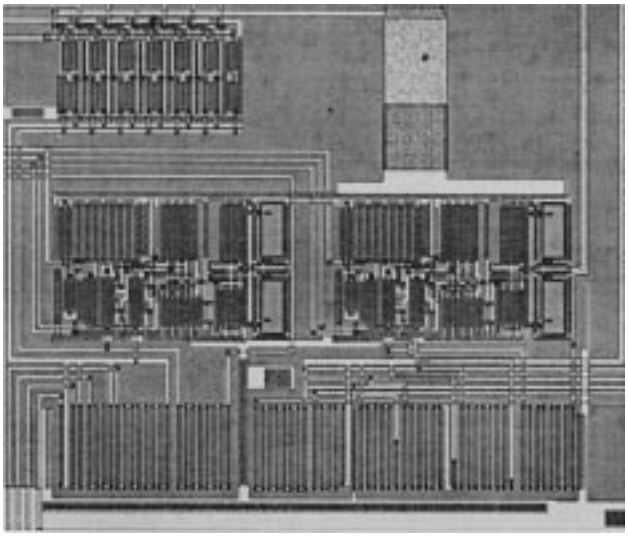

Fig. 13. Norton amplifier-based VGA die photo.

TABLE I
NORTON AMPLIFIER CIRCUIT MEASUREMENTS

Characteristics	single ended	fully differential
Input resistance	18Ω	1.7Ω
Transresistance gain	2.6MΩ	5.1MΩ
Standby current	389μA	426μA
Amplifier Bandwidth (@Cl=15pf)	4.1MHz	4.1MHz
current drive capability	800μA	800μA

VI. SIMULATION AND EXPERIMENTAL RESULTS

In this section, experimental results for the Norton amplifier and VGA circuits are discussed. The Norton amplifier-based VGA of Fig. 8 has been fabricated through MOSIS. The circuit was realized in a standard 2-μm n-well CMOS process. Fig. 13 shows the die photo of this VGA. The circuit occupies an area of 1450 $\times$ 1280 μm and provides a 6-bit digital offset trimming. Separate circuits for the current follower, Norton amplifier, and fully differential amplifier were also fabricated to provide more experimental data on the performance of the proposed Norton amplifier circuits. All circuits were tested with the supply voltage set to $\pm$1.5 V. The biasing current of the Norton amplifiers was adjusted to 38 μA and the current I_{sb} to 4 μA. A summary of measurement results for the single-ended and fully differential Norton amplifier is given in Table I. The transresistance gain of the single-ended Norton amplifier is measured by sweeping the input current and measuring the output voltage, as shown in Fig. 14. The transresistance gain is found to be more than 2.6 MΩ without cascoding. When the cascoding transistors are used, the transresistance gain is more than 8.1 MΩ. The plot also shows that the amplifier has an offset input current of about 2 μA.

To measure the equivalent resistance of the input virtual ground nodes of the amplifier, a current source is connected to the input

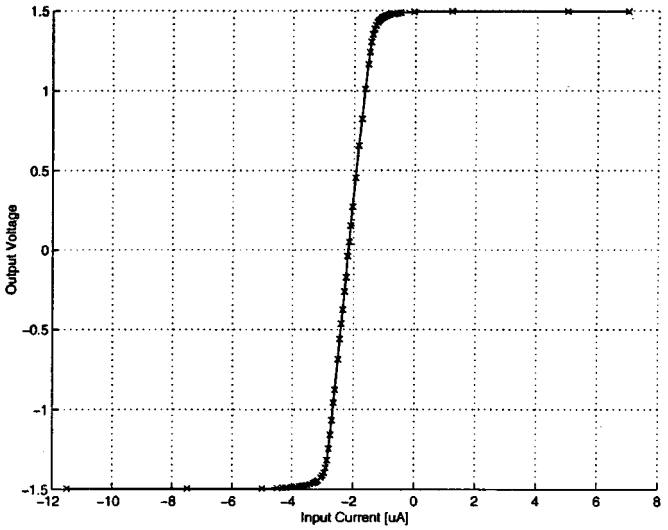

Fig. 14. The open-loop output voltage versus the input current of the Norton amplifier.

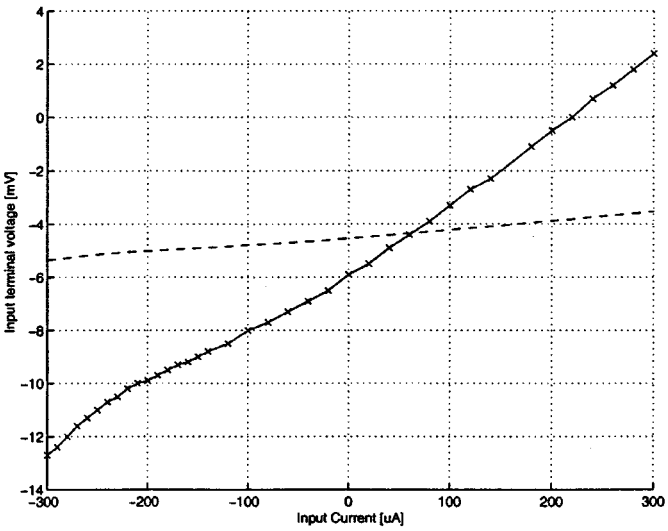

Fig. 15. The virtual ground voltage variation versus the input current (solid line for single-ended amplifier and the dotted line for the fully differential amplifier).

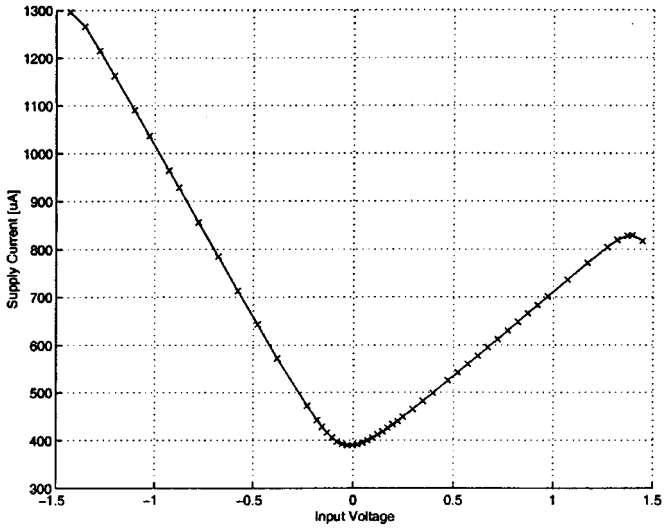

Fig. 16. The Norton amplifier supply current.

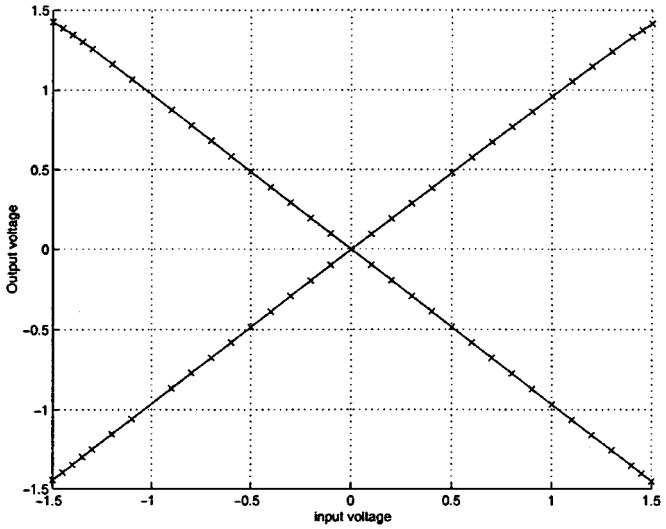

Fig. 17. Output voltage swing for a unity-gain amplifier based on the fully differential Norton amplifier.

of the amplifier. The current is then swept and the voltage level of the input virtual ground node is measured. The result is shown in Fig. 15. Ideally, the voltage level of the input node should remain at a constant level. Practically, the finite resistance of the input terminal causes the voltage level to vary slightly. The slope of this variation gives the equivalent input resistance. As expected, Fig. 15 shows that the input resistance of the single-ended Norton amplifier is 18 Ω, while that of the fully differential amplifier is about 1.7 Ω. Fig. 16 shows the supply current of the Norton amplifier versus the output current. The circuit was connected as an amplifier with unity gain. The figure clearly shows the class AB operation of the circuit. The standby current is found to be 389 μA for the single-ended Norton amplifier and about 426 μA for the fully differential amplifier. The maximum current drive capability of the Norton amplifier circuit is greater than 800 μA. The measured standby current value is about 14% higher than predicted. This difference can be attributed to the threshold voltage variation caused by the body effect. When deriving (6), it was assumed that transistors M3, M4 and M7, M18 have equal threshold voltages. This can only be true if the sources of those transistors are connected to the body to avoid variation of the threshold voltage caused by the body effect. To achieve this, a p-well process is required. The fabricated circuit uses an n-well process in which all NMOS transistors were placed in the same substrate. Mismatches in the threshold voltages of M3, M4 and M7, M18 resulted in more standby power dissipation.

Fig. 17 shows the rail-to-rail output swing of the fully differential amplifier when used as an amplifier of unity gain. The step response of this amplifier is also shown in Fig. 18. The plot shows the output of one of the amplifier output terminals when a square wave of 1 MHz is applied to the input. The load capacitance is more than 15 pF. Measurements show that the amplifier provide a nonslew-rate-limited output response. Next, the gain of the VGA circuit is measured for different digital gain settings. The result is shown in Fig. 19, where the x-axis represents the digital control word and the y-axis is the VGA gain in dB. The ideal gain is shown by a solid line, the measured gain values are

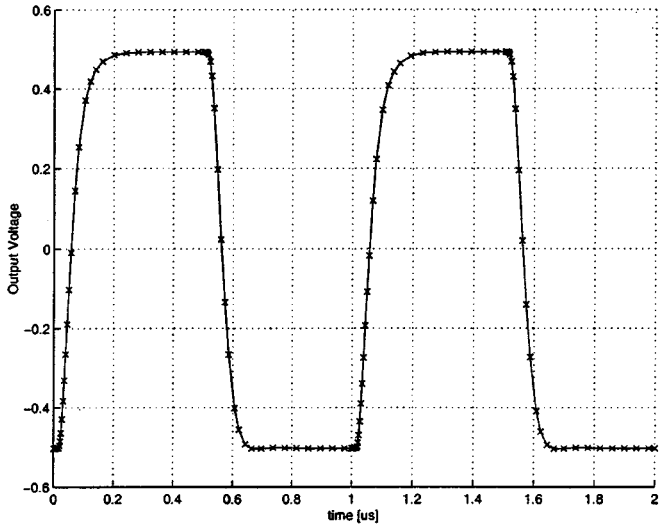

Fig. 18. The Norton amplifier step response (Cl = 15 pF).

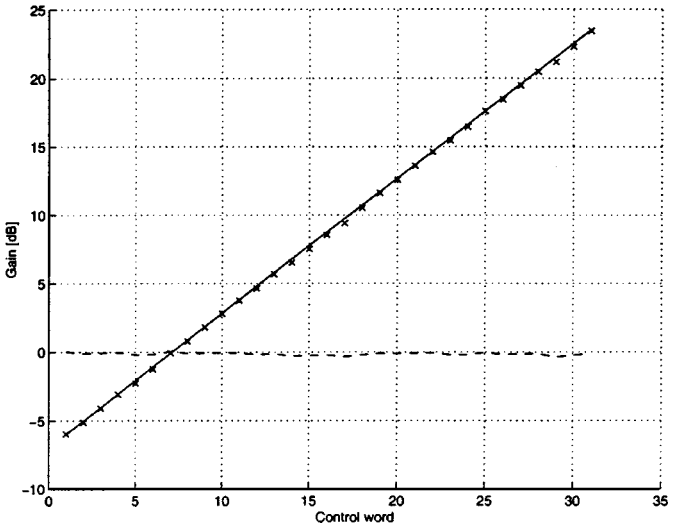

Fig. 19. The measured gain characteristic of the VGA circuit of Fig. 6. (The dotted line represents the gain error.)

denoted by X, and the gain error is the dotted line. A gain range of 30 dB can be achieved with gain error less than 0.4 dB.

Fig. 20 shows the frequency response of the VGA for different gain settings. As expected, the amplifier provides a constant bandwidth that varies slightly with the gain setting. The amplifier provides a bandwidth of more than 4.1 MHz when driving a load capacitance of more than 15 pF. The result is good, taking into account that the amplifier is fabricated in 2-μm technology and is driving a large capacitance. Simulation results of the same circuit implemented in 0.8-μm CMOS technology and driving a 5-pF capacitance indicates a bandwidth of more than 22 MHz while dissipating less than 350 μA of standby current for each amplifier. The intermodulation distortion of the VGA was measured by applying two sinusoidal signals to the input. The frequency of the applied tones are 350 and 400 KHz, respectively. Fig. 21 shows the resulting intermodulation distortion when two tones of -10 dBV are used. The IP3 of the VGA circuit is more than 29 dBm. The input-referred noise of the VGA is 16.5 nV/$\sqrt{\text{Hz}}$ at 18-dB gain setting. and 71 nV/$\sqrt{\text{Hz}}$ for 0-dB gain setting. It is worth noting that

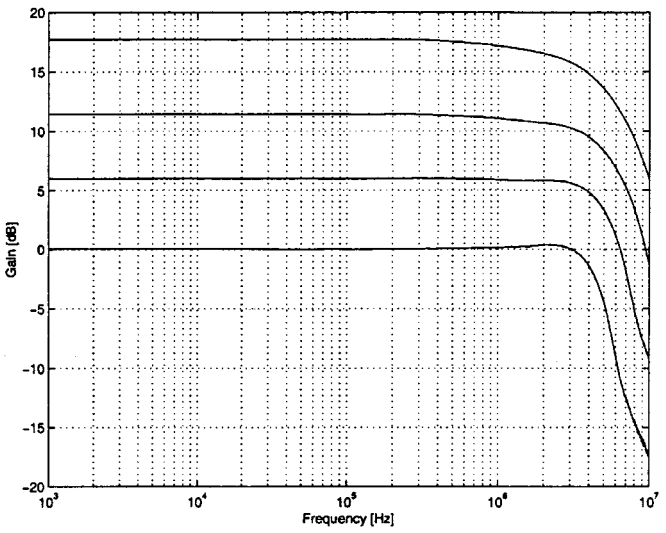

Fig. 20. The measured frequency response of the VGA for different gain settings.

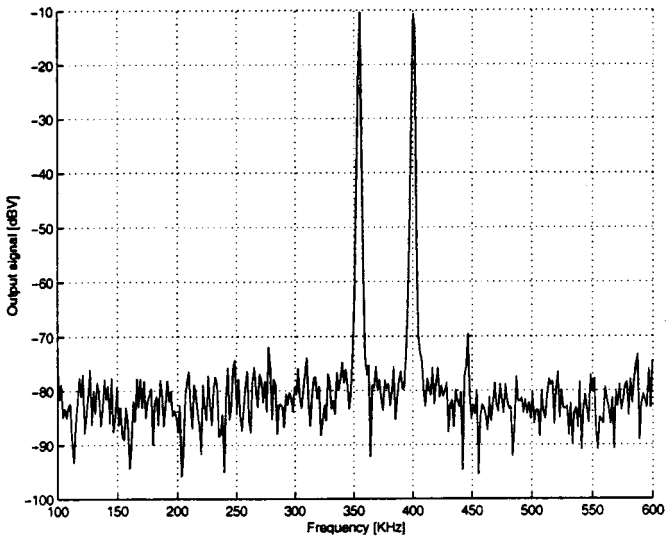

Fig. 21. Intermodulation distortion of the Norton amplifier-based VGA.

TABLE II
NORTON AMPLIFIER-BASED VGA MEASUREMENTS

Characteristics	Measurement
Technology	2μm
Area	1.45mmX1.28mm
Supply Voltage	3.0V
Standby current	884μA
Gain control range	30dB
gain step	1dB
Gain error	0.4dB
IIP3	29dBm
Input referred noise (@18dB gain)	$16.5\frac{nv}{\sqrt{Hz}}$
Input referred noise (@0dB gain)	$71\frac{nv}{\sqrt{Hz}}$

as predicted earlier, the VGA circuit exhibits an offset voltage. However, using the digital offset control current divider circuit with a 12-μA bias current, the output offset was kept below 4 mV in all cases. Measurement results for the VGA are summarized in Table II. It is clear that the circuit can be used as a

baseband VGA for a multistandard receiver covering the GSM, IS-95, and IS-54 bandwidth requirements. Simulation results indicate that the VGA can handle wider bandwidth signals associated with the third-generation WCDMA when fabricated in a 0.5-μm CMOS process.

VII. Conclusion

This paper discusses the potential use of Norton transresistance amplifier to realize digitally controlled variable-gain amplifiers for integrated wireless receivers. A new low-voltage CMOS realization for the Norton amplifier is proposed. The circuit utilizes class AB techniques to provide controllable low-power standby current consumption. It is shown that the extension of the Norton amplifier to handle fully differential signals reduces errors resulting from the finite input resistance of the virtual ground nodes and does not require accurate matching in the current follower. The VGA circuit offers digitally controlled offset trimming by utilizing a compact current division network. Experimental results from a test chip fabricated through MOSIS are in good agreement with the theoretical work.

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Hassan Elwan was born in Cairo, Egypt, in 1971. He received the B.Sc. and M.Sc. degrees from the Electronics and Communication Department, Cairo University, Cairo, Egypt, in 1994 and 1996, respectively. He is currently pursuing the Ph.D. degree from The Ohio State University, Columbus.

He is currently a Research Assistant at The Ohio State University. His research interests include mixed signal CMOS circuit design, wireless communication, filtering, and data converter design.

Ahmed M. Soliman was born in Cairo, Egypt, on November 22, 1943. He received the B.Sc. degree (with honors) from Cairo University, Cairo, in 1964 and the M.S. and Ph.D. degrees from the University of Pittsburgh, Pittsburgh, PA, in 1967 and 1970, respectively, all in electrical engineering.

He is currently Professor and Chairman of the Electronics and Communications Engineering Department, Cairo University. From 1985 to 1987, he was Professor and Chairman of the Electrical Engineering Department, United Arab Emirates University. From 1987 to 1991, he was the Associate Dean of Engineering at the same university. He has held visiting academic appointments at San Francisco State University, Florida Atlantic University, and the American University in Cairo. He was a Visiting Scholar at Bochum University, Germany (Summer 1985) and the Technical University of Wien, Austria (Summer 1987).

Dr. Soliman received the First Class Science Medal from the president of Egypt in 1977 for his services to the field of engineering and engineering education.

Mohammed Ismail (S'80–M'82–SM'94–F'97) received the B.S. and M.S. degrees in electronics and telecommunications engineering from Cairo University, Cairo, Egypt, in 1974 and 1978, respectively, and the Ph.D. degree in electrical engineering from the University of Manitoba in 1983.

He is a Professor with the Department of Electrical Engineering, The Ohio State University, Columbus, and the Founder and Director of the Analog VLSI Lab. He held several positions previously in both industry and academia and has served as a Corporate Consultant to nearly 30 companies in the United States and abroad. He held visiting appointments at the Norwegian Institute of Technology, University of Oslo, University of Twente, Tokyo Institute of Technology, Helsinki University of Technology, and the Swedish Royal Institute of Technology. He has authored many publications on VLSI circuit design and signal processing and has been awarded several patents in the area of analog VLSI. He has coedited and coauthored several books, including *Analog VLSI Signal and Information Processing* (New York: McGraw-Hill, 1994). He advised the work of 14 Ph.D. students, 42 M.S. students, and 16 visiting scholars. His current interests include low-voltage/low-power VLSI circuits, RF and mixed-signal VLSI circuits for wireless communications, statistical computer-aided design and optimization, integrated circuits for image, video and multimedia applications, and VLSI information processing systems. He is the Founder of the *International Journal of Analog Integrated Circuits and Signal Processing* and serves as its Editor-In-Chief (North America).

Dr. Ismail has received many awards, including the IEEE 1984 Outstanding Teacher Award, the NSF Presidential Young Investigator Award in 1985, the OSU Lumley Research Award in 1993 and 1997, the SRC Inventor Recognition Awards in 1992 and 1993, and a Fullbright/Nokia fellowship Award in 1995. He has served the IEEE in many editorial and administrative capacities, including General Chair of the 29th Midwest Symposium CAS, Member of the CAS Society Board of Governors, Chair of the CAS Analog Signal Processing Technical Committee, Editor of the IEEE CIRCUITS AND DEVICES MAGAZINE, Founder and Coeditor of *The Chip*, a column in the magazine, and Associate Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS, IEEE TRANSACTIONS ON NEURAL NETWORKS, IEEE TRANSACTIONS ON VLSI SYSTEMS, and IEEE TRANSACTIONS ON MULTIMEDIA.