with the solution, the nonlinear equation (16) can be linearized around the period-1 solution. Consequently, the rest of the samples can be computed using the vector $\mathbf{p}_m$ and the linear expression

$$p_n = -\frac{\sum_{k=1}^{m} a_k p_{n-k} + \sum_{k=1}^{m} b_k f'(x_{n-k}) p_{n-k}}{a_0 + b_0 f'(x_n)} \quad n > m.$$

Once the perturbation vector

$$\mathbf{p} = [p_1, p_2, \ldots, p_{2N}]^T$$

of $2N = 512$ samples has been computed, we obtain a period-2 solution adding the vector $\mathbf{p}$ multiplied by a constant α to two periods of the period-1 solution

$$\mathbf{x}_{|\text{period-2}} \approx [\mathbf{x}_{|\text{period-1}}; \mathbf{x}_{|\text{period-1}}] + \alpha \mathbf{p}. \tag{18}$$

If this constant is well chosen, the approximate solution is close to the final solution and the iteration will converge.

C. Period-2 and Period-4 Limit Cycles

With the initialization proposed in (18) with $\alpha = 0.6$, we obtain the phase plane depicted in Fig. 5. The eigenvalues are all inside the unit circle. Therefore the solution is stable. A *posteriori* we can verify the hypothesis made in (18) that the eigenvector $\mathbf{p}$ added to the period-1 solution is indeed close to the period-2 solution.

With the decrease of the parameter R over the period-2 solution a new period doubling bifurcation point is detected for $R = 1.796$ kΩ. A stable period-4 solution is computed for $R = 1.7952$ kΩ (Fig. 5).

VII. Conclusion

A new method to directly determine the steady-state response of nonlinear autonomous circuits with distributed parameters has been presented. To validate the method, it has been applied to the analysis of the TDCC in one of its periodic windows, a paradigmatic example of the kind of circuits to which this paper refers.

A procedure for determining the stability of the steady-state solutions is presented. To check the reliability of this method, it has been applied to the stability at the equilibrium points of the TDCC in which analytical results exist [11] and excellent agreement has been obtained.

The combination of the discrete-time approach with the study of the stability of the solutions obtained allows us to detect period-doubling bifurcation points. A procedure to initialize the iterative solving process to obtain the bifurcated solution is explained and successfully applied. The results coincide with those described in [11], and with those obtained using integration techniques, without having to integrate the response until the transient dies out.

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A Low-Voltage Single Input Class AB Transconductor With Rail-To-Rail Input Range

Ahmed A. El-Adawy and Ahmed M. Soliman

***Abstract*—A new CMOS programmable rail-to-rail transconductor is presented. A linear *V–I* characteristic is obtained by using the principle of nonlinearity cancellation of matched MOS transistors operating in the ohmic region. Rail-to-rail operation is achieved by using two complementary blocks. The circuit is suitable for low voltage as it can operate from supply voltages down to ±1.5 V. PSpice simulations show that the transconductance gain can be electronically tuned from 13 to 90 μ A/V with bandwidth of about 40 MHz.**

***Index Terms*—Low-voltage circuits, transconductors.**

I. Introduction

As the advances in the VLSI technology and the demand for portable electronic products lead VLSI circuits operating in low supply voltages (lower than 3 V), current-mode signal processing techniques will become increasingly important and attractive [1]–[5]. Circuits designed to exploit the current-mode techniques improve operating speed and can be implemented in low-cost digital CMOS fabrication process. Traditionally, however, most analog signal processing has been accomplished by using voltage as the signal variable. In order to maintain compatibility with voltage processing circuits, it is often necessary to convert the input and output signals of a current-mode signal processor to voltage, that is, to use transconductors (or *V-I* converters). Numerous transconductor design schemes have been proposed and implemented [6]–[12]. However, most of these schemes have the problem that the control voltage that controls the transconductance gain also affects the linear operating range. This leads to a conflict between obtaining large input linear range and high transconductance gain. The proposed transconductor has a programmable gain while

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achieving rail-to-rail operation. It uses the principle of nonlinearity cancellation of matched transistors operating in the ohmic region.

II. The Proposed Transconductor

Fig. 1 represents the block diagram of the proposed rail-to-rail transconductor, which consists of an N and a P part connected in parallel–parallel, where V_{BN} and V_{BP} are control voltages.

The N part of the proposed transconductor circuit is shown in Fig. 2. All the transistors are operating in the saturation region except the transistors $M5$ and $M9$ that operate in the ohmic region. The loop formed by $M3$ and $M4$ ensures that the voltage at the source of $M4$ is constant and is given by

$$V_{S4} = V_{BN} - V_{T4} - \sqrt{\frac{2I_{BN}}{K_4}} \tag{1}$$

where V_{T4} is the threshold voltage and K_4 is the transconductance parameter of $M4$. Where K is given by

$$K = \mu_n C_{\rm OX} \frac{W}{L}. \tag{2}$$

The rest of the undefined parameters have their usual meanings.

The role of transistor $M3$ is to supply the current needed by the transistor $M5$ so as to satisfy (1).

Similarly, the loop formed by $M8$ and $M10$ operates in the same manner, hence

$$V_{S8} = V_{BN} - V_{T8} - \sqrt{\frac{2I_{BN}}{K_8}}. \tag{3}$$

If $M4$ and $M8$ are matched, then from (1) and (3)

$$V_{S4} = V_{S8} = V_{BN} - V_{T4} - \sqrt{\frac{2I_{BN}}{K_4}}. \tag{4}$$

Hence, the body effect has no influence on the circuit operation. Applying KCL at node A

$$I_9 = I_{10} + I_7 + I_6 = I_{10} + I_5. \tag{5}$$

Then

$$I_{10} = I_9 - I_5. \tag{6}$$

The transistors $M5$ and $M9$ are assumed to operate in the ohmic region. Where the current in the ohmic region is given by

$$I = K(V_G - V_T)(V_D - V_S) + a_1(V_D^2 - V_S^2) + a_2(V_D^3 - V_S^3) + \cdots. \tag{7}$$

Since the transistors $M5$ and $M9$ have equal drain and equal source voltages, then

$$I_N = I_{10} = I_9 - I_5 = K_N(V_I) \cdot \left(V_{BN} - V_{T4} - \sqrt{\frac{2I_{BN}}{K_4}} - V_{SS}\right) \tag{8}$$

where K_N is the transconductance parameter of $M5$ and $M9$. Thus, the output current is linearly related to the input voltage, the tranconductance g_{mn} is given by

$$g_{mn} = K_N \left(V_{BN} - V_{T4} - \sqrt{\frac{2I_{BN}}{K_4}} - V_{SS}\right) \tag{9}$$

where the transconductance g_{mn} is controlled by the voltage V_{BN}. An important feature of the proposed circuit is that it operates as a transconductor as long as $V_I > 0$ and then $I_N > 0$. When $V_I < 0$ the transistor $M10$ will turn off and $I_{10} = 0$. In brief, the input–output relation is as follows:

$$I_N = I_{10} = \begin{cases} K_N(V_I)\left(V_{BN} - V_{T4} - \sqrt{\dfrac{2I_{BN}}{K_4}} - V_{SS}\right) \\ \qquad V_I > 0 \\ 0, \quad V_I < 0. \end{cases} \tag{10}$$

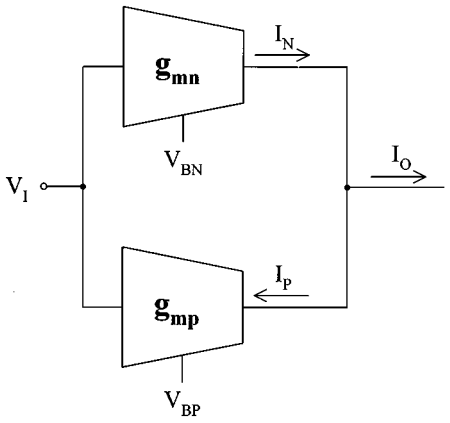

Fig. 1. The block diagram of the proposed transconductor circuit.

TABLE I
Aspect Ratios of the Transistors

Transistors	Aspect ratios (W/L)
M1, M2, M6	6/4.8
M3, M7	24/2.4
M4, M8	96/2.4
M5, M9	24/4.8
M10, M11	18/3.6
M12, M13, M17	6/4.8
M14, M18	24/2.4
M15, M19	48/4.8
M16, M20	48/4.8
M21, M22	12/4.8
M23 through M30	24/4.8

TABLE II
Transconductor Performance for Different Biasing Currents

I_B	20uA	40uA	60uA
Bandwidth	61MHz	43MHz	48MHz
Standby current	51μA	78μA	106μA
Transconductance	13.3 μA/V	26.7 μA/V	40 μA/V

TABLE III
THD for Different TemperaturesVskip 1pt

Temperature	THD
-40°C	2.57%
27°C	2.52%
100°C	2.46%

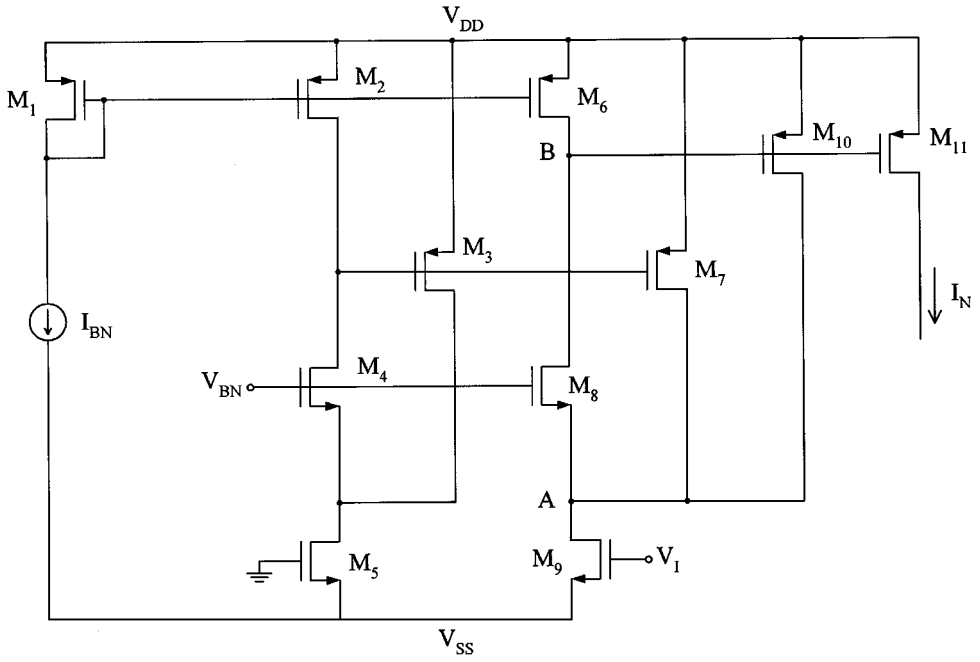

Fig. 2. The N part of the proposed transconductor.

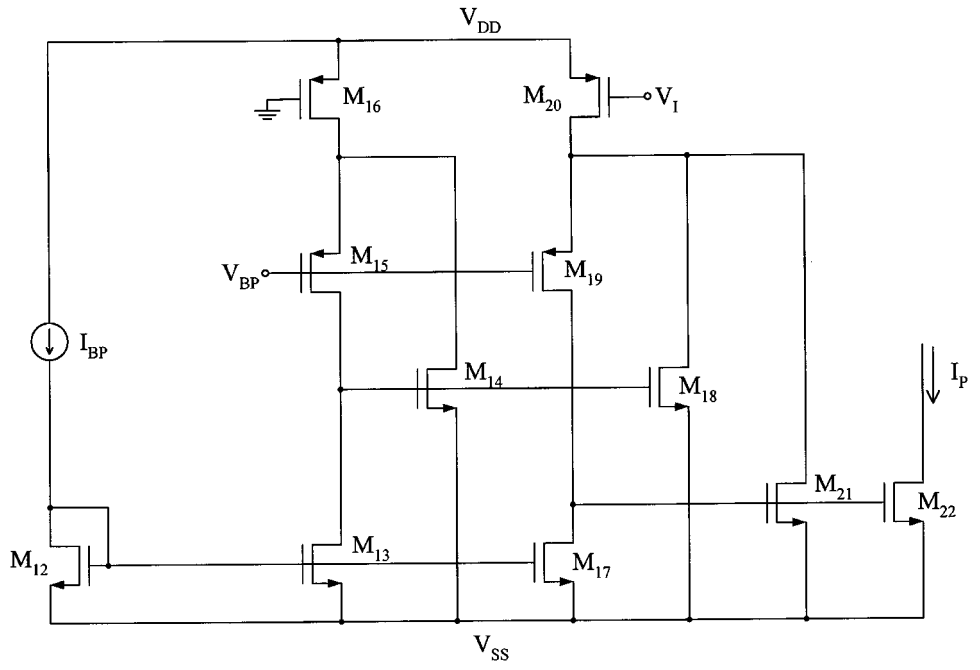

Fig. 3. The P part of the proposed transconductor.

It is worth mentioning that the transistors $M1$ through $M5$ form the biasing circuit of the transconductor. This means that the same biasing circuit can be used for several transconductors. To obtain a rail-to-rail input range transconductor a complementary block is used. This block is shown in Fig. 3. It operates in the range $V_I < 0$. Using the same procedure, it can be shown that

$$I_P = \begin{cases} 0, & V_I > 0 \\ K_P(-V_I)\left(V_{DD} - |V_{T15}| - \sqrt{\dfrac{2I_{BP}}{K_{15}}} - V_{BP}\right) & \\ & V_I < 0. \end{cases} \tag{11}$$

The output current of the proposed transconductor is given by

$$I_O = I_N - I_P = g_m V_I \tag{12}$$

where

$$\begin{aligned} g_m &= K_N\left(V_{BN} - V_{T4} - \sqrt{\frac{2I_{BN}}{K_4}} - V_{SS}\right) \\ &= K_P\left(V_{DD} - |V_{T15}| - \sqrt{\frac{2I_{BP}}{K_{15}}} - V_{BP}\right). \end{aligned} \tag{13}$$

Hence, by adjusting the K's, V_{BN}, and V_{BP}, equal transconductances in the two half ranges can be obtained. However, this equation

is hard to meet since the K's and V_T's are process- and temperature-dependent parameters and are hard to predict. This problem can be solved by using a self-correcting biasing circuit.

III. The Self-Correcting Biasing Circuit

The biasing circuit of the N part of the proposed transconductor is shown in Fig. 4. In this circuit, the same N part transconductor is used in a feedback loop where the output current I_N is subtracted from the biasing current I_B. The difference is multiplied by the high output resistance of the transistors $M24$ and $M25$ to produce the biasing voltage V_{BN}. This feedback loop ensures that

$$I_N = I_{B1} = g_{mn} V_{B1}. \tag{14}$$

Then

$$g_{mn} = \frac{I_{B1}}{V_{B1}} = K_N \left(V_{BN} - V_{T4} - \sqrt{\frac{2I_{BN}}{K_4}} - V_{SS} \right). \tag{15}$$

The output voltage V_{BN} of this feedback loop is used to control the transconductance g_{mn} of the N part of the transconductor. Any process or temperature variations are compensated by the self-correcting biasing circuit.

Similarly, the biasing circuit of the P part of the transconductor is shown in Fig. 5, where the transconductance is given by

$$g_{mp} = \frac{I_{B2}}{-V_{B2}} = K_P \left(V_{DD} - |V_{T15}| - \sqrt{\frac{2I_{BP}}{K_{15}}} - V_{BP} \right). \tag{16}$$

To satisfy (14), the following condition is obtained:

$$\frac{I_{B1}}{V_{B1}} = \frac{I_{B2}}{-V_{B2}}. \tag{17}$$

To simplify the control of the transconductance, the following design equations are used:

$$I_{B1} = I_{B2} = I_B \tag{18}$$

$$V_{B1} = V_{DD} \tag{19}$$

$$V_{B2} = V_{SS} \tag{20}$$

Hence,

$$g_m = \frac{I_B}{V_{DD}}. \tag{21}$$

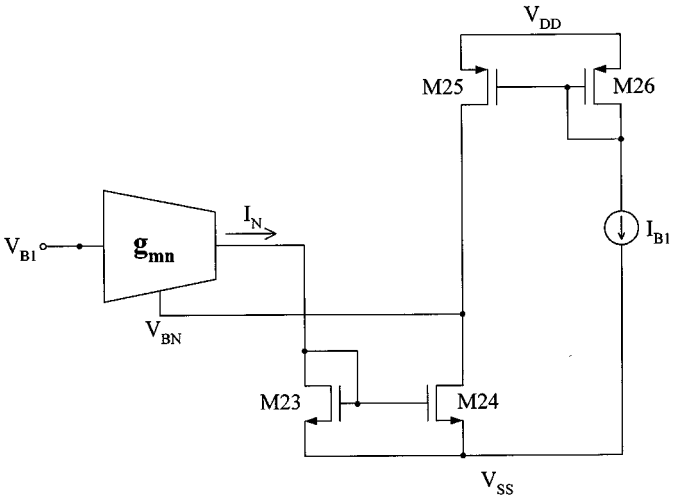

Fig. 4. The biasing circuit of the N part.

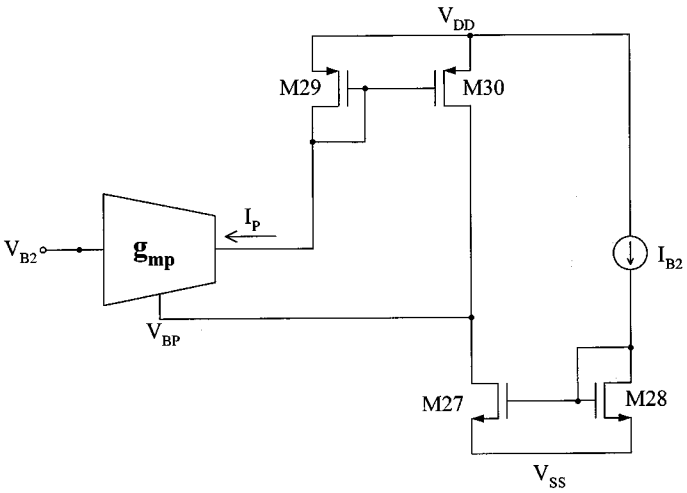

Fig. 5. The biasing circuit of the P part.

IV. Small Signal Analysis

Small signal analysis of the N part of the proposed transconductor leads to the transfer function (22), shown at the bottom of the page, where g_8 and g_{10} are the transconductances of $M8$ and $M10$ respectively. C_P is the parasitic capacitance at node B. A similar equation can be derived for the P part of the transconductor. From (22), the bandwidth is given by (23) at the bottom of the page. This equation suggests

$$\frac{i_O}{V_I} = \frac{g_8 g_{10} K_5 \left(V_{BN} - V_{TN} - \sqrt{\frac{2I_{BN}}{K_4}} - V_{SS} \right)}{g_8 g_{10} + sC_P \left(g_8 - K_5 \left(V_{T5} + V_{BN} - V_{TN} - \sqrt{\frac{2I_{BN}}{K_4}} - V_{SS} \right) \right)} \tag{22}$$

$$BW = \frac{g_8 g_{10}}{C_P \left(g_8 - K_5 \left(V_{T5} + V_{BN} - V_{TN} - \sqrt{\frac{2I_{BN}}{K_4}} - V_{SS} \right) \right)}. \tag{23}$$

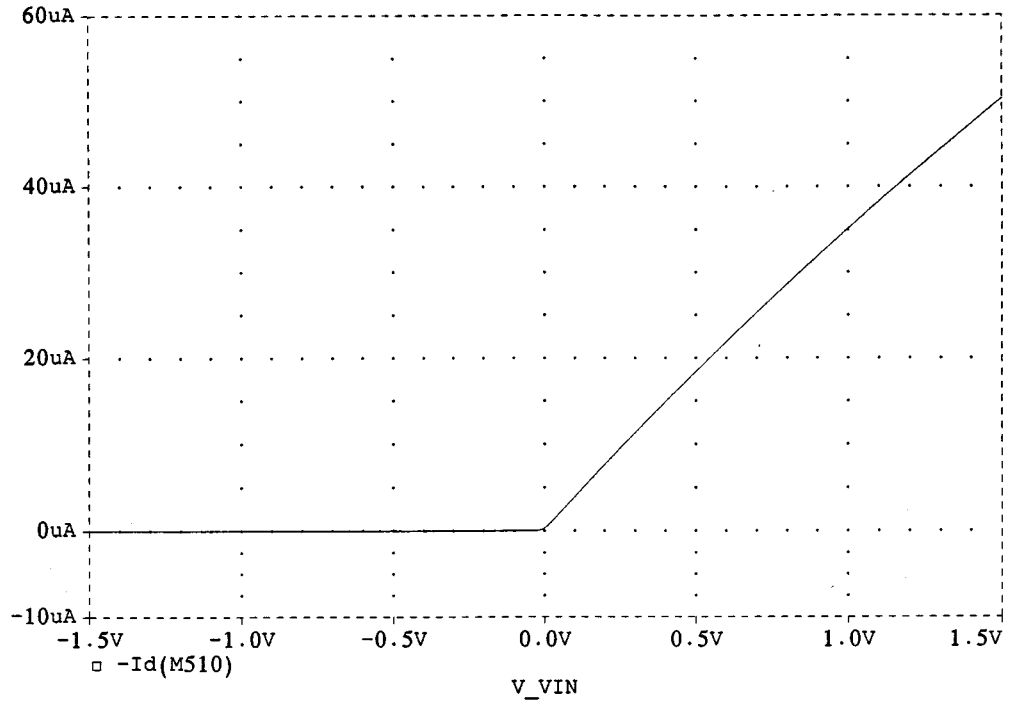

Fig. 6. The currents I_N against V_I when $I_B = 50\ \mu$A.

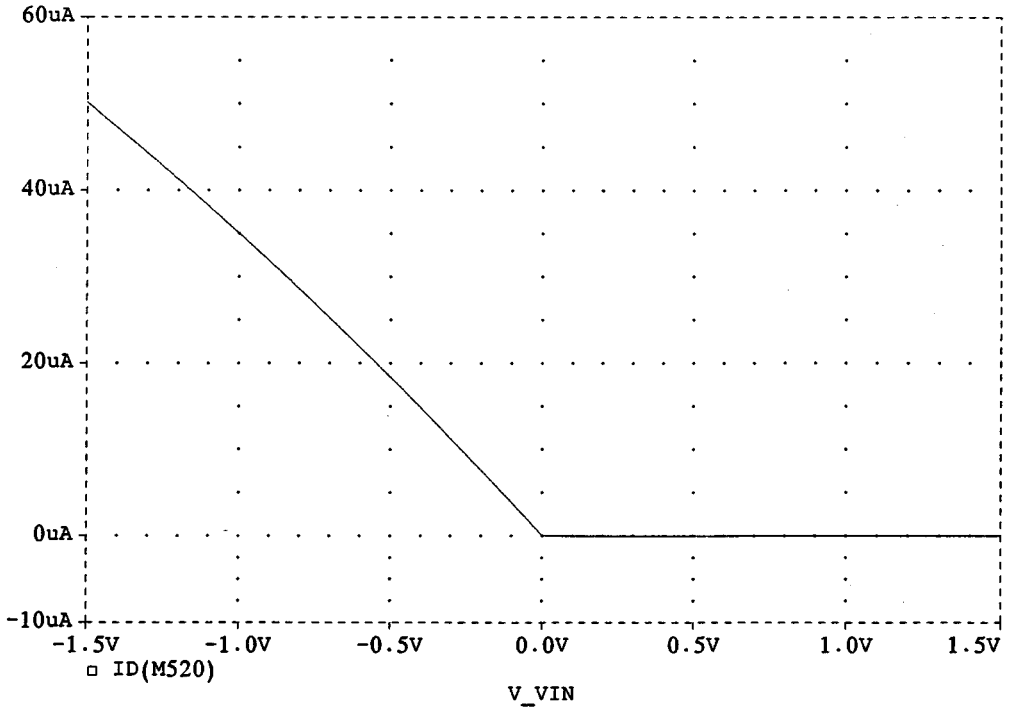

Fig. 7. The currents I_P against V_I when $I_B = 50\ \mu$A.

increasing the aspect ratio of the transistor $M8$ to maximize the bandwidth and to reduce its dependence on the control voltage V_{BN}.

V. Simulation Results

The proposed circuit has been simulated with PSpice using the AMI 1.2-μm CMOS technology provided by MOSIS. The aspect ratios of the transistors are given in Table I. Supply voltages are $\pm$1.5 V. Simulation is performed with the body of all transistors connected to the appropriate supply voltage. Table II shows the bandwidth, the standby current, and the transconductance for several values of the biasing current I_B.

The current I_N versus V_I is shown in Fig. 6 while Fig. 7 shows the current I_P when $I_B = 50\ \mu$A. Fig. 8 shows the output current of the proposed transconductor versus V_I for different values of I_B ranging

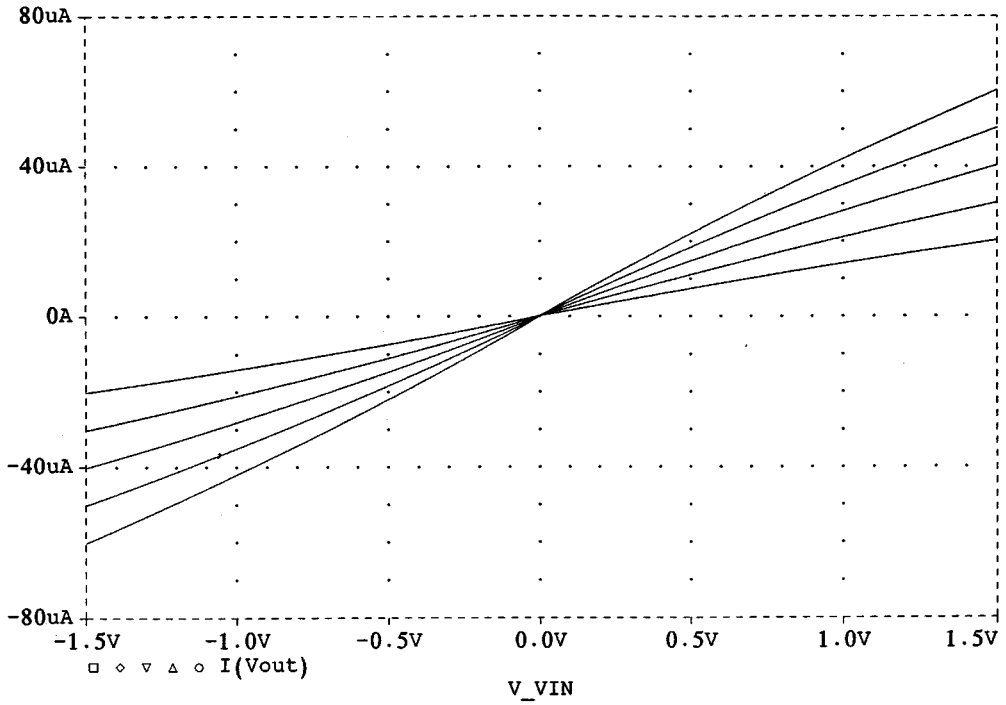

Fig. 8. Output current I_O against V_I with different values of I_B.

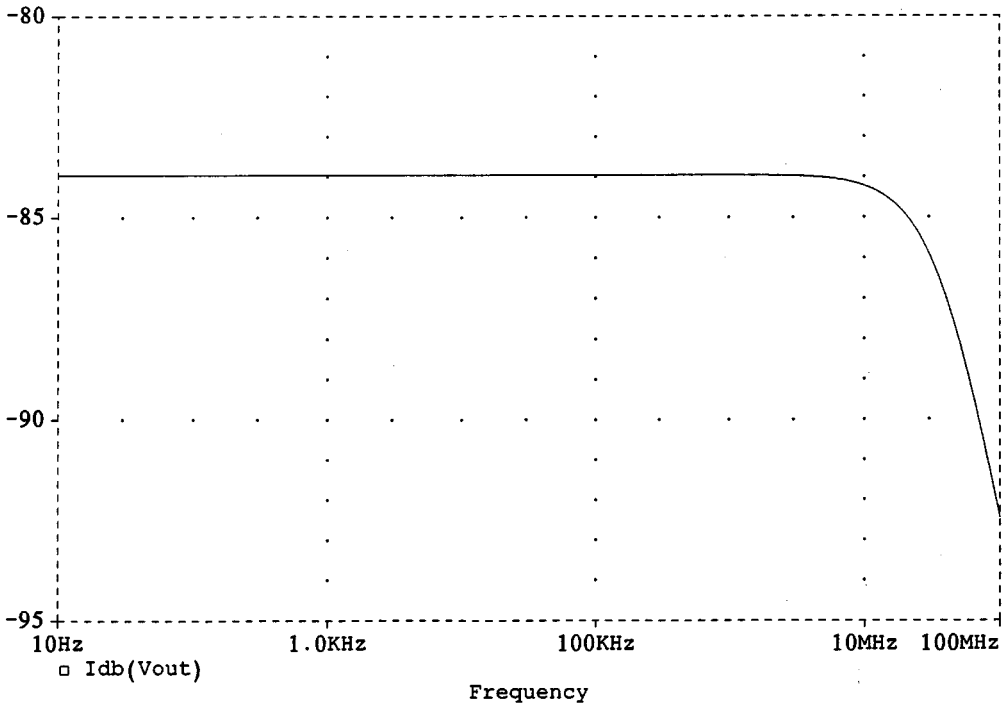

Fig. 9. Short-circuit frequency response at the output terminal when $V_I = 1$ V, $I_B = 50$ μA.

from 20 μA to 60 μA in steps of 10 μA. The frequency response of the output current is shown in Fig. 9, from which it is seen that the bandwidth is about 40 MHz.

To illustrate the temperature variations independence of the proposed transconductor, Fig. 10 shows the output current versus V_I for different temperatures (-40, 27, and 100°C). Total harmonic distortion

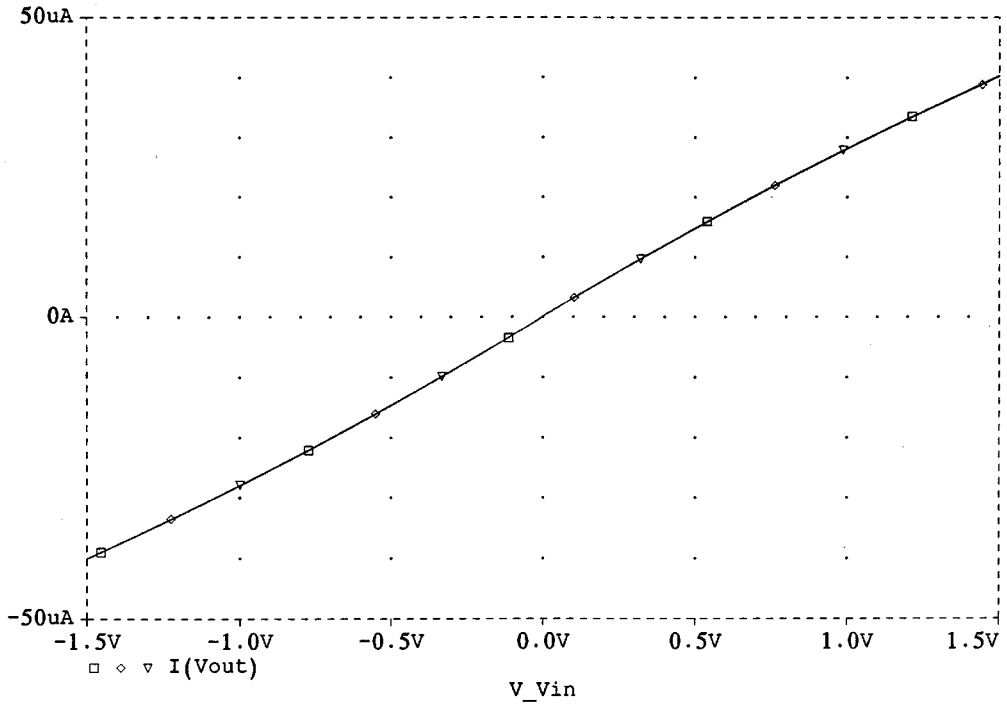

Fig. 10. Output current I_O versus V_I for different temperatures ($I_B = 40\ \mu$A).

(THD) is measured using a 100-KHz sinusoidal input with 1.5-V amplitude. The results are shown in Table III.

VI. Conclusion

A new single input class AB transconductor using the nonlinearity cancellation principle is proposed. The circuit has a rail-to-rail input range and its gain can be electronically tuned over a wide range. The control current does not affect the range of operation of the circuit. The circuit operation is independent of the body effect.

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Improved Delay Time Estimation of RC Ladder Networks

Chunhai Hou, Furong Gao, and Jixin Qian

***Abstract*—An improved delay time bound estimation is given in this paper for an n-cell RC ladder network with capacitive load.**

***Index Terms*— Bound estimation, delay time bound, RC ladder networks.**

I. Introduction

Recently, the delay time bound estimation has been attracting increasing attention due to its fundamental importance in digital circuits [1]–[6]. A basic model in integrated circuits is an RC ladder network, shown in Fig. 1. Delay time bound estimates have been

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