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Novel CMOS Realization of Balanced-Output Third Generation Inverting Current Conveyor with Applications

Ehab A. Sobhy · Ahmed M. Soliman

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Abstract A new current conveyor block, called a balanced-output third generation inverting current conveyor (ICCIII+−), is introduced in this paper. A novel CMOS realization for this block is proposed. To show the strength of this block, many applications are given, such as integrators, filters, and an oscillator. The proposed ICCIII+− and the presented applications are tested with SPICE simulations using CMOS 0.35 μm technology to verify the theoretical results.

Keywords Current conveyor · Integrators · Filters · Oscillators

1 Introduction

The third generation current conveyor (CCIII) was first introduced in [6]. The accurate performance and the wide bandwidth of the CCIII make this relatively new building block very attractive for use in many applications. It is a useful current-mode building block in current-sensing applications, filter design, and impedance simulation [6–8, 13–15, 18].

Since the inverting version of the second generation current conveyor (ICCII) has proved to be a useful building block [3, 4, 15], in this paper a balanced-output inverting CCIII (ICCIII+−) is introduced. It is a four-terminal device. Its symbol is shown in Fig. 1(a).

E.A. Sobhy
Analog & Mixed-Signal Center (AMSC), Texas A&M University, College Station, TX 77843-3128, USA
e-mail: ehsobhy@neo.tamu.edu

A.M. Soliman (✉)
Electronics and Communications Engineering Department, Cairo University, Giza 12613, Egypt
e-mail: asoliman@ieee.org

The relation between terminal voltages and currents can be described using the following matrix equation:

$$\begin{pmatrix} I_{\mathrm{Y}} \\ V_{\mathrm{X}} \\ I_{\mathrm{Z}+} \\ I_{\mathrm{Z}-} \end{pmatrix} = \begin{pmatrix} 0 & -1 & 0 & 0 \\ -1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & -1 & 0 & 0 \end{pmatrix} \begin{pmatrix} V_{\mathrm{Y}} \\ I_{\mathrm{X}} \\ V_{\mathrm{Z}+} \\ V_{\mathrm{Z}-} \end{pmatrix}. \tag{1}$$

The positive and negative signs at the Z terminals define positive and negative Z output currents.

In the second section of this paper, a new CMOS realization of the ICCIII+− is proposed. The principle of the circuit operation will be described, followed by SPICE simulations. In the third section of this paper applications of the ICCIII+− are introduced to show how the ICCIII+− is powerful and attractive in many applications.

2 New CMOS Realization for the ICCIII+−

In this section a new CMOS realization for the ICCIII+− is proposed. The circuit description is introduced, followed by SPICE simulations for the DC and AC characteristics between the terminal voltages and currents.

2.1 Circuit Description

Figure 1(b) shows the new CMOS realization of the ICCIII+−. The input stage is formed from a single input transconductor stage, which uses two matched CMOS pairs (M_1–M_2, M_3–M_4) and two current mirrors (M_5–M_6 and M_7–M_8).

$$I_{\mathrm{M1,2}} = I_{\mathrm{M3,4}}, \tag{2}$$

$$\frac{K_{\mathrm{eff}}}{2}(V_{\mathrm{B1}} - V_{\mathrm{Y}} - V_{\mathrm{Teff}})^2 = \frac{K_{\mathrm{eff}}}{2}(V_{\mathrm{X}} - V_{\mathrm{B2}} - V_{\mathrm{Teff}})^2, \tag{3}$$

where

$$K_{\mathrm{eff}} = \frac{K_{\mathrm{n}}K_{\mathrm{p}}}{\sqrt{K_{\mathrm{n}}} + \sqrt{K_{\mathrm{p}}}}, \qquad V_{\mathrm{Teff}} = V_{\mathrm{Tn}} + |V_{\mathrm{Tp}}|. \tag{4}$$

From the above equations [9], the necessary condition for $V_{\mathrm{X}} = -V_{\mathrm{Y}}$ is that $V_{\mathrm{B1}} = -V_{\mathrm{B2}}$.

The output stage formed from two floating current sources (FCSs) was introduced in [2]. A feedback is made from the first current source (M_9–M_{14}) to achieve the current inversion between the X and Y terminals. The second FCS (M_{15}−M_{20}) is used to achieve the positive and negative current following action between the Z and X terminals. It worth noting that using FCSs will impose a restriction on the supply to be at least $2[V_{\mathrm{GS}} + V_{\mathrm{DS}}(sat)]$.

In the above analysis, the body of the transistors is connected to the source, which is necessary to make the threshold voltage constant for all transistors. This requires

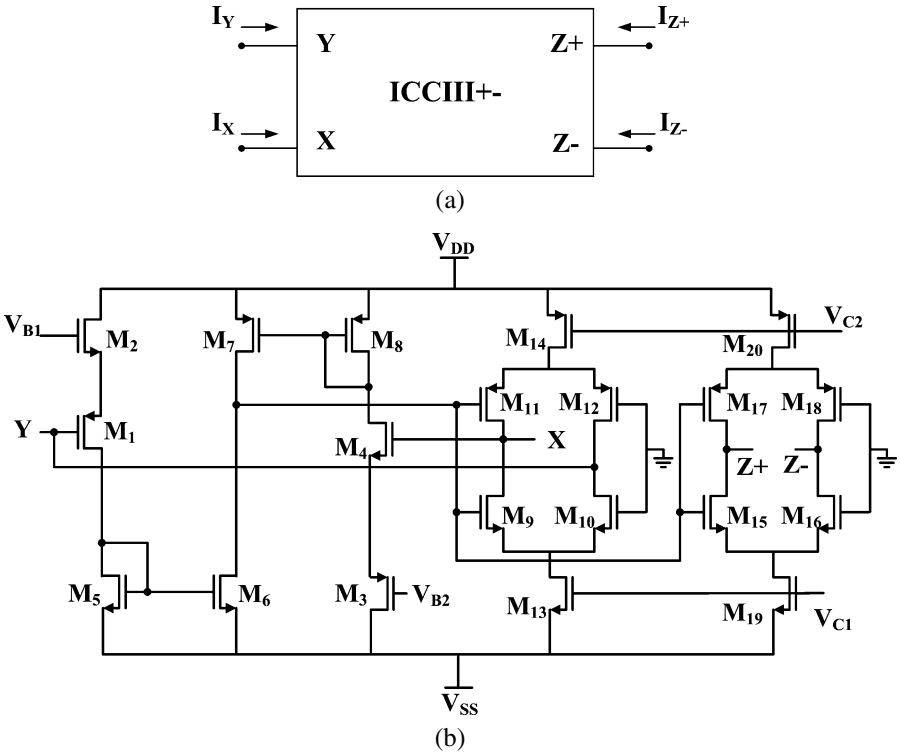


Fig. 1 (**a**) Block diagram of ICCIII+−. (**b**) The proposed ICCIII+− CMOS realization

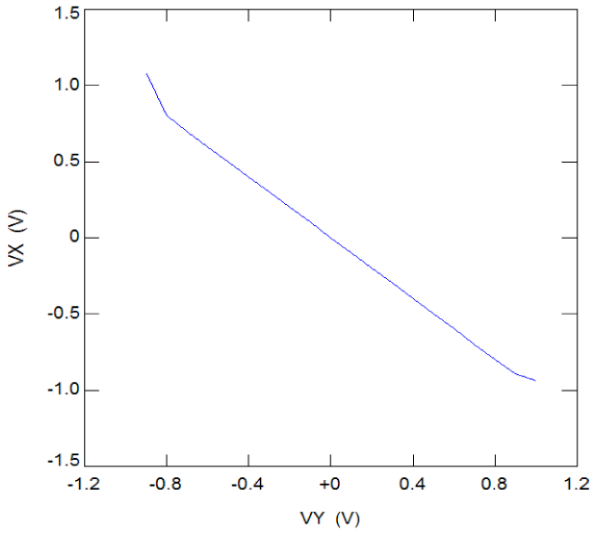
a twin-well process so that the NMOS and PMOS transistors can be separated in different wells. Although the twin-well CMOS process is available, it is not a standard VLSI technology.

2.2 Simulation Results

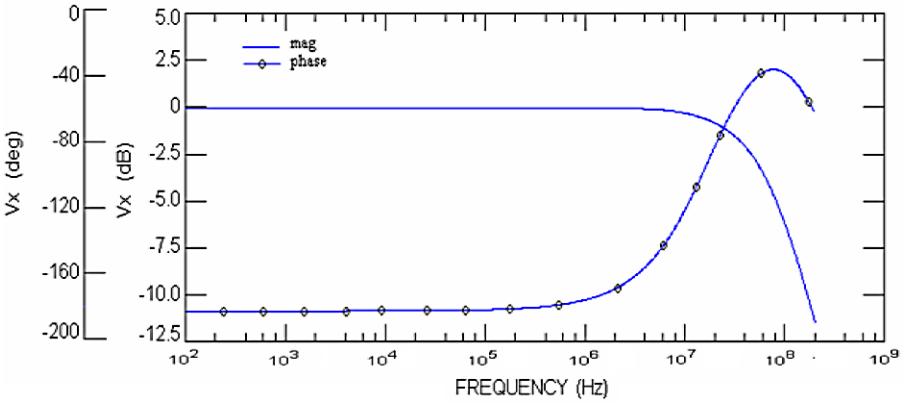
Transistor aspect ratios are given in Table 1. The supply voltages are taken as ±1.5 V. The simulation results are shown in Fig. 2 with a compensation capacitor of 0.25 pF connected between terminal X and the drain of M_8. The control voltages V_{B1} and V_{B2} are taken as ±1.45 V respectively, while V_{C1} is −0.4 V and V_{C2} is 0.1 V. The DC and AC characteristics between the Y and X terminal voltages are shown in Figs. 2(a) and 2(b) respectively. The DC and AC characteristics between the X and Y terminal currents are shown in Figs. 2(c) and 2(d) respectively. The DC and AC characteristics between the X and Z terminal currents are shown in Figs. 2(e) and 2(f) respectively. The total harmonic distortion is found to be 4% for a 1 MHz, 0.35 V, peak-to-peak sinusoidal input at terminal Y, and the terminal X input resistance is 8.4 Ω. Also, the total power dissipation is 0.9 mW.

Table 1 Transistor aspect ratios of the ICCIII+− shown in Fig. 1(b)

Transistor	W (μm)/L (μm)
M1, M2, M3, M4	35/1.05
M5, M6	8.75/1.05
M7, M8	26.25/1.05
M9, M10, M15, M16	35/0.35
M11, M12, M17, M18	70/0.35
M13, M19	27.65/1.05
M14, M20	57.75/1.05

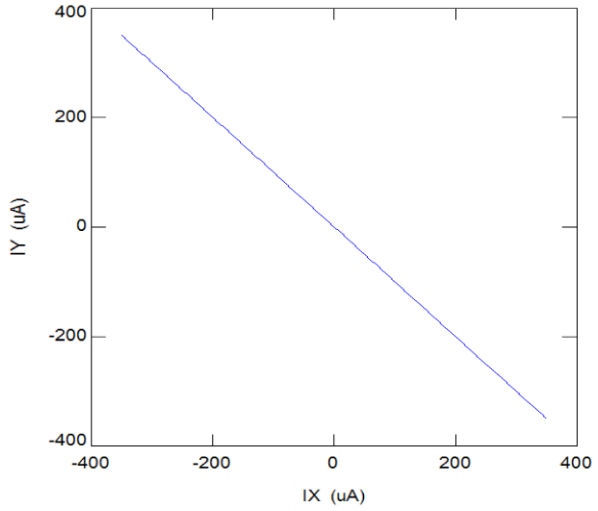


(a)

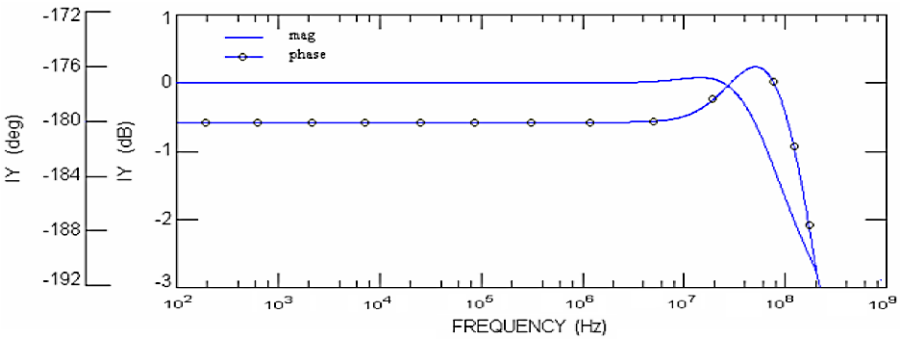


(b)

Fig. 2 Simulation results of the proposed ICCIII+−



(c)



(d)

Fig. 2 (*Continued*)

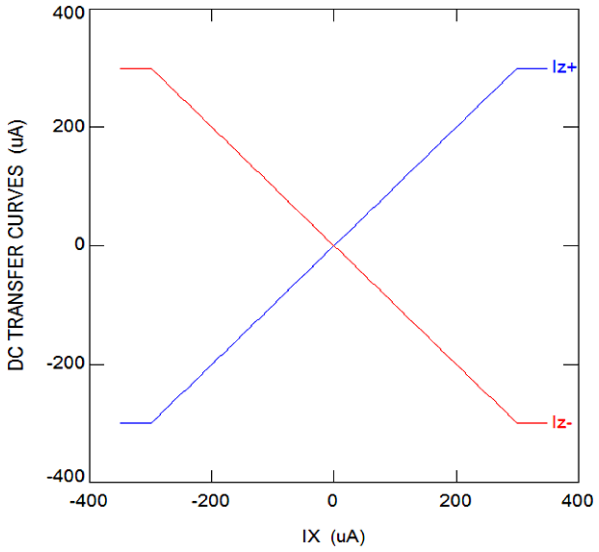
3 Applications of the Balanced-Output ICCIII

In the following sections, the applications of the balanced-output ICCIII in realizing a MOS ICCIII+− voltage-to-current converter and a MOS-C ICCIII+− lossless integrator are given. SPICE simulations are given to verify the analytical results.

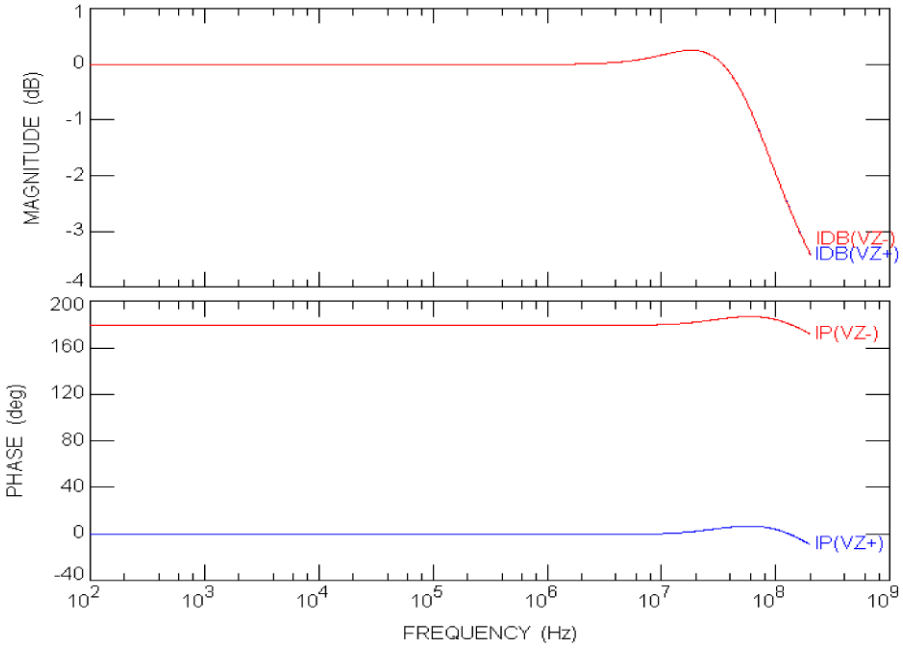
3.1 MOS ICCIII+− Transconductor

A voltage-to-current converter is introduced in this subsection. The structure, as shown in Fig. 3(a), is based on using a MOS transistor operating in the nonsaturation region and connected between the X and Y terminals of the ICCIII+−. Even nonlinearity cancellation of the MOS transistor is done using this structure. In this case, the output currents are given by

$$I_{Z+} = -I_{Z-} = GV_{IN}, \tag{5}$$



(e)



(f)

Fig. 2 (*Continued*)

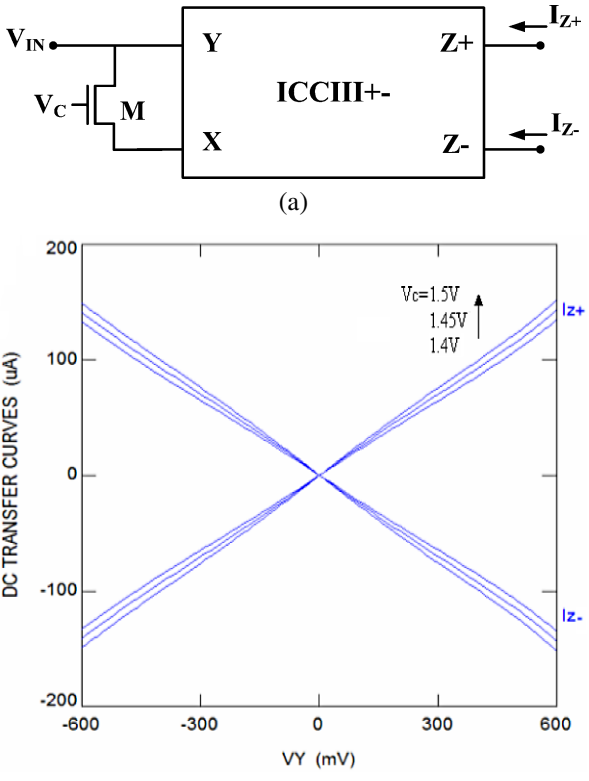


Fig. 3 (**a**) The proposed MOS ICCIII+− voltage-to-current converter. (**b**) Output currents of the MOS ICCIII+− transconductor

where

$$G = 2K(V_C - V_T) \text{ and } K = \mu_n C_{ox} \frac{W}{L}. \tag{6}$$

Figure 3(b) shows the output currents of the MOS ICCIII+− voltage-to-current converter for different values of the control gate voltage. The basic idea here is based on the fact that $I_X = -I_Y$, so the current in the MOS transistor leaving the X terminal is entering the Y of the same ICCIII and vice versa. The current is linearized by the fact that $V_X = -V_Y$ and transferred to Z+ and Z−.The current circulation in this case is between the Y and X terminals of the ICCIII. Although it is a different situation, it is worth noting that the current circulation between the X and Z− terminals of a CCII was used before in [1].

3.2 MOS-C ICCIII+− Lossless Integrator

By adding capacitors at the output terminals of the MOS ICCIII+− voltage-to-current converter, a lossless integrator can be obtained, as shown in Fig. 4(a). The output voltage of the integrator is given by

$$V_{Z+} = -V_{Z-} = \frac{G}{sC} V_{IN}. \tag{7}$$

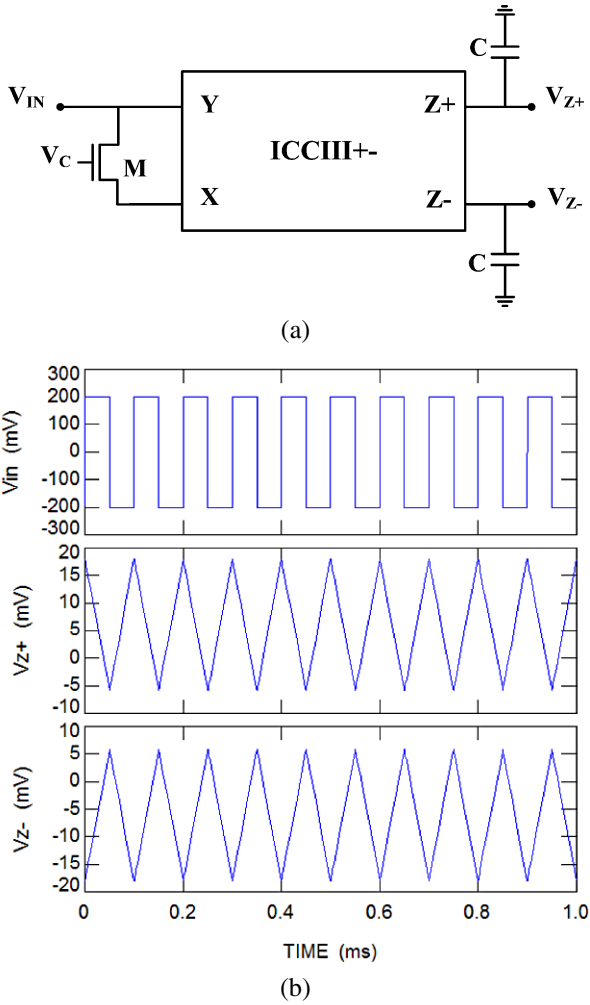


Fig. 4 (**a**) The proposed MOS-C ICCIII+− lossless integrator. (**b**) The output of the MOS-C ICCIII+− integrator with a square wave input signal

SPICE simulation results for the integrator are shown in Fig. 4(b) with a square wave input of 0.4 V peak-to-peak amplitude and a frequency of 10 kHz.

3.3 Balanced-Output ICCIII MOS-C Filters

In the following subsections, second-order MOS-C balanced output ICCIII filters are proposed. These filters have an input voltage terminal and both voltage and current output terminals.

3.3.1 The MOS-C balanced-output ICCIII Tow-Thomas filter

Figure 5 represents a filter circuit and block diagram which realizes second-order lowpass and bandpass responses. The outputs exist in voltage and current modes.

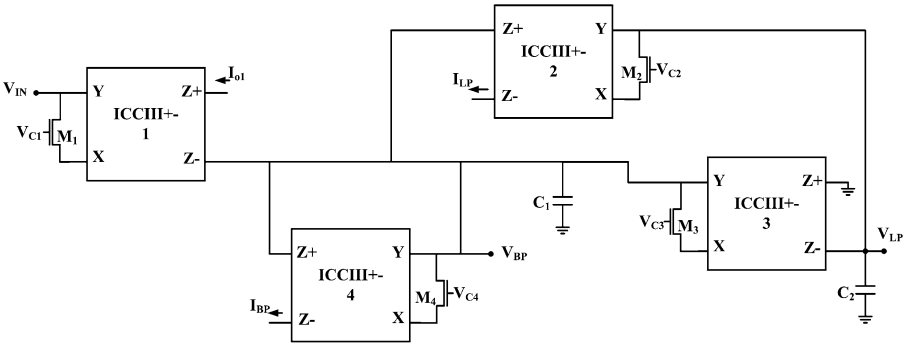


Fig. 5 The Tow-Thomas MOS-C ICCIII+− filter circuit

The filter includes four MOS-C balanced outputs ICCIII and two grounded capacitors, which make it suitable for VLSI implementation. The filter is considered to be another form of the well-known Tow-Thomas biquad filter which is realized using operational amplifiers [5], CCIIs [17], and transconductors [12].

By direct analysis, the following transfer functions are obtained:

$$\frac{V_{\mathrm{BP}}}{V_{\mathrm{IN}}} = \frac{s\frac{G_1}{C_1}}{D(s)}, \qquad \frac{I_{\mathrm{BP}}}{V_{\mathrm{IN}}} = \frac{s\frac{G_1G_4}{C_1}}{D(s)}, \tag{8}$$

$$\frac{V_{\mathrm{LP}}}{V_{\mathrm{IN}}} = \frac{\frac{G_1G_3}{C_1C_2}}{D(s)}, \qquad \frac{I_{\mathrm{LP}}}{V_{\mathrm{IN}}} = \frac{\frac{G_1G_2G_3}{C_1C_2}}{D(s)}, \tag{9}$$

where

$$D(s) = s^2 + s\frac{G_4}{C_1} + \frac{G_2G_3}{C_1C_2}. \tag{10}$$

From the above equations, the ω_{o} and Q of the filter are given by

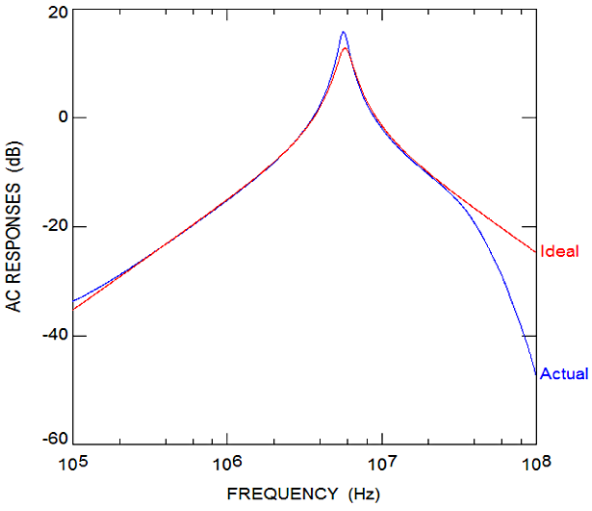
$$\omega_{\mathrm{o}} = \sqrt{\frac{G_2G_3}{C_1C_2}}, \qquad Q = \frac{1}{G_4}\sqrt{\frac{G_2G_3C_1}{C_2}}. \tag{11}$$

We can notice from the above equations that the proposed filter has the advantage of controlling the gain using G_1 without affecting ω_{o} and Q. Also, G_4 controls Q without affecting ω_{o} and the gain, but unfortunately, ω_{o} cannot be controlled independently.

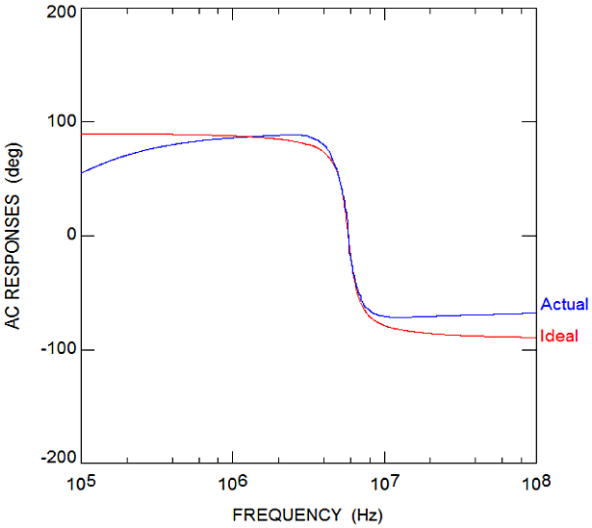
Besides the proposed filter circuit, three other filter circuits can be obtained with different polarities for the lowpass and bandpass responses. This is achieved by simply reversing the output Z terminals of the MOS ICCIII+−s.

SPICE simulations for the filter shown in Figs. 6(a), 6(b) are done to verify the bandpass responses for both the voltage and current outputs. The filter elements are chosen to have $f_{\mathrm{o}} = 5.5$ MHz and $Q = 7$.

Also, simulations for the same filter are done to verify the lowpass responses for both the voltage and current outputs. The filter elements are chosen to have maximally flat responses with $f_{\mathrm{o}} = 700$ kHz. Simulation results are shown in Figs. 6(c) and 6(d).



(a)



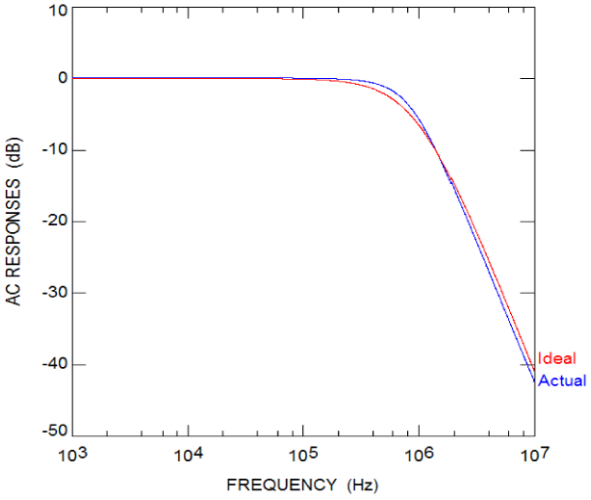
(b)

Fig. 6 (**a**) The magnitude response of the voltage bandpass output compared with the ideal curve. (**b**) The phase response of the voltage bandpass output compared with the ideal curve. (**c**) The magnitude response of the voltage lowpass output compared with the ideal curve. (**d**) The phase response of the voltage lowpass output compared with the ideal curve

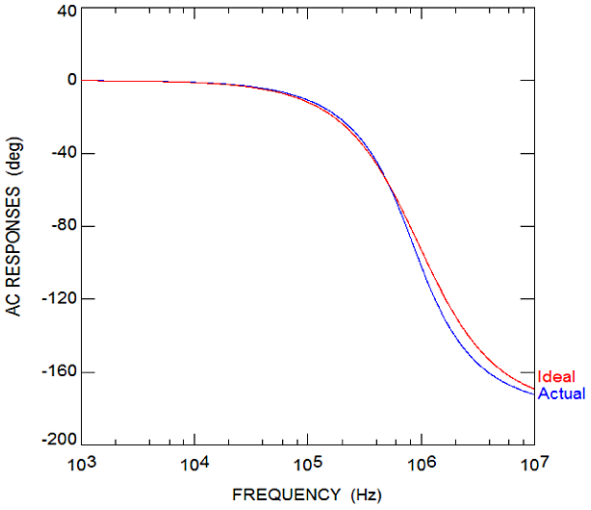
3.3.2 The MOS-C balanced-output ICCIII Kerwin–Huelsman–Newcomb filter

Figure 7 represents the second proposed filter circuit and block diagram which realizes second-order lowpass, highpass, and bandpass responses. The outputs exist in voltage and current modes. The filter consists of six MOS-C balanced outputs ICCIII and two grounded capacitors, which makes it suitable for VLSI implementation. The filter is considered another form of the well-known Kerwin–Huelsman–Newcomb (KHN) biquad filter, which is realized using operational amplifiers [10], CCIIs [16], and transconductors [11].

Fig. 6 (*Continued*)



(c)



(d)

By direct analysis, the following transfer functions are obtained:

$$\frac{V_{\mathrm{LP}}}{V_{\mathrm{IN}}}=\frac{\frac{G_1G_2G_3}{G_6C_1C_2}}{D(s)},\qquad \frac{I_{\mathrm{LP}}}{V_{\mathrm{IN}}}=\frac{\frac{G_1G_2G_3G_4}{G_6C_1C_2}}{D(s)}, \tag{12}$$

$$\frac{V_{\mathrm{BP}}}{V_{\mathrm{IN}}}=\frac{s\frac{G_1G_2}{G_6C_1}}{D(s)},\qquad \frac{I_{\mathrm{BP1}}}{V_{\mathrm{IN}}}=\frac{s\frac{G_1G_2G_3}{G_6C_1}}{D(s)},\qquad \frac{I_{\mathrm{BP2}}}{V_{\mathrm{IN}}}=\frac{s\frac{G_1G_2G_5}{G_6C_1}}{D(s)}, \tag{13}$$

$$\frac{V_{\mathrm{HP}}}{V_{\mathrm{IN}}}=\frac{s^2\frac{G_1}{G_6}}{D(s)},\qquad \frac{I_{\mathrm{HP1}}}{V_{\mathrm{IN}}}=\frac{s^2\frac{G_1G_2}{G_6}}{D(s)},\qquad \frac{I_{\mathrm{HP2}}}{V_{\mathrm{IN}}}=\frac{s^2G_1}{D(s)}, \tag{14}$$

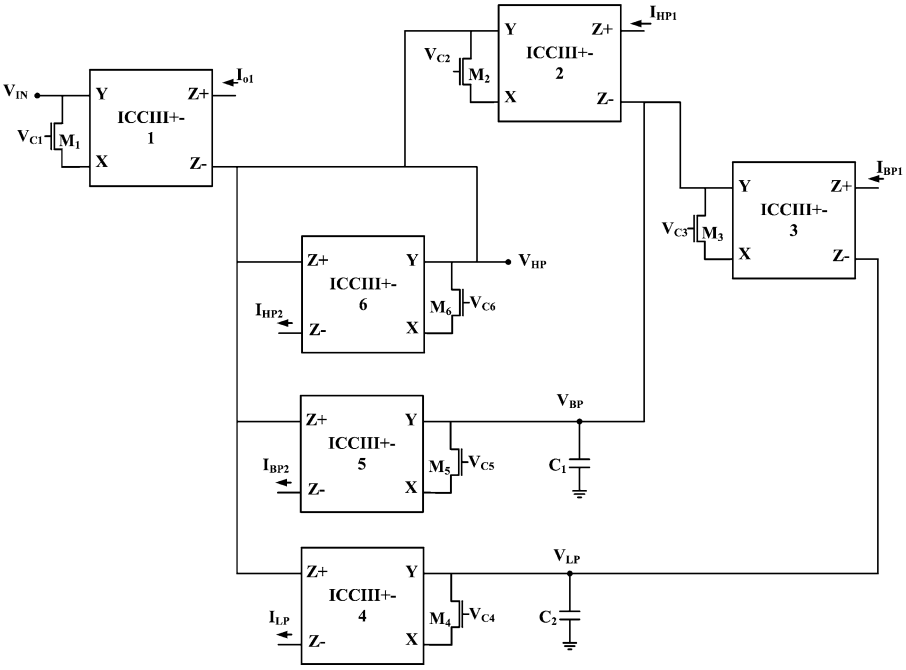


Fig. 7 The KHN MOS-C ICCIII+− filter circuit

where

$$D(s) = s^2 + s\frac{G_2G_5}{G_6C_1} + \frac{G_2G_3G_4}{G_6C_1C_2}. \tag{15}$$

From the above equations, the ω_o and Q of the filter are given by

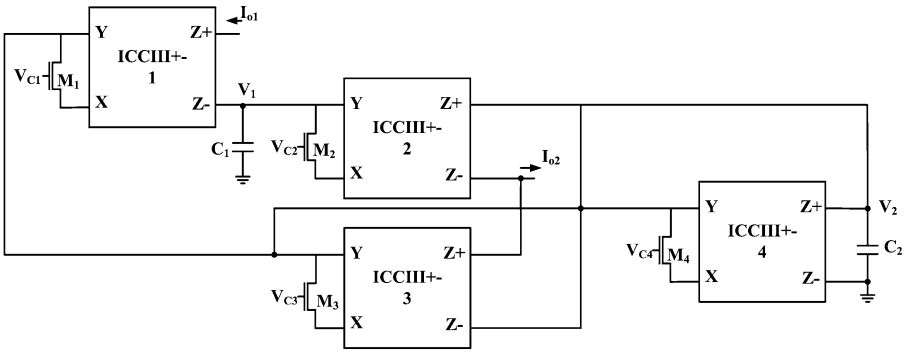
$$\omega_o = \sqrt{\frac{G_2G_3G_4}{G_6C_1C_2}}, \qquad Q = \frac{1}{G_5}\sqrt{\frac{G_3G_4G_6C_1}{G_2C_2}} \tag{16}$$

We can notice from the above equations that the proposed filter has the advantage of controlling the gain using G_1 without affecting ω_o and Q. Also G_5 controls Q without affecting ω_o and the gain, but unfortunately, ω_o cannot be controlled independently.

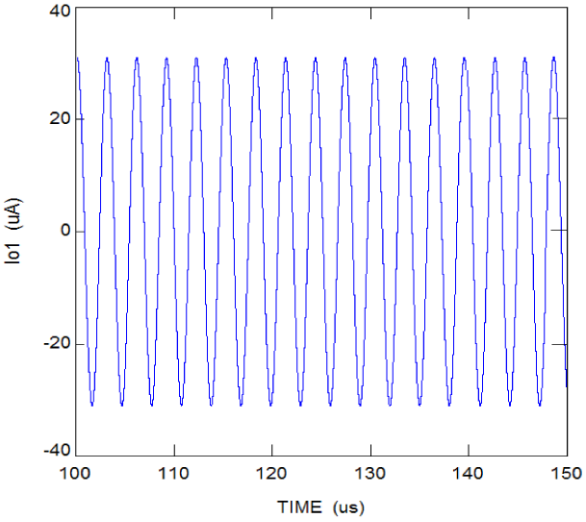
Besides the proposed filter circuit, seven other filter circuits can be obtained with different polarities for the lowpass, bandpass, and highpass responses. This is achieved by simply reversing the output Z terminals of the MOS ICCIII+−s.

3.4 MOS-C ICCIII+− Current-Mode Oscillator

A proposed oscillator circuit employing four MOS-C ICCIII+−s and two grounded capacitors is shown in Fig. 8(a). The oscillator is obtained from the previously reported transconductor-based oscillator [11] by modifying it using the MOS ICCIII+−.



(a)



(b)

Fig. 8 (**a**) The proposed MOS-C ICCIII+− oscillator. (**b**, **c**) The output current waveforms of the proposed oscillator

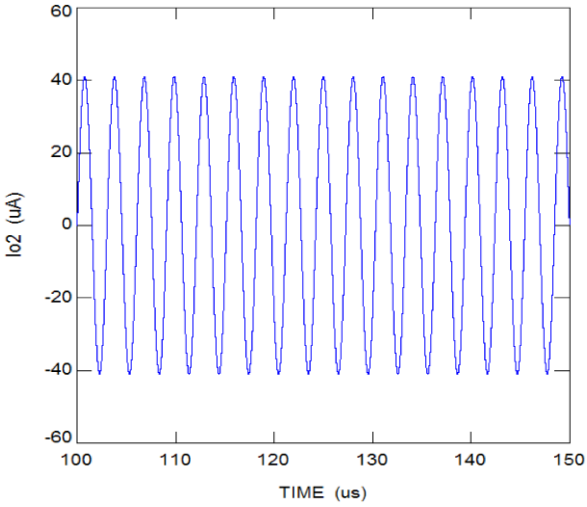
The state equations of the proposed oscillator are given as follows:

$$\begin{pmatrix} \frac{dv_1}{dt} \\ \frac{dv_2}{dt} \end{pmatrix} = \begin{pmatrix} 0 & \frac{G_1}{C_1} \\ \frac{-G_2}{C_2} & \frac{1}{C_2}(G_3 - G_4) \end{pmatrix} \begin{pmatrix} v_1 \\ v_2 \end{pmatrix}. \tag{17}$$

From (17), the condition of oscillation and the radian frequency of oscillation are given, respectively, by

$$G_3 = G_4, \qquad \omega_o = \sqrt{\frac{G_1 G_2}{C_1 C_2}}. \tag{18}$$

Fig. 8 (*Continued*)



(c)

The advantage of the proposed oscillator circuit is that both the oscillation frequency and the oscillation condition can be adjusted independently.

A simulation is done for the proposed oscillator, and the results for the output current waveforms are shown in Figs. 8(b), 8(c). The circuit elements are chosen to achieve $f_o = 330$ kHz.

4 Conclusion

A new inverting balanced-output third generation current conveyor block is introduced. A CMOS realization for this block is proposed, and applications utilizing the introduced block are given. These applications are a MOS ICCIII+− voltage-to-current converter, a MOS-C ICCIII+− lossless integrator, MOS-C ICCIII+− filters, and a MOS-C ICCIII+− oscillator. SPICE simulations confirm the analytical results.

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