A Novel Fully Differential Current Conveyor and Applications for Analog VLSI

Ahmed A. El-Adawy, Ahmed M. Soliman, and Hassan O. Elwan

***Abstract*—In this paper, a novel fully differential second-generation current conveyor (FDCCII) is presented. The proposed block is useful in mixed-mode applications where fully differential signal processing is required. Furthermore, the FDCCII can be used to realize MOSFET-C filters. The circuit has a bandwidth of about 10 MHz under heavy capacitive loads and can operate from low supply voltages down to ±1.5 V.**

***Index Terms*—Class AB operation, current conveyor, fully differential, transconductor.**

I. Introduction

ONE of the standard techniques to extend the dynamic range of analog blocks is to use fully differential (FD) signal processing. It can extend the dynamic range over one order of magnitude through the cancellation of even harmonics, as well as the suppression of all undesirable common mode (CM) signals. These undesirable signals can be generated by analog or digital blocks in mixed-mode circuits. However, digital circuits are the most serious source of noise due to clock feedthrough and charge injection. Besides being useful in increasing the dynamic range of analog blocks, FD implementations are useful in some analog signal processing, such as MOSFET-C filters.

The purpose of this paper is to introduce a novel FDCCII. The proposed block is an extension of the second-generation current conveyor (CCII) introduced by Sedra and Smith [1] in 1970. The CCII is a versatile building block and is described by the following matrix equation:

$$\begin{bmatrix} V_X \\ I_Z \\ I_Y \end{bmatrix} = \begin{bmatrix} 0 & 0 & 1 \\ 1 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_X \\ V_Z \\ V_Y \end{bmatrix}. \tag{1}$$

Because of the voltage and current conveying properties, CCII circuits may be used to synthesize many analog functions that may not be easily realizable using other building blocks [2]–[8]. Since the introduction of the CCII, many modifications are added to increase the versatility of the block. The modified differential current conveyor (MDCC) [2] and the differential voltage current conveyor (DVCC) [3] are examples of those modifications. However, only one or two of the three terminals of the CCII are made differential in these modifications. Up until now, no FD current conveyor is presented.

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II. The Fully Differential CCII

The FDCCII is an eight-terminal analog building block shown symbolically in Fig. 1(a) with a describing matrix equation of the form

$$\begin{bmatrix} V_{X+} \\ V_{X-} \\ I_{Z+} \\ I_{Z-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 1 & -1 & 1 & 0 \\ 0 & 0 & -1 & 1 & 0 & 1 \\ 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_{X+} \\ I_{X-} \\ V_{Y1} \\ V_{Y2} \\ V_{Y3} \\ V_{Y4} \end{bmatrix} \tag{2}$$

It should be noted that $V_{X+} = -V_{X-}$ if $V_{Y3} = V_{Y4} = 0$. A CMOS realization of the FDCCII is shown in Fig. 1(b). All transistors are assumed to be operating in the saturation region. The input voltage is applied to the gates of the differential pair transistors M1 and M2. As a result, the drain currents of these transistors are given by

$$I_1 = \frac{I_B}{2} + \Delta I \tag{3}$$

$$I_2 = \frac{I_B}{2} - \Delta I \tag{4}$$

where ΔI is function only of the input differential voltage $(V_{Y1} - V_{Y2})$ and is given by

$$\Delta I = \frac{\sqrt{KI_B}}{2}(V_{Y1} - V_{Y2})\sqrt{1 - \frac{K(V_{Y1} - V_{Y2})^2}{4I_B}} \tag{5}$$

where K is the transconductance parameter of the input transistors

$$K = \mu_n C_{\rm OX}\frac{W}{L}. \tag{6}$$

By applying KCL at nodes a and b, it can be shown that

$$I_1 + I_4 = I_7 = I_B \tag{7}$$

$$I_2 + I_5 = I_9 = I_B \tag{8}$$

where I_j is the current flowing in the transistor M_j $(j = 1, 2, \cdots)$. From (3)–(5), (7), and (8), it can be shown that

$$I_4 = \frac{I_B}{2} - \Delta I \tag{9}$$

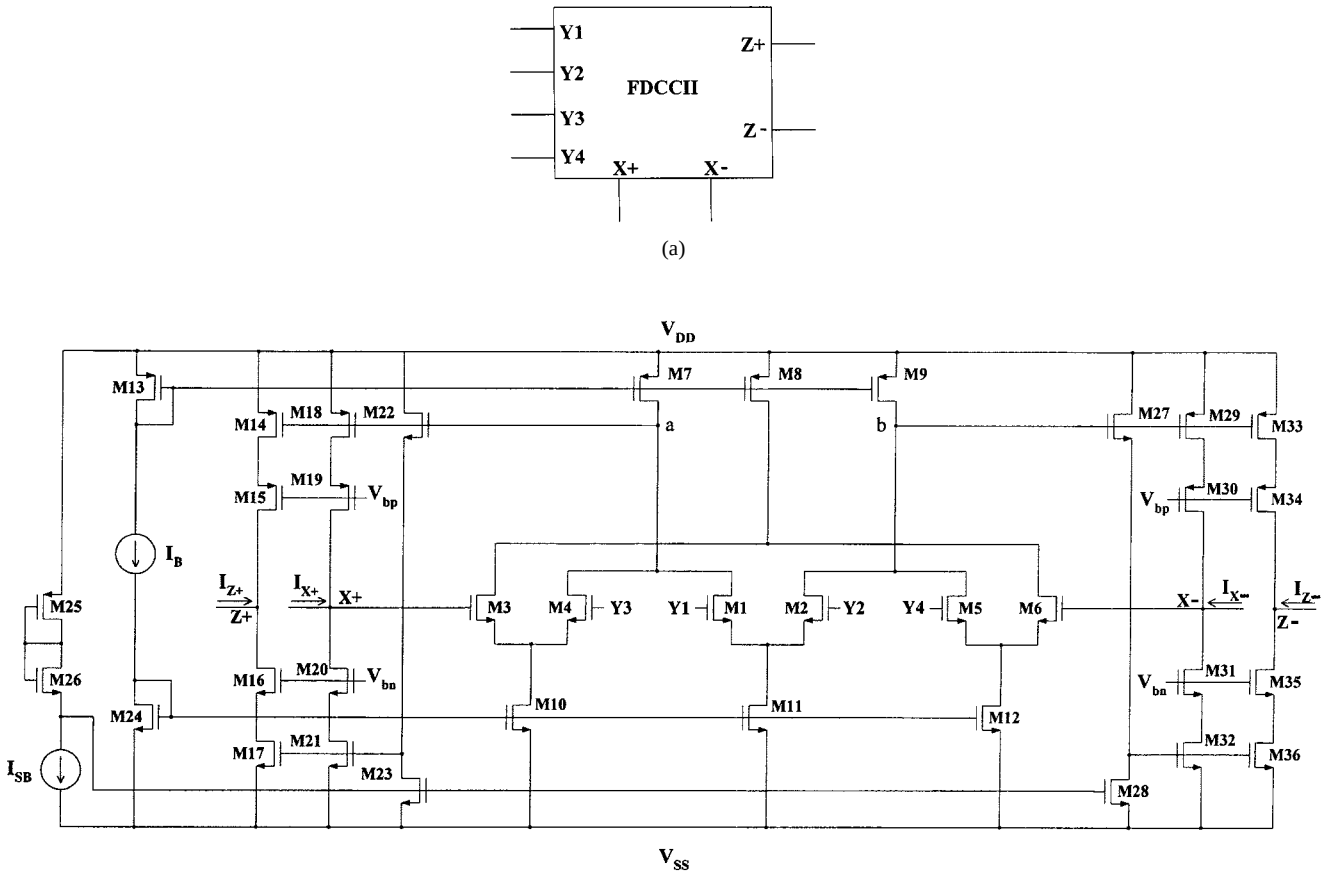

Fig. 1. The proposed FDCCII (a) symbol and (b) CMOS realization.

TABLE I
TRANSISTOR ASPECT RATIO (W/L)

Transistor	Aspect ratio (W/L)
M1, M2, M3, M4, M5, M6	60/4.8
M7, M8, M9, M13	480/4.8
M10, M11, M12, M24	120/4.8
M14, M15, M18, M19, M25, M29, M30, M33, M34	240/2.4
M16, M17, M20, M21, M26, M31, M32, M35, M36	60/2.4
M22, M23, M27, M28	4.8/4.8

$$I_5 = \frac{I_B}{2} + \Delta I. \tag{10}$$

Hence

$$\Delta I = \frac{\sqrt{KI_B}}{2}(V_{X+} - V_{Y3})\sqrt{1 - \frac{K(V_{X+} - V_{Y3})^2}{4I_B}} \tag{11a}$$

$$= \frac{\sqrt{KI_B}}{2}(V_{Y4} - V_{X-})\sqrt{1 - \frac{K(V_{Y4} - V_{X-})^2}{4I_B}}. \tag{11b}$$

From (5) and (11), it is clear that

$$V_{X+} = V_{Y3} + (V_{Y1} - V_{Y2}) \tag{12a}$$

$$V_{X-} = V_{Y4} - (V_{Y1} - V_{Y2}). \tag{12b}$$

Furthermore

$$I_{Z+} = I_{X+} \tag{13}$$

and similarly

$$I_{Z-} = I_{X-}. \tag{14}$$

It is worth mentioning that the proposed FDCCII can be divided into two separate CCII's by connecting $Y1$ and $Y2$ terminals to ground by using $Y3, X+$, and $Z+$ as the terminals of the first CCII and $Y4, X-, Z-$ as the terminals of the second CCII.

The transistors M18–M23 form the class-AB output stage for the $X+$ terminal. The operation of the class-AB output stage can be described as follows. If a current is withdrawn from the $X+$ terminal, the gate voltage of M18 decreases. By the action of the level shift transistors M22 and M23, the gate voltage of M21 decreases as well. Thus, the current through M21 decreases as the current in M18 increases. The level shift voltage is used to adjust the standby current of the loop. It can be shown that

$$V_{\mathrm{SG18}} + V_{\mathrm{GS22}} + V_{\mathrm{GS21}} = V_{\mathrm{DD}} - V_{\mathrm{SS}} \tag{15}$$

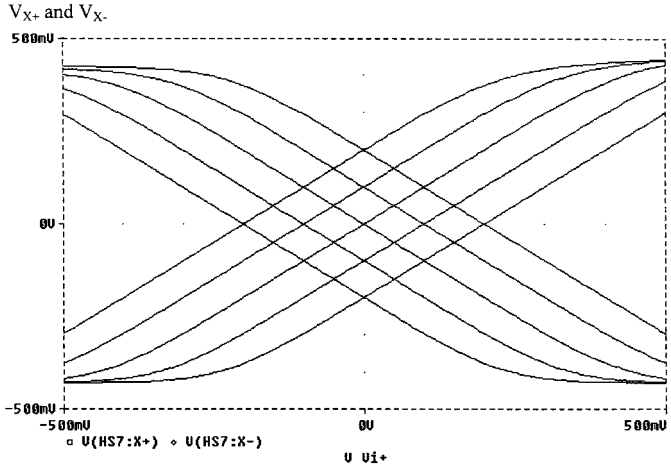

Fig. 2. V_{X+} and V_{X-} versus V_{Y+} for different values of V_{Y-}.

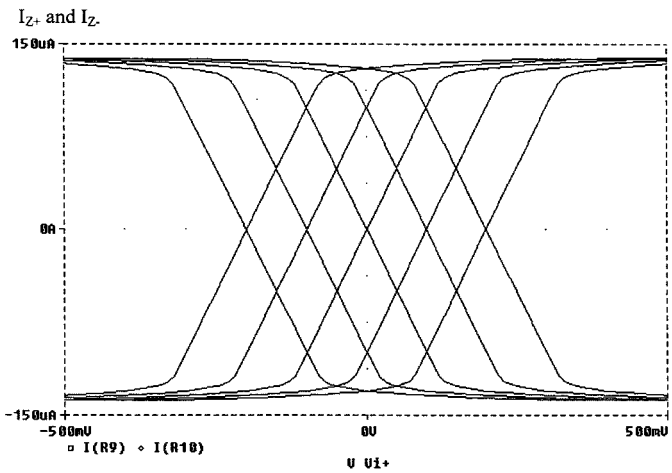

Fig. 3. I_{Z+} and I_{Z-} versus V_{Y+} when $R_X = 10$ kΩ.

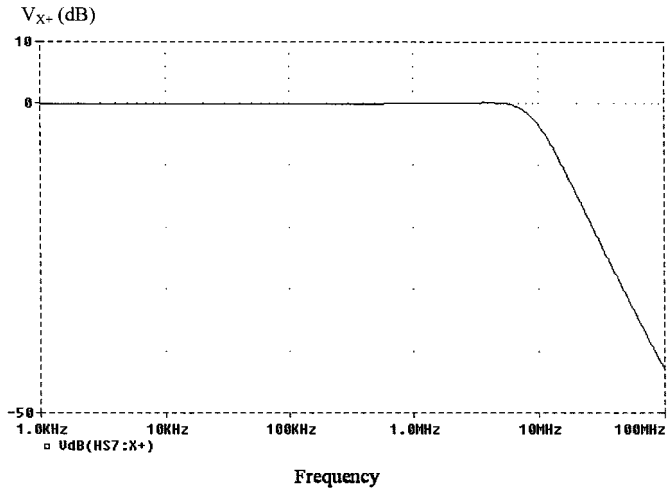

Fig. 4. Frequency response of the X terminal voltage when $R_X = 1$ kΩ.

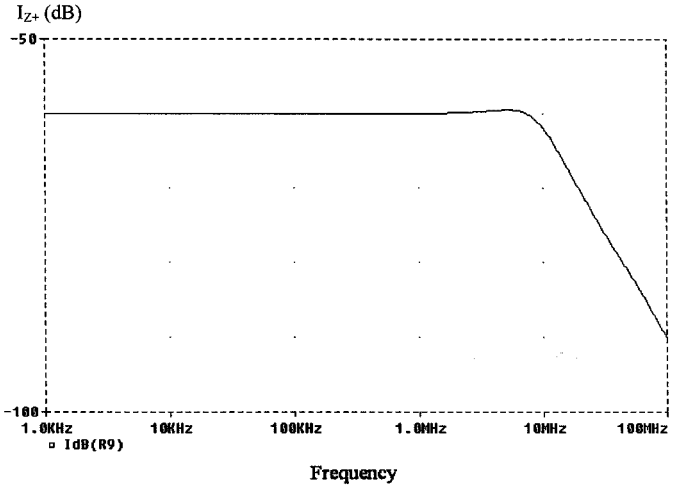

Fig. 5. Frequency response of the Z terminal current when $R_Z = 1$ kΩ.

The two-level shift transistors M22 and M23 have the same current. If these transistors are matched, then

$$V_{\mathrm{GS22}} = V_{\mathrm{GS23}}. \tag{17}$$

From (15), (16), and (17), and noting that $V_{\mathrm{SG14}} = V_{\mathrm{SG18}}$, it can be shown that the standby current in the output stage is given by

$$I_{14} = I_{18} = I_{\mathrm{SB}}. \tag{18}$$

The proposed FDCCII has been simulated with PSPICE using the AMI 1.2 μm CMOS technology provided by MOSIS. The aspect ratios of the transistors are given in Table I. Simulations are performed with the X terminals connected to 1-kΩ resistances and 10-pF capacitances and the Z terminals connected to 10-kΩ resistances. The supply voltages used are $\pm$1.5 V, while the tail current I_B is 50 μA and the standby current I_{SB} is 20 μA. Fig. 2 shows the dc voltage characteristics of the two terminals $X+$ and $X-$ versus V_{Y1} when $V_{Y3} = V_{Y4} = 0$ V and V_{Y2} is swept from -0.2 to 0.2 V in steps of 0.1 V. The output currents I_{Z+} and I_{Z-} versus V_{Y+} are shown in Fig. 3. The X terminal voltage frequency response of the FDCCII is shown in Fig. 4, from which it can be seen that the bandwidth is 10 MHz. Fig. 5 shows the frequency response of the Z terminal current.

III. Differential Input Transconductor

The FDCCII can be used to implement a differential input balanced output transconductor as shown in Fig. 6. The transistor M1 is operating in the ohmic region where the current is given by

$$I = K\left[(V_G - V_T)(V_D - V_S) - \frac{1}{2}\left(V_D^2 - V_S^2\right)\right] \tag{19}$$

where V_T is the threshold voltage of the nMOS transistor.

From Fig. 6

$$V_{Y3} = Y_{Y4} = 0 \tag{20}$$

$$V_{\mathrm{SG25}} + V_{\mathrm{GS26}} + V_{\mathrm{GS23}} = V_{\mathrm{DD}} - V_{\mathrm{SS}}. \tag{16}$$

$$V_{X+} = -V_{X-} = V_1 - V_2 \tag{21}$$

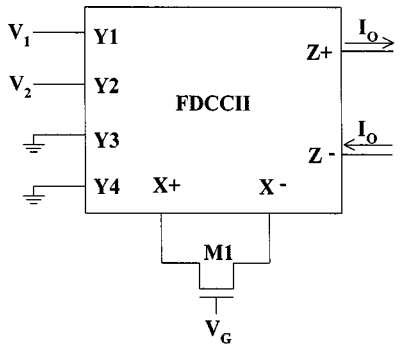

Fig. 6. A differential input balanced output transconductor using the proposed FDCCII.

Hence, from (19) and (21), it can be shown that

$$I_O = 2K(V_G - V_T)(V_1 - V_2). \tag{22}$$

Thus, the output current is proportional to the input differential voltage and the transconductance is given by

$$G = 2K(V_G - V_T). \tag{23}$$

Therefore, the transconductance can be tuned by varying the gate voltage. Another advantage is that the transconductance is realized using a single transistor external to the FDCCII. Hence, there are no matching requirements in the external components.

IV. Four-Quadrant Multiplier

Fig. 7 shows a four-quadrant multiplier using two FDCCII and two matched transistors M1 and M2 operating in the ohmic region. The output of the lower FDCCII is given by

$$I_{O2} = 2K(V_{G2} - V_C - V_T)(V_1 - V_2). \tag{24}$$

The two balanced output currents of this FDCCII are subtracted from the current in the transistor M1 to give the following output:

$$I_{O1} = 2K(V_{G1} - V_{G2})(V_1 - V_2). \tag{25}$$

Hence, a four-quadrant analog transconductance multiplier is obtained. Fig. 8 shows the output current I_{O1} versus V_1 when $V_2 = 0$ V, $V_C = -0.25$ V, $V_{G2} = 1.25$ V, and $V_{G1} = 1$ to 1.5 V in steps of 0.05 V.

V. Second-Order Universal Filters

Fig. 9 shows a second-order mixed-mode MOSFET-C universal filter. The filter is based on the differential input balanced output transconductor described in the previous section. The high-pass, bandpass, and low-pass responses are given, respectively, by

$$I_{\mathrm{HP}} = -V_I \frac{s^2 G_1}{D(s)} \tag{26}$$

$$I_{\mathrm{BP}} = V_I \frac{s\frac{G_1 G_2}{C_1}}{D(s)} \tag{27}$$

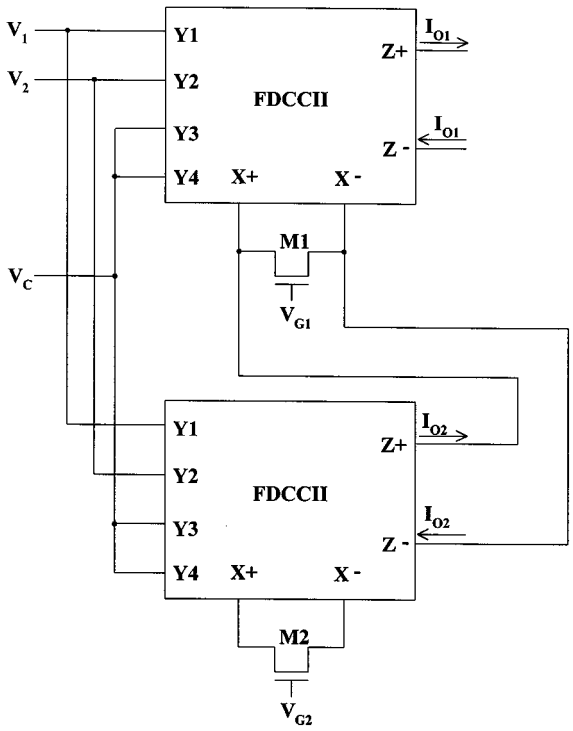

Fig. 7. A four-quadrant multiplier.

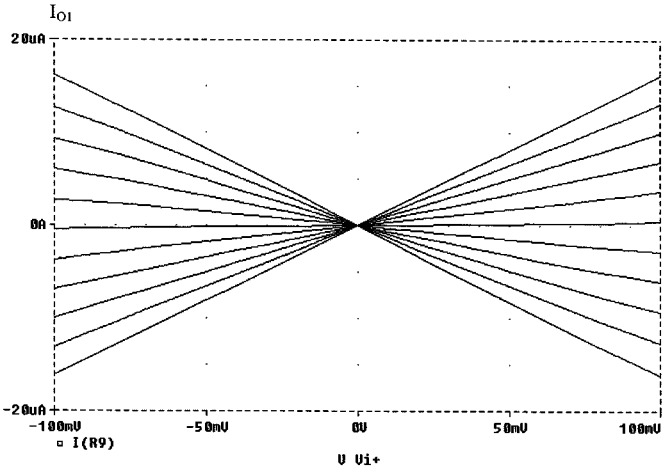

Fig. 8. The output current I_{O1} versus the V_1 for different values of V_{G1}.

$$I_{\mathrm{LP}} = -V_1 \frac{\frac{G_1 G_2 G_3}{C_1 C_2}}{D(s)} \tag{28}$$

where

$$D(s) = s^2 + s\frac{G_1}{C_1} + \frac{G_1 G_2}{C_1 C_2} \tag{29}$$

$$G_i = 2K_i(V_{G_i} - V_T), \quad i = 1, 2, 3. \tag{30}$$

It can be shown that a universal notch response can be obtained by connecting the low-pass and high-pass terminals. Also, by connecting the low-pass, bandpass, and high-pass terminals, an all-pass response is obtained provided that $G_1 = G_2 = G_3$ and

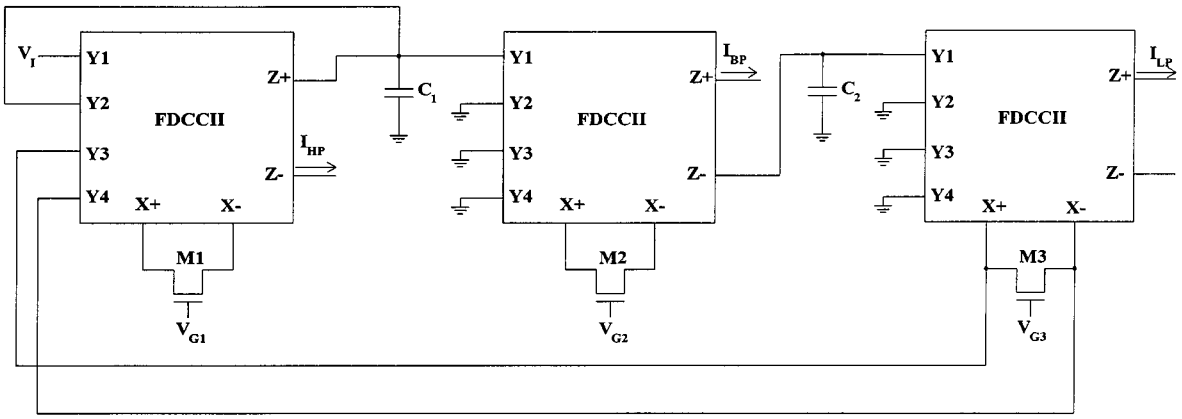

Fig. 9. A universal mixed-mode second-order filter (realization I).

$C_1 = C_2$. The phase response of the all-pass filter is shown in Fig. 10, where $K_1 = K_2 = K_3 = 75\ \mu$A/V^2 and $C_1 = C_2 = 20$ pF.

To demonstrate the functionality and versatility of the FD-CCII, another realization of the universal mixed-mode filter is shown in Fig. 11. The output current responses are expressed as

$$I_{\rm HP} = V_I \frac{s^2 G_1}{D(s)} \tag{31}$$

$$I_{\rm BP} = -V_I \frac{s\frac{G_1 G_2}{C_1}}{D(s)} \tag{32}$$

$$I_{\rm LP} = V_I \frac{\frac{G_1 G_2 G_3}{C_1 C_2}}{D(s)} \tag{33}$$

where $D(s)$ and G_i are given by (29) and (30), respectively. Hence, the output currents are the same as those of the filter in Fig. 9, but with inverted signs.

The above two filters have the drawback that there is no independent control on Q. Fig. 12 shows a third realization of a second order universal filter with independent control on Q, which is characterized by the following equations:

$$I_{\rm HP} = -V_I \frac{s^2 G_1}{D(s)} \tag{34}$$

$$V_{\rm BP} = V_I \frac{s\frac{G_1}{C_1}}{D(s)} \tag{35}$$

$$V_{\rm LP} = -V_I \frac{\frac{G_1 G_2}{C_1 C_2}}{D(s)} \tag{36}$$

where

$$D(s) = s^2 + \frac{G_1}{C_1}s + \frac{G_2 G_3}{C_1 C_2} \tag{37}$$

and

$$G_i = 2K_i(V_{G_i} - V_T) \quad i = 1, 2, 3. \tag{38}$$

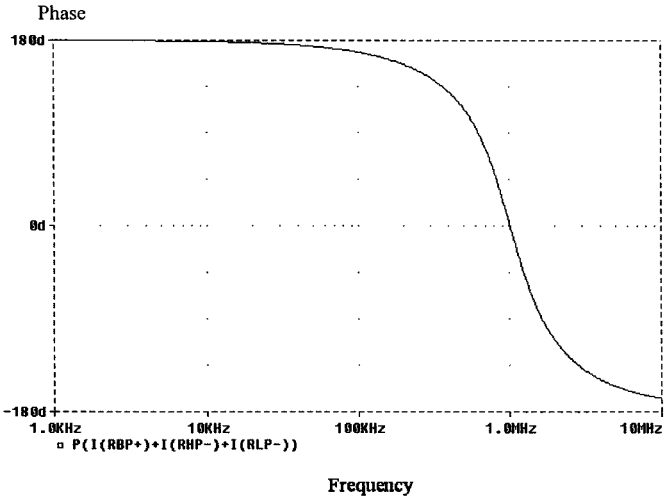

Fig. 10. All-pass response.

Fig. 13 shows the bandpass response of this filter with $C_1 = C_2 = 20$ pF, $K_1 = 1.875\ \mu$A/V^2, $K_2 = K_3 = 75\ \mu$A/V^2, $V_{Gi} = 1.5$ V and $V_T = 0.65$ V, which realizes $Q = 40$.

VI. Fully Differential Signal Processing

A. Fully Differential Amplifier

Certain applications require the use of fully differential signal processing to extend the dynamic range of the signal, cancel even harmonics, and suppress undesirable CM signals. A fully differential amplifier that is used as a basic cell to realize fully differential filters is shown in Fig. 14. It can be shown that the differential mode (DM) and CM output voltages are given by

$$V_{Od} = \frac{Z_2}{Z_1}(2V_{1d} + V_{2d}) \tag{39}$$

$$V_{Oc} = \frac{Z_2}{Z_1}V_{2c} \tag{40}$$

where

$$V_{id} = \frac{1}{2}(V_{i+} - V_{i-})$$
$$V_{ic} = \frac{1}{2}(V_{i+} + V_{i-}) \quad (i = 1, 2) \tag{41}$$

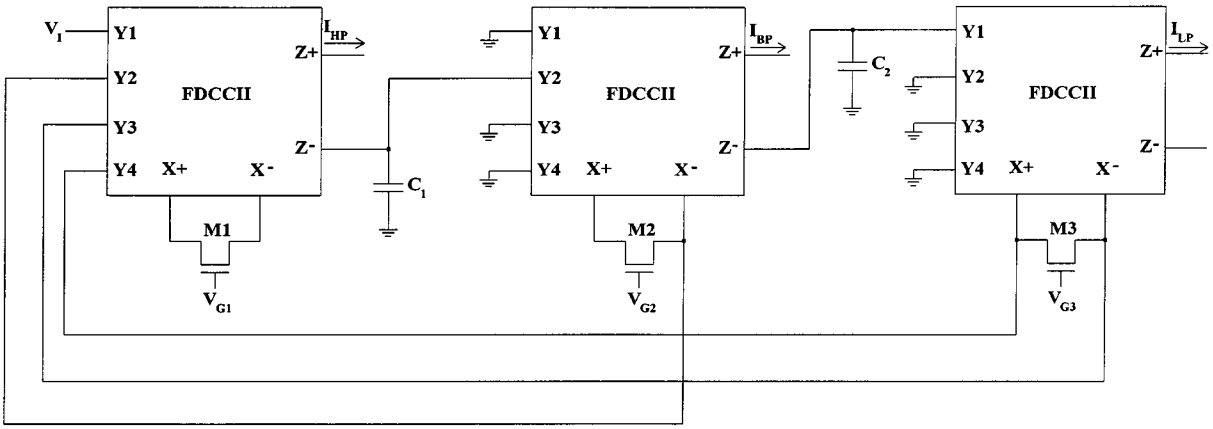

Fig. 11. A universal mixed-mode second-order filter (realization II).

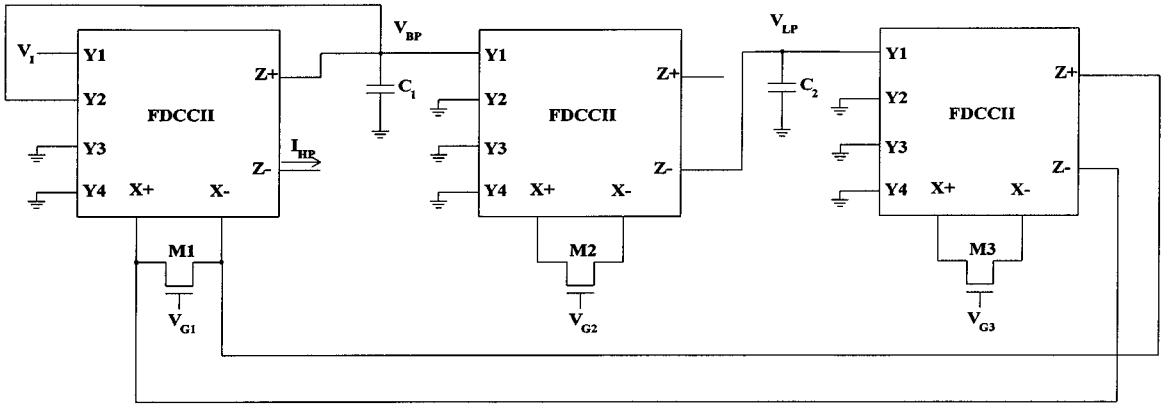

Fig. 12. A universal mixed-mode second-order filter (realization III).

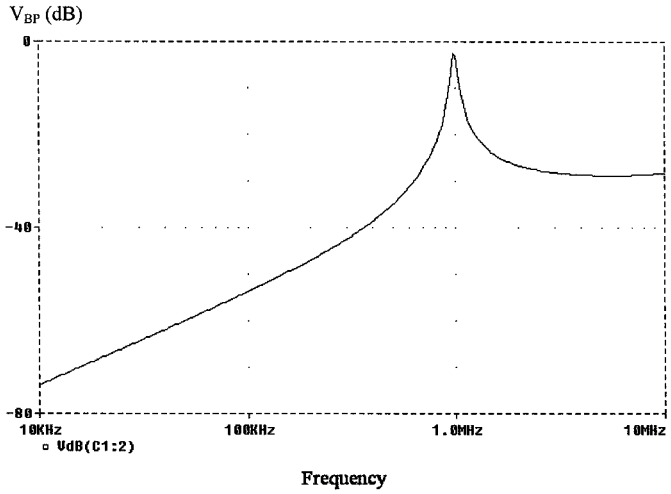

Fig. 13. Bandpass frequency response with $Q = 40$.

$$V_{Od} = \frac{1}{2}(V_{O+} - V_{O-})$$
$$V_{Oc} = \frac{1}{2}(V_{O+} + V_{O-}) \tag{42}$$

when a DM filter using the proposed FDCCII is realized, the DM and CM feedback loops must be studied to ensure the stability of both loops. It is clear from (41) and (42) that the amplifier has the same DM and CM gains for the input V_2. Hence, the characteristic equation of the filter will be the same for both DM and CM signals when Y_3 and Y_4 terminals are used. However, to suppress the CM input signals, external inputs should be applied to the Y_1 and Y_2 terminals where the CM gain is zero. In short, to implement a fully differential filter, Y_1 and Y_2 terminals are used for the external inputs while Y_3 and Y_4 terminals are used for the feedback signals.

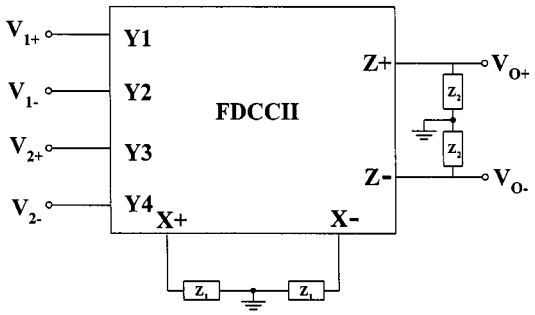

Fig. 14. The fully differential amplifier.

B. Fully Differential Filter

A fully differential filter based on the proposed FDCCII is shown in Fig. 15. No CM feedback loop is added to control the CM signals, as the filter loop is the CM feedback loop at the

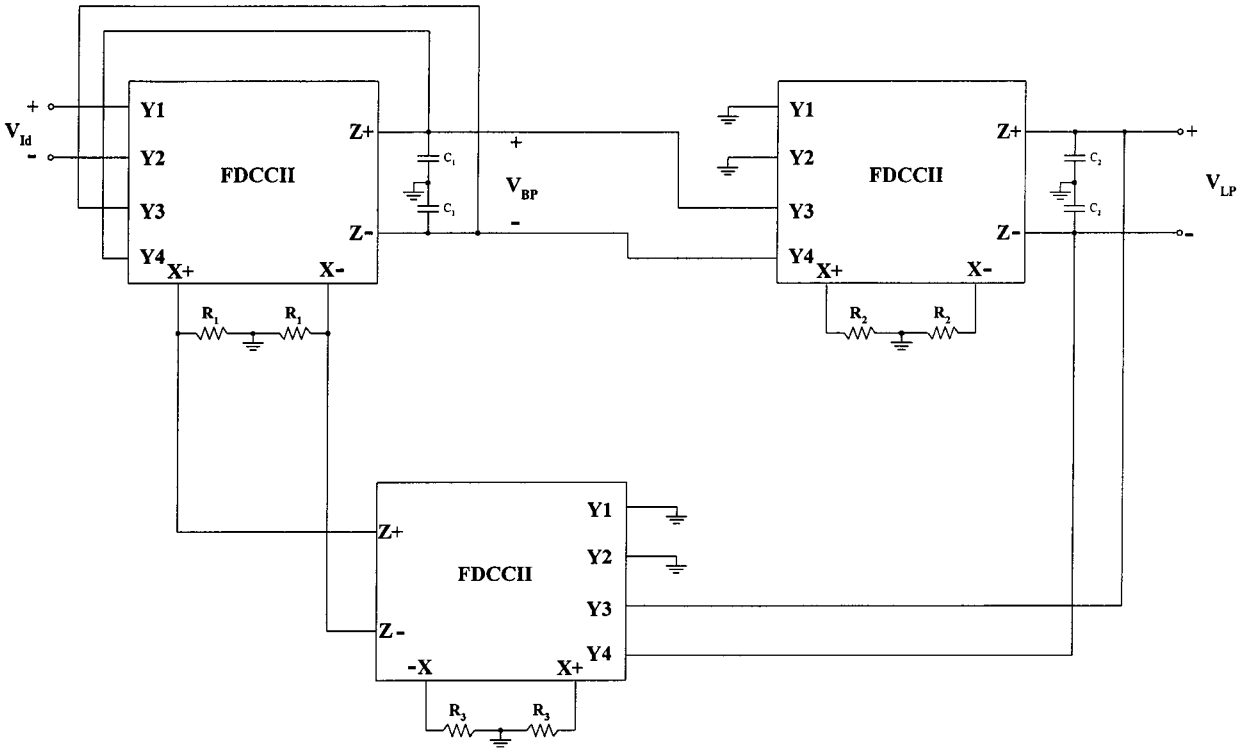

Fig. 15. A fully differential filter.

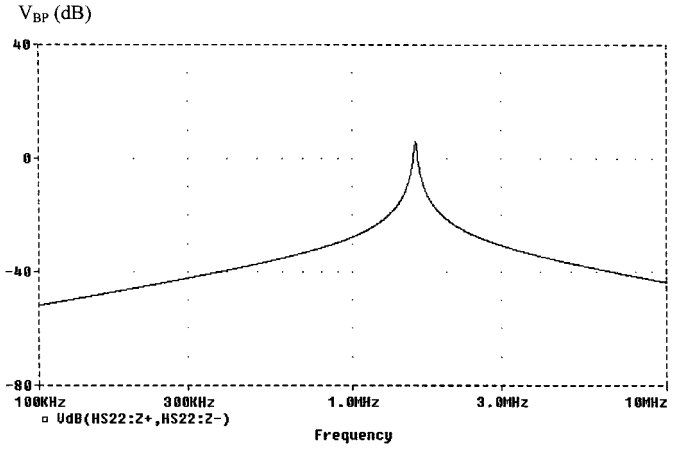

Fig. 16. Bandpass frequency response with $Q = 50$.

same time. The bandpass and low-pass frequency responses are given by

$$V_{\mathrm{BP}} = V_{Id}\frac{s\frac{2}{R_1C_1}}{D(s)} \tag{43}$$

$$V_{\mathrm{LP}} = V_{Id}\frac{\frac{2}{R_1R_2C_1C_2}}{D(s)} \tag{44}$$

where

$$D(s) = s^2 + \frac{1}{R_1C_1}s + \frac{1}{R_2R_3C_1C_2}. \tag{45}$$

The bandpass response of the proposed filter is shown in Fig. 16, with $R_1 = 250\ \mathrm{k}\Omega$, $R_2 = R_3 = 5\ \mathrm{k}\Omega$, and $C_1 = C_2 = 20$ pF. These values are selected to obtain a quality factor of 50 at a center frequency of 1.59 MHz.

VII. Conclusion

A novel fully differential second-generation current conveyor FDCCII is presented. Applications of the proposed block, such as a differential input balanced output transconductor, a four-quadrant multiplier, universal differential MOSFET-C second-order filters, and a fully differential RC second-order filter have been presented. The proposed block is also useful in mixed-mode applications where fully differential signal processing is required. The circuit has a bandwidth of about 10 MHz under heavy capacitive loads and can operate from supply voltages as low as ± 1.5 V.

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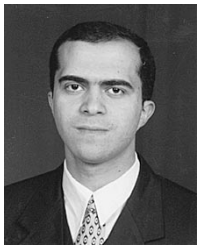

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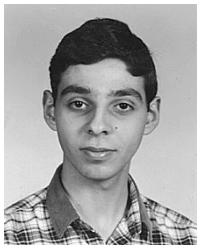
Dr. Soliman was decorated, in 1977, with the First Class Science Medal from the President of Egypt for his services to the field of Engineering and Engineering Education.



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