

NOVEL CMOS REALIZATIONS OF THE OPERATIONAL FLOATING CONVEYOR AND APPLICATIONS

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This paper presents novel CMOS realizations of the operational floating conveyor (OFC) based on novel block diagrams. It also introduces novel applications based on one of the proposed OFC realizations. The proposed OFC realization provides a wide bandwidth and a large gain bandwidth product. Hence, it exhibits wide bandwidth at higher gains. All the circuits in this paper are designed following a fair comparison criterion. The supply voltages are ± 1.5 V. The reference DC current source I_B is taken as $50 \mu\text{A}$. The CMOS model for all circuits is identical. The transistor model is $0.5 \mu\text{m}$ CMOS process provided by MOSIS (AGILENT).

Keywords: Low voltage; operational floating conveyor; analog circuits.

1. Introduction

The second generation current conveyor (CCII)^{1–3} and the current feedback op-amp (CFOA) are considered among the versatile building blocks in analog CMOS current-mode signal processing. The operational floating conveyor (OFC)⁴ is a new two-port general purpose analog building block. Its interesting aspect is that of providing the features of both the current conveyor and the current feedback op-amp. The symbol of the OFC is shown in Fig. 1.

It is a four-terminal building block that is defined by the following matrix equation:

$$\begin{bmatrix} V_x \\ I_y \\ V_w \\ I_z \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ Z_t & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} I_x \\ V_y \\ I_w \\ V_z \end{bmatrix}. \quad (1)$$

The input current at terminal X is multiplied by the open loop transimpedance gain Z_t to produce an output voltage at terminal W . The voltage at terminal X follows the voltage at terminal Y , so a voltage following action exists at its input



Fig. 1. Block diagram of the OFC.

port. The current at terminal W is conveyed to terminal Z , so a current following action exists at its output port.

Some of the high performance measures of the OFC are: wide input voltage and current ranges, high accuracy in voltage and current transfer (unity gain and zero offset), wide voltage and current transfer bandwidths, high open loop transimpedance gain (ideally infinite open loop transimpedance gain and correspondingly, zero input current at terminal X), large gain bandwidth product, low input impedance at terminals X and W , high output impedance at terminal Z as well as low power dissipation.

The OFC was first introduced by Toumazou, Payne, and Lidgey in 1991.⁴ Since then different realizations were introduced in the literature.⁵ These realizations provide large power dissipation and small bandwidth.^{4,5} The proposed OFC realizations presented in this paper provides smaller power dissipation and larger bandwidth compared to their previous OFC realizations. Moreover, the proposed OFC realizations follow simple block diagram architecture and hence it is easier to replace one block without much effect on the other blocks of the OFC realization. This will lead to easier improvement and this is the main advantage of the proposed OFC realizations introduced in this paper.

The OFC can be implemented using the realizations shown in Figs. 2–4. The first realization (Fig. 2)⁵ is implemented using two CCII⁺ blocks and one noninverting transimpedance amplifier. The first CCII⁺ is used to perform the required voltage following action at the input port between terminals Y and X . The second CCII⁺ is used to perform the required current following action at the output port between terminals W and Z . The input current at terminal X is multiplied by the transimpedance amplifier gain to provide the output voltage at terminal W . In the second realization (Fig. 3) proposed in this paper, the second CCII⁺ of the

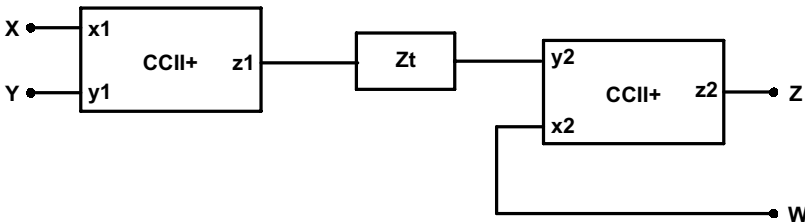


Fig. 2. The first block diagram realization of the OFC using two CCII⁺ blocks and one noninverting transimpedance amplifier.⁵

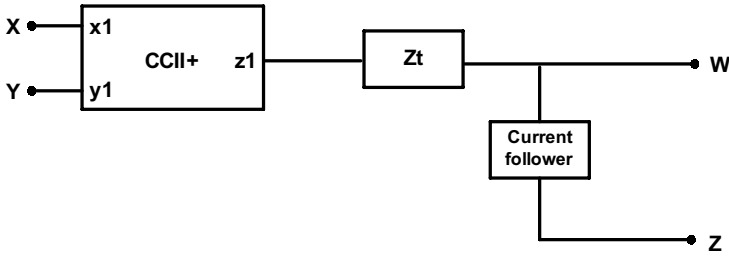


Fig. 3. The second block diagram realization of the OFC using one $CCII^+$ block, one noninverting transimpedance amplifier, and a positive current follower.

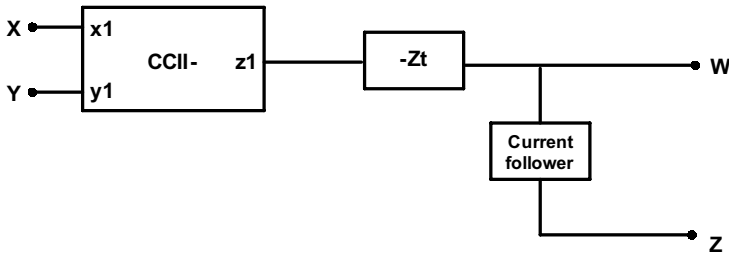


Fig. 4. The third block diagram realization of the OFC using one $CCII^-$ block, one inverting transimpedance amplifier, and a positive current follower.

first realization is replaced by a simple current follower to convey the terminal W current to terminal Z . In the third realization (Fig. 4) proposed in this paper, the first $CCII^+$ of the second realization is replaced by a $CCII^-$ and hence an inverting transimpedance amplifier is needed for proper operation.

It must be noted that the output voltage at terminal $W(V_w)$ equals to the sum of the voltage at the input terminal of the transimpedance amplifier and the input current at terminal $X(I_x)$ multiplied by the transimpedance amplifier gain (Z_t). Therefore, the input terminal of the transimpedance amplifier of all above realizations must be virtually grounded in order to produce an output voltage at terminal $W(V_w)$ equals to the input current at terminal $X(I_x)$ multiplied by the transimpedance amplifier gain (Z_t) to provide a proper realization of the OFC block.

In the second section of this paper, a novel CMOS OFC is proposed based on the first block diagram realization shown in Fig. 2 and using the $CCII^+$.⁶ The proposed circuit is examined and simulation results are given. In the third section of this paper, another novel CMOS OFC is proposed based on the second block diagram realization shown in Fig. 3 and using the $CCII^+$.⁶ In the fourth section of this paper, a novel CMOS OFC is proposed based on the third block diagram realization shown in Fig. 4 and using one floating current source (FCS)-based $CCII^-$. The main advantage of the proposed $CCII^-$ is that it is not implemented by using current mirrors. In the fifth section of this paper, different OFC applications

are proposed such as: voltage-controlled voltage source (VCVS), current-controlled current source (CCCS), transconductance amplifier, transresistance amplifier, positive second generation current conveyor, voltage-mode digitally controlled variable gain amplifier (VGA) and current-mode digitally controlled variable gain amplifier (VGA). These applications are examined and simulation results are given using the second proposed circuit, which gives the best results.

2. The First OFC Circuit Realization

2.1. Circuit description

The first CMOS realization of the OFC based on the block diagram shown in Fig. 2⁵ is shown in Fig. 5. The groups of the transistors ($M1$ and $M2$), ($M3$ and $M4$), ($M14$ and $M15$), ($M16$ and $M17$), ($M5$ and $M18$), ($M6$ and $M19$), ($M11$ and $M12$) as well as ($M7$ and $M20$) are matched. Assuming that all the transistors operate in the saturation region, the operation of the circuit can be explained as follows. The first CCII⁺ ($M1$ – $M7$)⁶ perform the voltage following action at the input port between terminals Y and X . The second CCII⁺ ($M14$ – $M20$)⁶ perform the current following action at the output port between terminals W and Z . The transimpedance amplifier ($M8$ – $M13$) multiply the input current at terminal X by a large transimpedance gain Z_t to produce the output voltage at terminal W . The transimpedance amplifier operation can be explained as follows. The input current at terminal X is mirrored by transistors $M3$, $M4$, $M6$ and $M7$, and the mirrored current will flow in the equivalent parasitic impedance of the gate terminal of $M8$, producing a voltage on it. This voltage is then amplified to produce the output voltage at terminal W .

Taking the finite value of the transistor transconductance g_m and drain to source conductance g_d into consideration and replacing each transistor by its small signal equivalent circuit, the small signal voltage transfer gain from the Y terminal to the X terminal is given approximately by:

$$A_v = \frac{v_x}{v_y} = \frac{g_{m1}}{g_{m1} + g_{d1} + \frac{g_{d3}(g_{d1} + 2g_{d5})}{(g_{d5} + g_{m3})}}. \quad (2)$$

The small signal input resistance seen at terminal X is given approximately by:

$$r_x = \frac{(g_{d1} + 2g_{d5})}{(g_{m1} + g_{d1})(g_{m3} + g_{d5}) + g_{d3}(g_{d1} + 2g_{d5})}. \quad (3)$$

The small signal open loop transimpedance gain Z_t is given approximately by:

$$Z_t = \frac{g_{m12}g_{m13}g_{m14}}{(g_{d4} + g_{d7})(g_{d12} + g_{d10})(g_{m11} + g_{d13}) \left(g_{m14} + g_{d14} + \frac{g_{d16}(g_{d14} + 2g_{d18})}{(g_{d18} + g_{m16})} \right)}. \quad (4)$$

The output resistance at terminal Z is given by:

$$r_z = \frac{1}{g_{d17} + g_{d20}}. \quad (5)$$

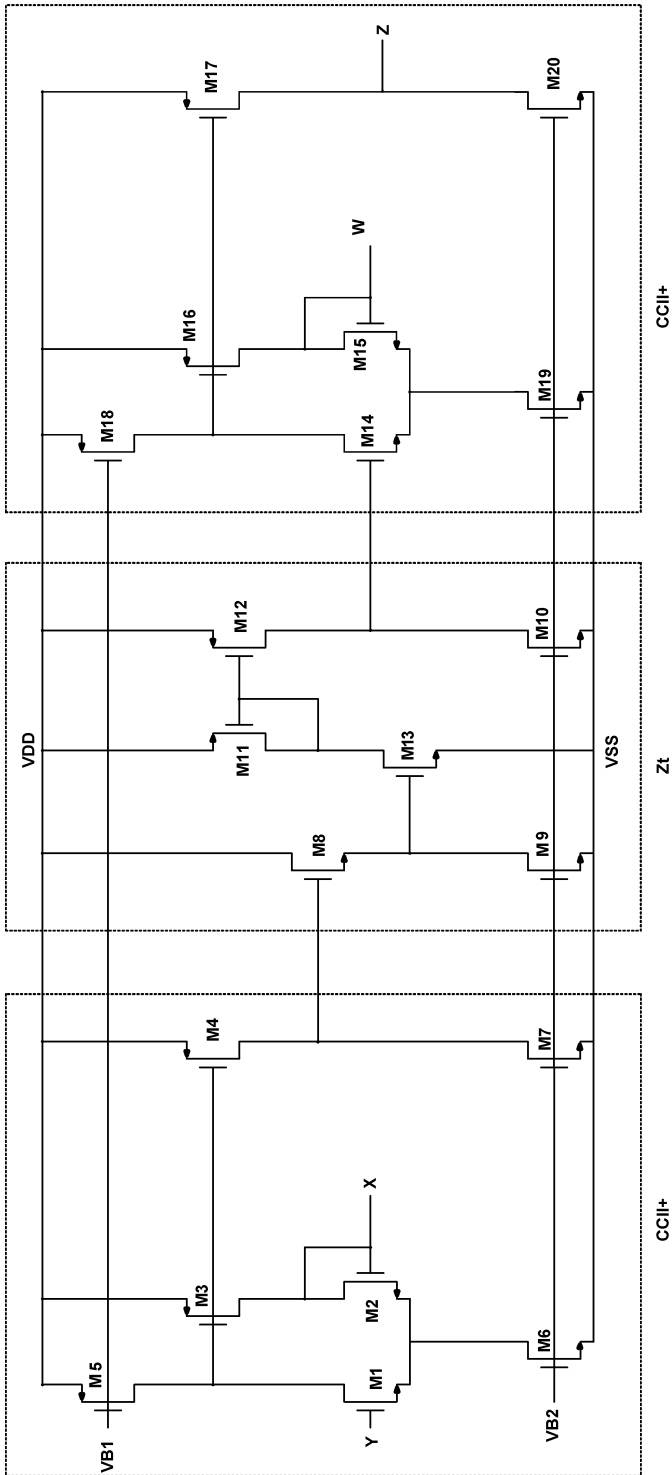


Fig. 5. The proposed OFC based on the realization shown in Fig. 2.

2.2. Simulation results

Transistors aspect ratios are reported in Table 1, the biasing current $2I_B = 100 \mu\text{A}$. Simulation results are tabulated in Table 4 and shown in Figs. 6–8. It must be noted that the scale used for the frequency axis for all simulations in the paper is in decade ($10^0 \text{ Hz} - 10^1 \text{ Hz} - 10^2 \text{ Hz} - 10^3 \text{ Hz} \dots$). These results can be described as follows. The input voltage range is from -0.4 V to 1.2 V . The average value of the open circuit voltage transfer gain equals 0.99887. The open loop gain of the voltage section equals 59 dB. The open circuit voltage transfer bandwidth exhibits a 3-dB frequency of 826 MHz (Fig. 6). The input resistance at terminal X at DC equals 30.2Ω (Fig. 8). The total harmonic distortion (THD) of an input sinusoid of frequency 100 KHz and amplitude 0.5 V peak to peak is 0.038%. The power dissipation of the circuit equals

Table 1. Transistors aspect ratios of the circuit shown in Fig. 5.

Transistor	$W (\mu\text{m})/L (\mu\text{m})$
$M1, M2, M14, M15$	50/1
$M3, M4, M11, M12, M16, M17$	50/2.5
$M5, M7, M10, M18, M20$	20/2.5
$M6, M8, M19$	40/2.5
$M9, M13$	100/2.5

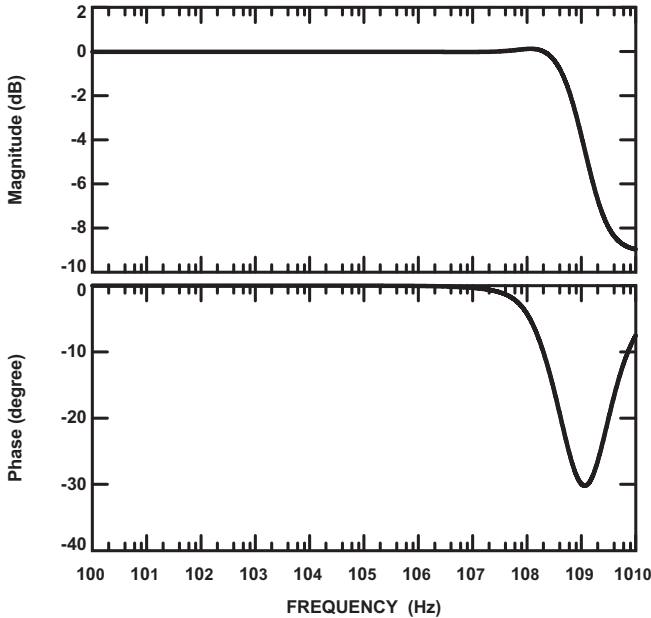


Fig. 6. Frequency characteristics of the open circuit voltage transfer gain between Y and X (V_X/V_Y) for the circuit shown in Fig. 5.

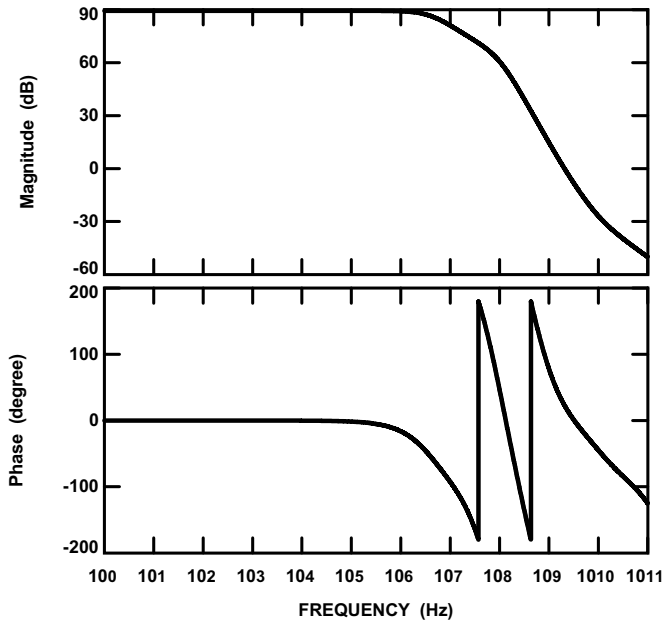


Fig. 7. Frequency characteristics of the open loop transimpedance gain between X and W (V_W/I_X) for the circuit shown in Fig. 5.

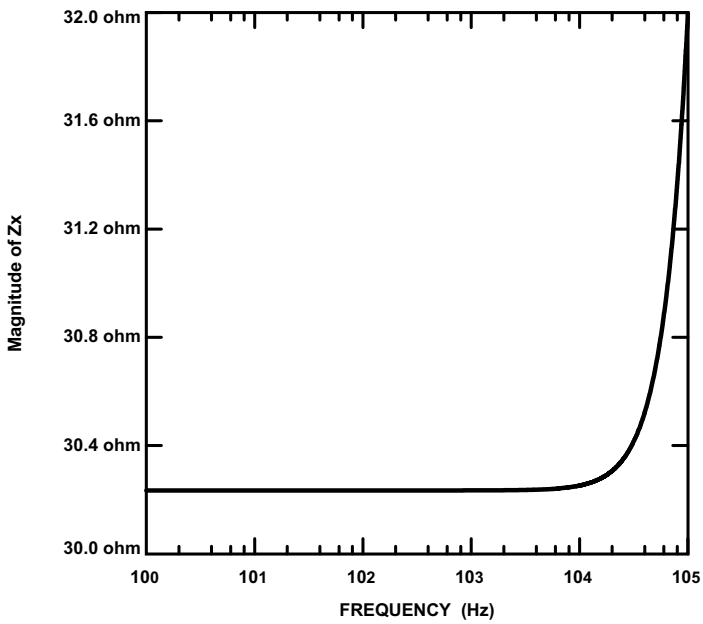


Fig. 8. Input impedance at terminal X for the circuit shown in Fig. 5.

2.4 mW. The DC open loop transimpedance gain equals 89.42 dB (= 29.58 K Ω) (Fig. 7). The gain bandwidth product equals 2070 MHz Ω .

3. The Second OFC Circuit Realization

3.1. Circuit description

The second CMOS realization of the OFC based on the block diagram shown in Fig. 3 is shown in Fig. 9. The groups of the transistors ($M1$ and $M2$), ($M3$ and $M4$), ($M10$ and $M15$) as well as ($M11$, $M12$ and $M14$) are matched. Assuming that all the transistors operate in the saturation region, the operation of the circuit can be explained as follows. The first CCII⁺ ($M1$ – $M7$)⁶ perform the voltage following action at the input port between terminals Y and X . The positive current follower ($M10$, $M12$, $M14$ and $M15$) performs the current following action at the output port between terminals W and Z . The transimpedance amplifier ($M8$ – $M13$) multiply the input current at terminal X by a large transimpedance gain Z_t to produce the output voltage at terminal W . The transimpedance amplifier operation can be explained as follows. The input current at terminal X is mirrored by transistors $M3$, $M4$, $M6$ and $M7$, and the mirrored current will flow in the equivalent parasitic impedance of the gate terminal of $M8$, producing a voltage on it. This voltage is then amplified to produce the output voltage at terminal W .

Taking the finite value of the transistor transconductance g_m and drain to source conductance g_d into consideration and replacing each transistor by its small signal equivalent circuit, the small signal voltage transfer gain from the Y terminal to the X terminal is given approximately by:

$$A_v = \frac{v_x}{v_y} = \frac{g_{m1}}{g_{m1} + g_{d1} + \frac{g_{d3}(g_{d1} + 2g_{d5})}{(g_{d5} + g_{m3})}}. \quad (6)$$

The small signal input resistance seen at terminal X is given approximately by:

$$r_x = \frac{(g_{d1} + 2g_{d5})}{(g_{m1} + g_{d1})(g_{m3} + g_{d5}) + g_{d3}(g_{d1} + 2g_{d5})}. \quad (7)$$

The small signal open loop transimpedance gain Z_t is given approximately by:

$$Z_t = \frac{g_{m12}g_{m13}}{(g_{d4} + g_{d7})(g_{d12} + g_{d10})(g_{m11} + g_{d13})}. \quad (8)$$

The output resistance at terminal Z is given by:

$$r_z = \frac{1}{g_{d14} + g_{d15}}. \quad (9)$$

3.2. Simulation results

Transistors aspect ratios are reported in Table 2. The biasing current $2I_B = 100 \mu\text{A}$. Simulation results are tabulated in Table 4 and shown in Figs. 10–12. These results

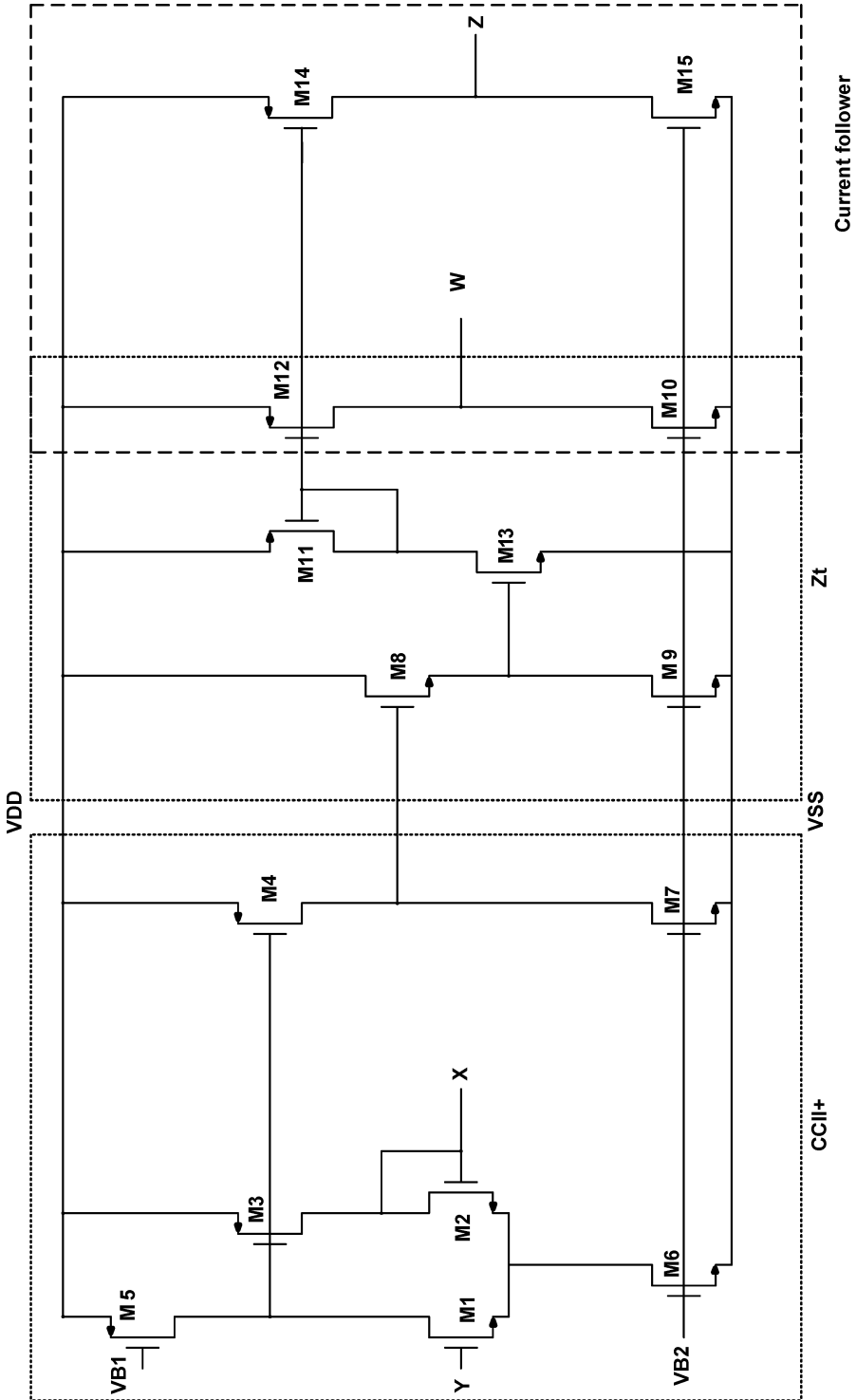


Fig. 9. The proposed OFC based on the realization shown in Fig. 3.

Table 2. Transistors aspect ratios of the circuit shown in Fig. 9.

Transistor	$W (\mu\text{m})/L (\mu\text{m})$
$M1, M2$	50/1
$M3, M4, M11, M12, M14$	50/2.5
$M5, M7, M10, M15$	20/2.5
$M6, M8$	40/2.5
$M9, M13$	100/2.5

can be described as follows. The input voltage range is from -0.4 V to 1.2 V . The average value of the open circuit voltage transfer gain equals 0.99887 . The open loop gain of the voltage section equals 59 dB . The open circuit voltage transfer bandwidth exhibits a 3-dB frequency of 826 MHz (Fig. 10). The input resistance at terminal X at DC equals $30.2\ \Omega$ (Fig. 12). The total harmonic distortion (THD) of an input sinusoid of frequency 100 KHz and amplitude 0.5 V peak to peak is 0.038% . The power dissipation of the circuit equals 2.1 mW . The DC open loop transimpedance gain equals 103.287 dB ($= 146\text{ K}\Omega$) (Fig. 11). The gain bandwidth product equals $3615\text{ MHz}\ \Omega$.

The advantage of this second proposed OFC realization circuit shown in Fig. 9 is proved by the following comparison. From Table 4, it is clear that the second proposed OFC provides more DC open loop transimpedance gain and more gain

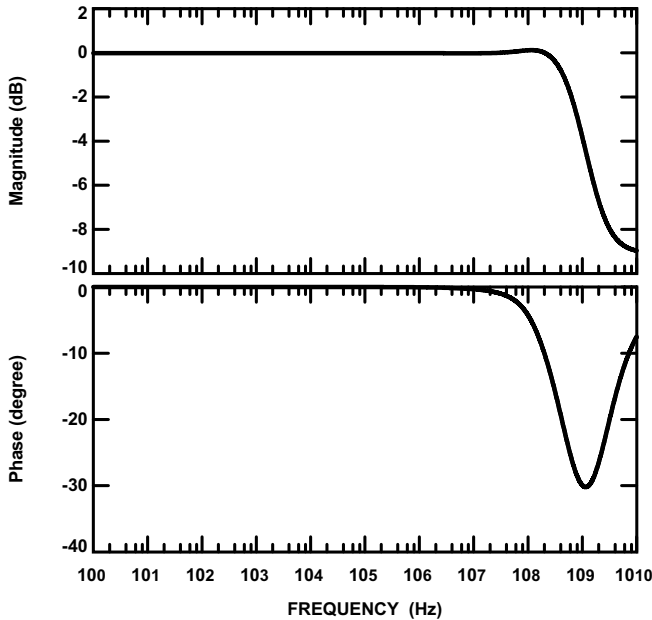


Fig. 10. Frequency characteristics of the open circuit voltage transfer gain between Y and X (V_X/V_Y) for the circuit shown in Fig. 9.

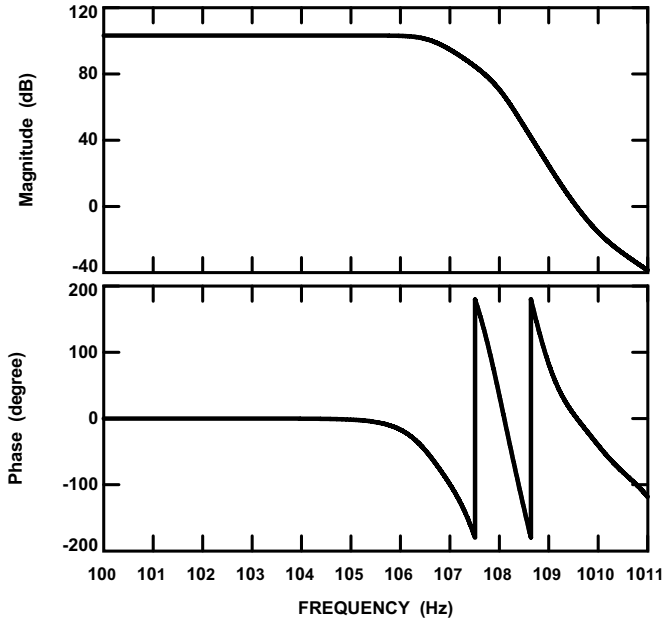


Fig. 11. Frequency characteristics of the open loop transimpedance gain between X and W (V_W/I_X) for the circuit shown in Fig. 9.

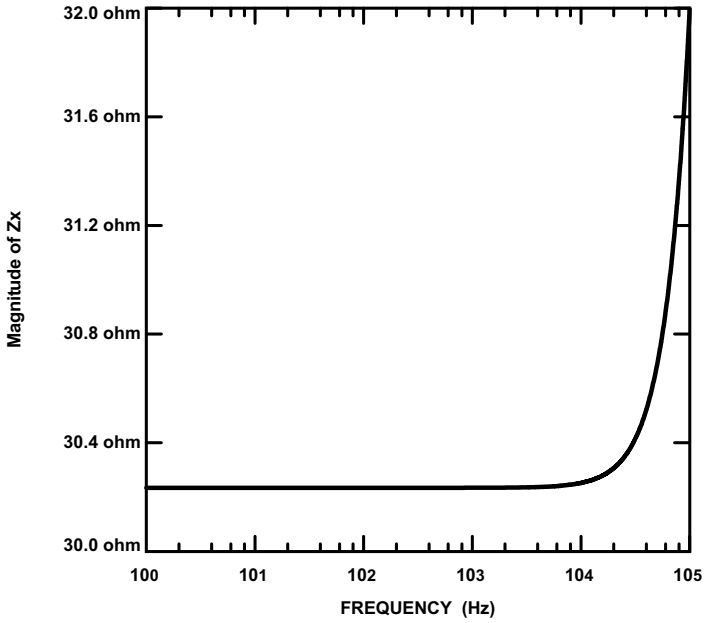


Fig. 12. Input impedance at terminal X for the circuit shown in Fig. 9.

bandwidth product. Moreover, it dissipates less power, keeping all the other parameters the same. The DC open loop transimpedance gain increased from 89.42 dB to 103.287 dB. The gain bandwidth product also increased from 2070 MHz Ω to 3615 MHz Ω .

It is important to note that the second CCII⁺ of the first proposed OFC realization shown in Fig. 5 performs unwanted voltage following action. It is needed only to perform current following action at the output port between terminals *W* and *Z*. Hence, this second CCII⁺ is removed in the second OFC realization shown in Fig. 9. This removal results in less power dissipation and more transimpedance amplifier gain as proved from the simulation (Table 4).

4. The Third OFC Circuit Realization

4.1. Circuit description

The third CMOS realization of the OFC based on the block diagram shown in Fig. 4 is shown in Fig. 13. The groups of the transistors (*M1–M8*), (*M10* and *M11*) as well as (*M12* and *M13*) are matched. Assuming that all the transistors operate in the saturation region, the operation of the circuit can be explained as follows. The first CCII⁻ (*M1–M8*) performs the voltage following action at the input port between terminals *Y* and *X*. It consists of two floating current source (FCS) blocks.⁷ The first FCS (*M1–M4*) produces two output-balanced currents I_{o1} and I_{o2} which are given by⁸ Eq. (10) where $v_d = V_x - V_y$. These two currents are forced to be zero by applying them to the input stage of the second FCS block and correspondingly, from Eq. (10), the differential voltage $v_d = 0$. Hence, the voltage at terminal *X* will follow the voltage at terminal *Y*. The second FCS is responsible for conveying the *X* terminal current to the *Z* terminal. The positive current follower (*M10–M13*) performs the current following action at the output port between terminals *W* and *Z*. The transimpedance amplifier (*M9* and *M14*) multiply the input current at terminal *X* by a large inverting transimpedance gain Z_t to produce the output voltage at terminal *W*. The use of an inverting transimpedance amplifier is essential since the conveyed current at the gate terminal of *M14* will be an inverted replica of the input current at terminal *X*. Hence, the inverting transimpedance amplifier is essential to provide an output voltage at terminal *W* directly proportional to the input current at terminal *X*. The transimpedance amplifier operation can be explained as follows. The input current at terminal *X* is conveyed by the CCII⁻ to the gate terminal of *M14*. This current will flow in the equivalent parasitic impedance of this gate terminal producing a voltage on it. This voltage is then amplified to produce the output voltage at terminal *W*:

$$I_{o1} = -I_{o2} = -\frac{1}{2}v_d \left(\sqrt{K_n} \sqrt{2I_B - \frac{K_n v_d^2}{4}} + \sqrt{K_P} \sqrt{2I_B - \frac{K_P v_d^2}{4}} \right), \quad (10)$$

where $K_n = \mu_n C_{OX} \frac{W_1}{L_1}$ and $K_p = \mu_p C_{OX} \frac{W_3}{L_3}$.

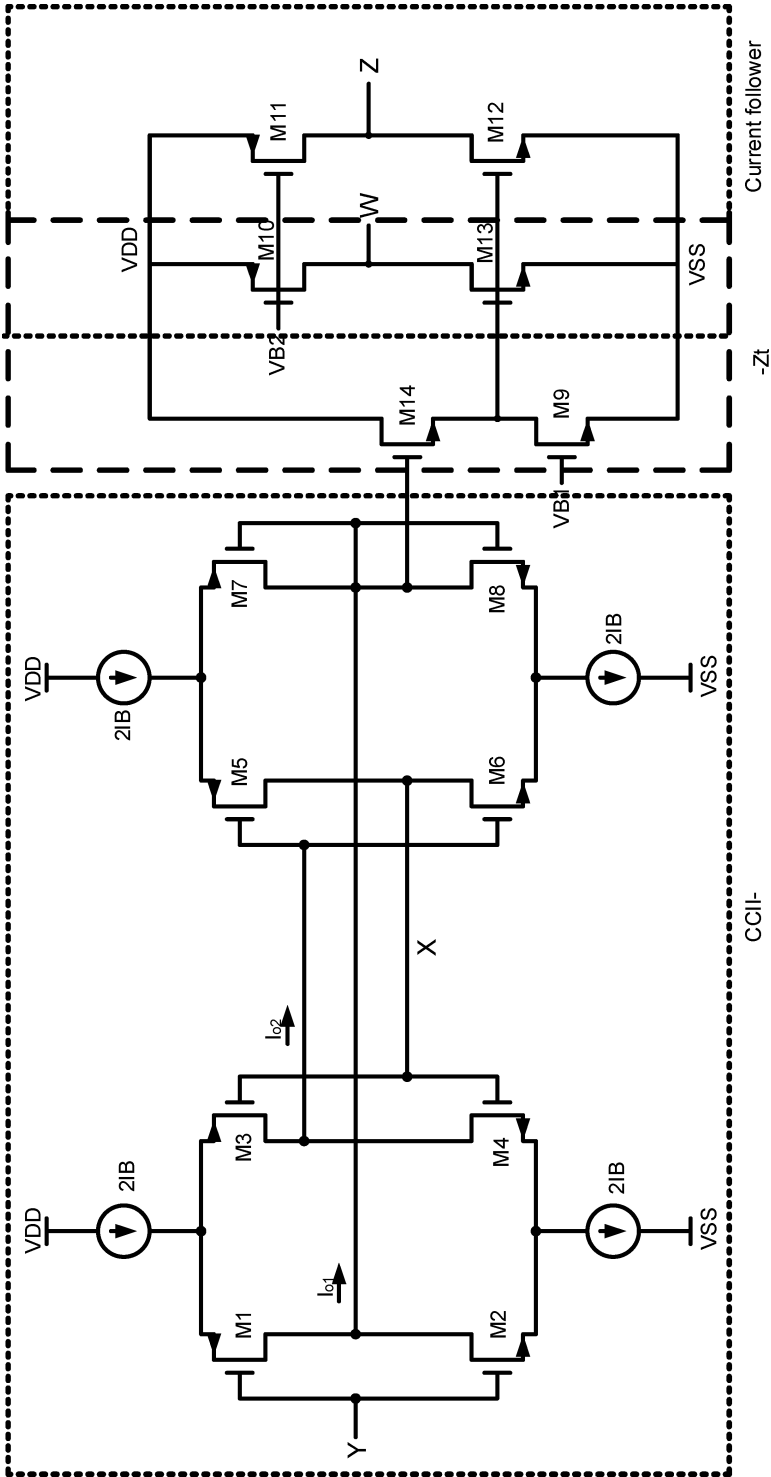


Fig. 13. The proposed OFC based on the realization shown in Fig. 4.

Taking the finite value of the transistor transconductance g_m and drain to source conductance g_d into consideration and replacing each transistor by its small signal equivalent circuit, the small signal voltage transfer gain from the Y terminal to the X terminal is given approximately by:

$$A_v = \frac{v_x}{v_y} = \frac{1}{1 + \frac{(g_{d3} + g_{d4})(g_{d5} + g_{d6})}{(g_{m1} + g_{m2})(g_{m5} + g_{m6})}}. \quad (11)$$

The small signal input resistance seen at terminal X is given approximately by:

$$r_x = \frac{(g_{d3} + g_{d4})}{(g_{m1} + g_{m2})(g_{m5} + g_{m6})}. \quad (12)$$

The small signal open loop transimpedance gain Z_t is given approximately by:

$$Z_t = \frac{g_{m13}}{(g_{d1} + g_{d2} + g_{d7} + g_{d8})(g_{d13} + g_{d10})} \frac{1 + \frac{(g_{o1} + g_{o2})}{2(g_{m9} + g_{m10})}}{1 - \frac{(g_{o1} + g_{o2})}{2(g_{m9} + g_{m10})}}, \quad (13)$$

where g_{o1} and g_{o2} are the effect of nonideal current sources in the circuit which can be represented by CMOS transistors and they are equal to the drain to source conductances of the biasing transistors.

The output resistance at terminal Z is given by:

$$r_z = \frac{1}{g_{d11} + g_{d12}}. \quad (14)$$

4.2. Simulation results

Transistors aspect ratios are reported in Table 3. The biasing current $2I_B = 100 \mu\text{A}$. Simulation results are tabulated in Table 4 and shown in Figs. 14–16. These results can be described as follows. The input voltage range is from -0.6 V to 0.5 . The average value of the open circuit voltage transfer gain equals 1.00007 . The open loop gain of the voltage section equals 83 dB . The open circuit voltage transfer bandwidth exhibits a 3-dB frequency of 695 MHz (Fig. 14). The input resistance at terminal X at DC equals 12.8Ω (Fig. 16). The total harmonic distortion (THD) of an input sinusoid of frequency 100 KHz and amplitude 0.5 V peak to peak is 0.005% . The power dissipation of the circuit equals 1.2 mW . The DC open loop transimpedance gain equals 226.78 dB ($= 218300 \text{ M}\Omega$) (Fig. 15). The gain bandwidth product equals $7943 \text{ MHz}\Omega$.

The advantage of this third proposed OFC realization circuit shown in Fig. 13 is proved by the following comparison. From Table 4, it is clear that the third proposed OFC provides more accurate voltage following action. Also, it dissipates less power and achieves less input resistance at the X terminal. Moreover, it provides more DC open loop transimpedance gain as well as more gain bandwidth product. The DC open loop transimpedance gain increased to 226.78 dB . The gain bandwidth product also is increased to $7943 \text{ MHz}\Omega$. The third proposed OFC realization exhibits less

Table 3. Transistors aspect ratios of the circuit shown in Fig. 13.

Transistor	$W (\mu\text{m})/L (\mu\text{m})$
$M1-M8$	50/1
$M9-M13$	50/2.5
$M14$	100/0.5

Table 4. Parameters of the circuits shown in Figs. 5, 9 and 13.

Parameter	The OFC realization based on the block diagram shown in Fig. 2 ⁵	The OFC realization based on the block diagram shown in Fig. 3	The OFC realization based on the block diagram shown in Fig. 4	Unit
Input voltage dynamic range	-0.4 to 1.2	-0.4 to 1.2	-0.6 to 0.5	V
A_v (average value) of open circuit voltage transfer gain	0.99887	0.99887	1.00007	V/V
Open loop gain (voltage section)	59	59	83	dB
3-dB bandwidth of open circuit voltage transfer gain	826	826	695	MHz
r_x	30.2	30.2	12.8	Ω
THD for a sinusoid of 100 KHz	0.038%	0.038%	0.005%	—
Power dissipation	2.4	2.1	1.2	mW
DC open loop transimpedance gain	89.42	103.287	226.78	dB
Gain bandwidth product	2070	3615	7943	MHz Ω

open circuit voltage transfer bandwidth than the other proposed architecture and that is the price paid for the low power dissipation.

The strength of the third proposed OFC realization using CCII⁻ shown in Fig. 13 is that it exhibits only one peak at its transimpedance frequency phase response (Fig. 15). However, the first and second proposed OFC realizations provide more peaks at their transimpedance frequency phase responses (Figs. 7 and 11). These peaks can be reduced to only one peak by compensation methods which are not used in this paper to introduce a fair comparison between the three OFC realizations. This compensation may be done by adding two compensation capacitors $C_1 = 5 \text{ pF}$ (connected between the terminal X and the terminal W) and $C_2 = 5 \text{ pF}$ (connected between terminal X and the ground). Moreover, the FCS-based CCII⁻ realization has no current mirrors. Hence, it does not suffer from frequency limitations or transistor mirrors mismatch.

5. Applications Based on OFC

The OFC is designed to be used in a closed loop implementation with current feedback from terminal W to terminal X . Since both input and output ports are floating, the OFC is an extremely versatile analog device. Different applications can be accurately configured in a closed loop implementation such as: noninverting

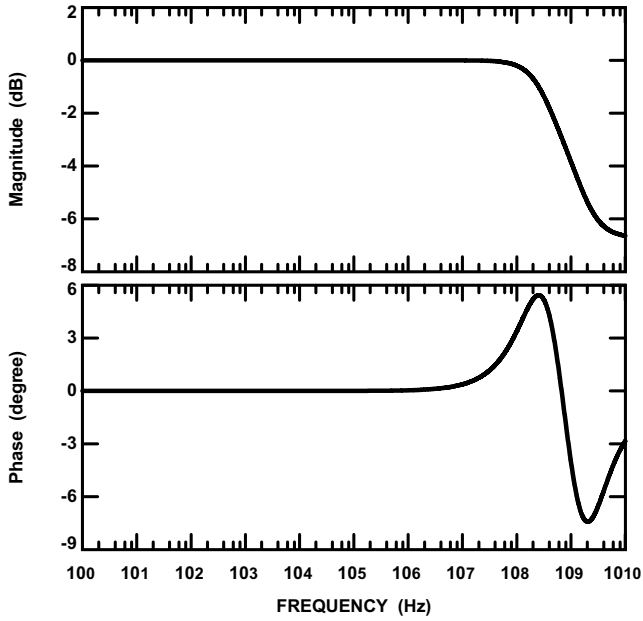


Fig. 14. Frequency characteristics of the open circuit voltage transfer gain between Y and X (V_X/V_Y) for the circuit shown in Fig. 13.

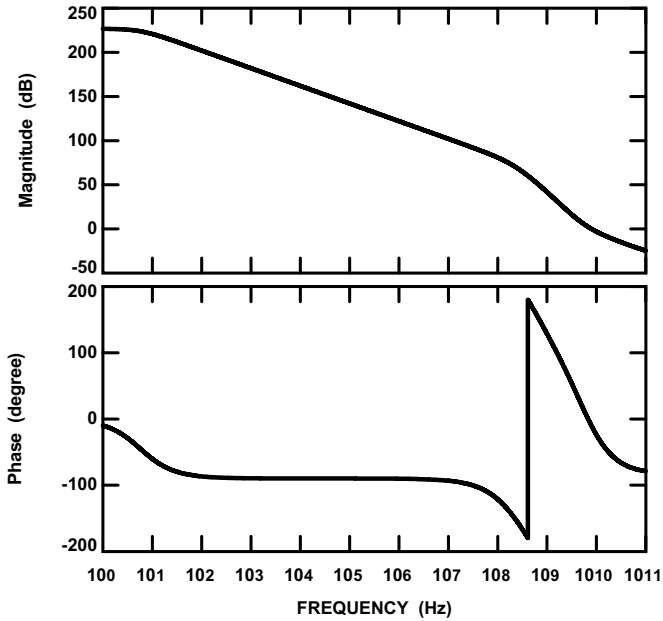


Fig. 15. Frequency characteristics of the open loop transimpedance gain between X and W (V_W/I_X) for the circuit shown in Fig. 13.

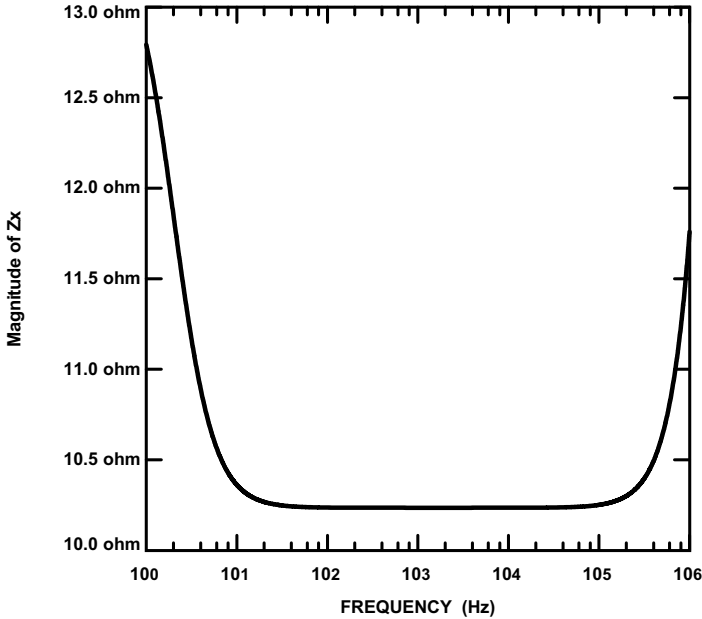


Fig. 16. Input impedance at terminal X for the circuit shown in Fig. 13.

voltage amplifier, inverting current amplifier, transresistance amplifier, transconductance amplifier, positive second generation current conveyor (CCII⁺), voltage-mode digitally controlled variable gain amplifier (VGA) and current-mode digitally controlled variable gain amplifier (VGA).

It worth noting that there are other blocks perform the same applications mentioned above such as the operational floating current conveyor (OFCC).⁹ It has the same transmission properties as the OFC but with an additional current output terminal. This additional terminal output current is a negative replica of the output current at terminal Z. The proposed OFC realizations introduced in this paper can be extended to realize the OFCC by adding one extra floating current source (FCS) at its output stage. The main advantage of the OFC over the OFCC is that the OFC is a four-terminal building block. However, the OFCC is a five-terminal block. Moreover, the OFC can be used to realize the same applications as the OFCC. One advantage of the OFCC block is that the CCII⁻ can be realized using only one OFCC block. However, two OFC-based CCII⁺ blocks are needed to realize the CCII⁻.

5.1. Noninverting voltage amplifier (VCVS)

The noninverting voltage amplifier (voltage-controlled voltage source) configuration is shown in Fig. 17.⁴ The voltage gain can be obtained as follows:

$$\text{Voltage gain } (A_v) = \frac{V_o}{V_i} = 1 + \frac{R_2}{R_1}. \tag{15}$$

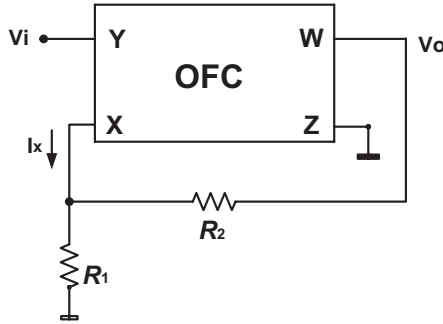


Fig. 17. The noninverting voltage amplifier configuration using the OFC.

Taking the effect of the finite transimpedance gain, Z_t , and using the finite transimpedance single pole model. The single pole model transimpedance gain is given by:

$$Z_t(s) = \frac{Z_{to}}{1 + \frac{s}{\omega_o}}, \tag{16}$$

where Z_{to} is the DC open loop transimpedance gain and ω_o is the transimpedance cut off frequency.

For high frequency applications, the transimpedance gain, $Z_t(s)$, may be expressed as:

$$Z_t(s) = \frac{1}{sC_p}, \tag{17a}$$

where

$$C_p = \frac{1}{Z_{to}\omega_o}. \tag{17b}$$

Applying KCL at terminal X, the node equation may be given by:

$$I_x + \frac{V_o - V_i}{R_2} = \frac{V_i}{R_1}. \tag{18a}$$

Substituting by $I_x = V_o/Z_t$ in Eq. (18a), the noninverting voltage amplifier gain may be given by:

$$\text{Voltage gain } (A_v) = \frac{V_o}{V_i} = \left(1 + \frac{R_2}{R_1}\right) \frac{1}{1 + \frac{R_2}{Z_t(s)}} = \left(1 + \frac{R_2}{R_1}\right) \varepsilon(s), \tag{18b}$$

where $\varepsilon(s)$ is the error function and can be expressed as:

$$\varepsilon(s) = \frac{1}{1 + \frac{R_2}{Z_t(s)}}. \tag{19}$$

By substituting from Eq. (17a) into Eq. (19), the error function reduces to

$$\varepsilon(s) = \frac{1}{1 + sR_2C_p}. \tag{20}$$

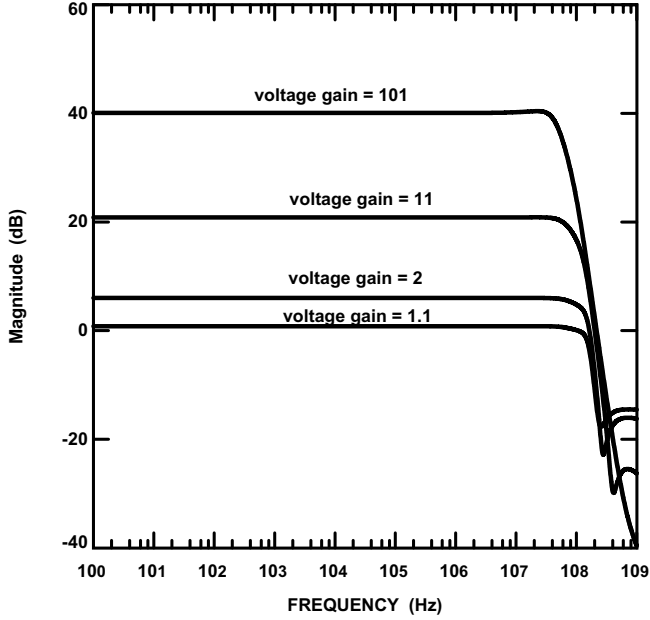


Fig. 18. Frequency characteristics of the voltage gain of the noninverting voltage amplifier configuration shown in Fig. 17.

Hence, for high frequency applications, compensation methods must be employed in order to account for the error function given by Eq. (20).

The noninverting voltage amplifier is simulated using $R_1 = 1\text{ k}\Omega$ and $R_2 = 0.1\text{ k}\Omega, 1\text{ k}\Omega, 10\text{ k}\Omega$ and $100\text{ k}\Omega$. The circuit is compensated by using a capacitor $C = 0.5\text{ pF}$ (connected between the output terminal W and the input terminal Y). The different gains of the differential voltage amplifier are shown in Fig. 18.

5.2. Inverting current amplifier (CCCS)

The inverting current amplifier (current-controlled current source) configuration is shown in Fig. 19.⁴ The current gain can be obtained as follows:

$$\text{Current gain } (A_i) = \frac{I_o}{I_i} = \frac{I_w}{I_i} = - \left(1 + \frac{R_2}{R_1} \right). \tag{21}$$

Taking the effect of the finite transimpedance gain, Z_t , and using the finite transimpedance single pole model (Sec. 5.1), the current gain can be expressed as:

$$\text{Current gain } (A_i) = \frac{I_o}{I_i} = \frac{I_w}{I_i} = - \left(1 + \frac{R_2}{R_1} \right) \varepsilon(s), \tag{22}$$

where $\varepsilon(s)$ is given by Eq. (20). Hence, for high frequency applications, compensation methods must be employed in order to account for the error function given by Eq. (20).

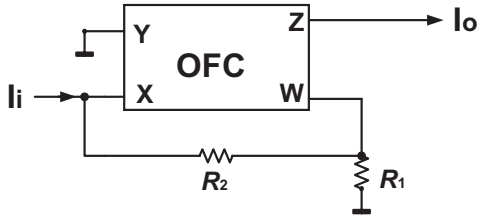


Fig. 19. The inverting current amplifier configuration using the OFC.

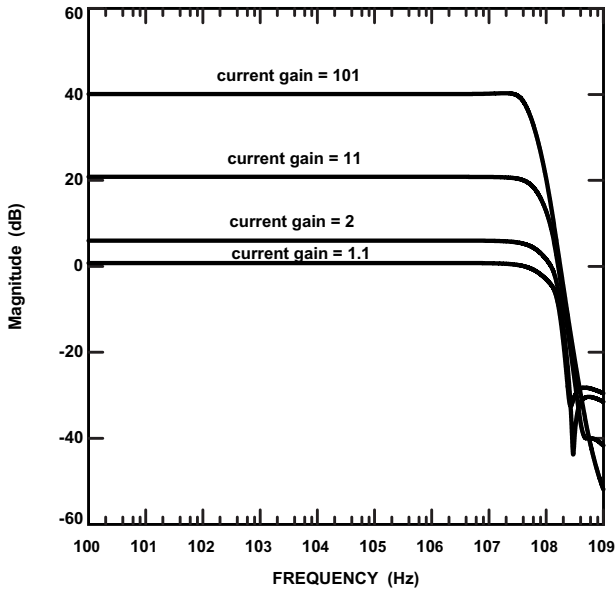


Fig. 20. Frequency characteristics of the current gain for the current amplifier configuration shown in Fig. 19.

The inverting current amplifier is simulated using $R_1 = 1\text{ k}\Omega$ and $R_2 = 0.1\text{ k}\Omega$, $1\text{ k}\Omega$, $10\text{ k}\Omega$ and $100\text{ k}\Omega$. The circuit is compensated by using a capacitor $C = 0.5\text{ pF}$ (connected between the output terminal W and the input terminal Y). The different gains of the current amplifier are shown in Fig. 20.

5.3. Transconductance amplifier

The transconductance amplifier configuration is shown in Fig. 21.⁴ The transconductance gain can be obtained as follows:

$$\text{Transconductance gain} = \frac{I_o}{V_i} = \frac{I_w}{V_i} = \frac{1}{R}. \tag{23}$$

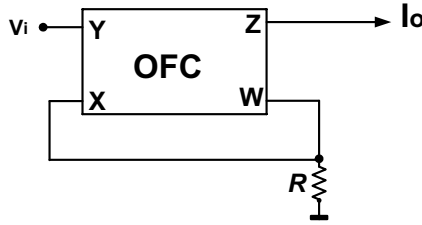


Fig. 21. The transconductance amplifier configuration using the OFC.

Taking the effect of the finite transimpedance gain, Z_t , and using the finite transimpedance single pole model, the transconductance gain can be expressed as:

$$\text{Transconductance gain} = \frac{I_o}{V_i} = \frac{I_w}{V_i} = \frac{1}{R}\varepsilon(s), \tag{24}$$

where $\varepsilon(s)$ is the error function and it is given by:

$$\varepsilon(s) = \frac{1}{1 + sRC_p}. \tag{25}$$

Hence, for high frequency applications, compensation methods must be employed in order to account for the error function given by Eq. (25).

The transconductance amplifier is simulated using $R = 1\ \Omega, 10\ \Omega, 0.1\ \text{k}\Omega, 1\ \text{k}\Omega$ and $10\ \text{k}\Omega$. The circuit is compensated by using a capacitor $C = 0.5\ \text{pF}$ (connected between the output terminal W and the input terminal Y). The different gains of the transconductance amplifier are shown in Fig. 22.

5.4. Transresistance amplifier

The transresistance amplifier configuration is shown in Fig. 23.⁴ The transresistance gain can be obtained as follows:

$$\text{Transresistance gain} = \frac{V_o}{I_i} = -R. \tag{26}$$

Taking the effect of the finite transimpedance gain, Z_t , and using the finite transimpedance single pole model, the transresistance gain can be expressed as:

$$\text{Transresistance gain} = \frac{V_o}{I_i} = -R\varepsilon(s), \tag{27}$$

where $\varepsilon(s)$ is the error function and it is given by Eq. (25). Hence, for high frequency applications, compensation methods must be employed in order to account for the error function given by Eq. (25).

The transresistance amplifier is simulated using $R = 1\ \Omega, 10\ \Omega, 0.1\ \text{k}\Omega, 1\ \text{k}\Omega, 10\ \text{k}\Omega$ and $100\ \text{k}\Omega$. The circuit is compensated by using a capacitor $C = 0.5\ \text{pF}$ (connected between the output terminal W and the input terminal Y). The different gains of the transresistance amplifier are shown in Fig. 24.

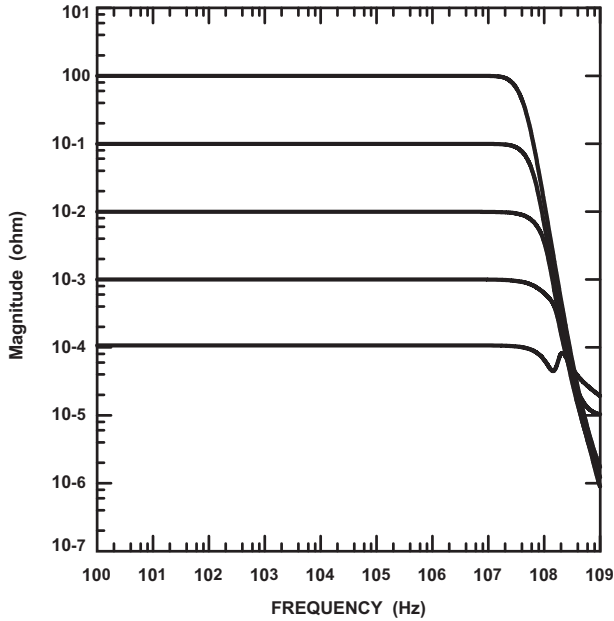


Fig. 22. Frequency characteristics of the transconductance gain of the transconductance amplifier configuration shown in Fig. 21.

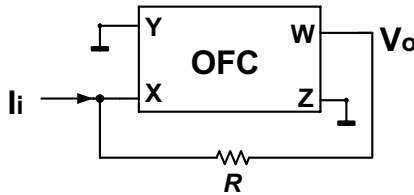


Fig. 23. The transresistance amplifier configuration using the OFC.

5.5. CCII⁺

The CCII⁺ configuration is shown in Fig. 25.⁴ It can be shown that the following configuration realizes a CCII⁺.

It can be shown that the short circuit current transfer ratio between terminals X and Z (I_z/I_x) can be given by:

$$\frac{I_z}{I_x} = \varepsilon(s), \tag{28}$$

where $\varepsilon(s)$ is the error function and it is given by Eq. (25). Hence, for high frequency applications, compensation methods must be employed in order to account for the error function given by Eq. (25).

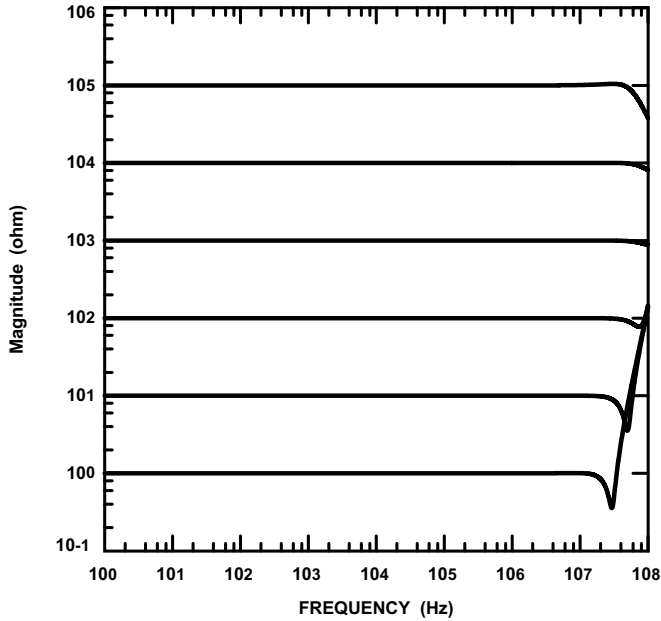


Fig. 24. Frequency characteristics of the transresistance gain for the transresistance amplifier configuration shown in Fig. 23.

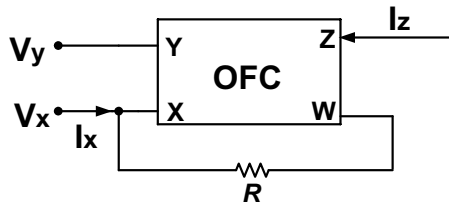


Fig. 25. The CCII⁺ configuration using the OFC.

The CCII⁺ is simulated with $R = 1\text{ k}\Omega$ and the input current at terminal X equals $10\text{ }\mu\text{A}$. The circuit is compensated by using a capacitor $C = 0.5\text{ pF}$ (connected between the output terminal W and the input terminal Y). The short circuit current transfer gain between terminals X and Z (I_z/I_x) is shown in Fig. 26.

It is obvious from the simulation results of the OFC applications introduced in Secs. 5.1–5.4 that the OFC exhibits wide bandwidth at high gain values. Hence, it provides wide bandwidth approximately independent of the gain.

5.6. Novel voltage-mode digitally controlled variable gain amplifier

5.6.1. Introduction

Variable gain amplifiers (VGAs) are used in many applications in order to maximize the dynamic range of the overall system. Hearing aids,¹⁰ disk drives,^{11,12} and

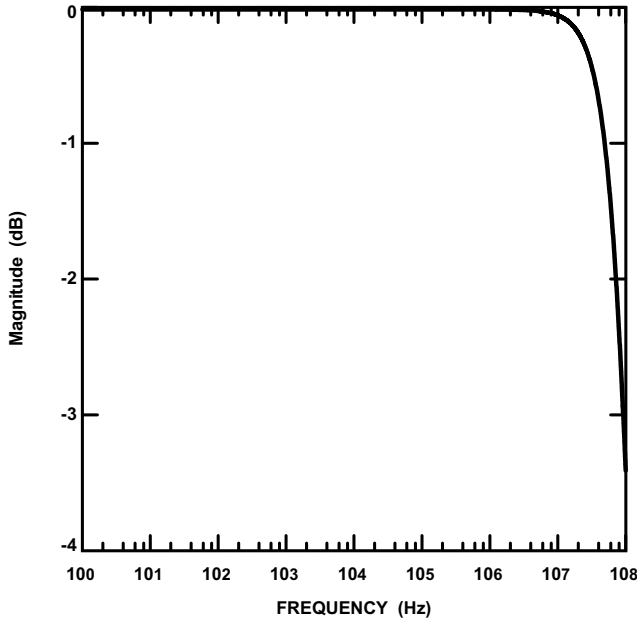


Fig. 26. Frequency characteristics of the short circuit current transfer gain between X and Z (I_Z/I_X) for the $CCII^+$ configuration shown in Fig. 25.

wireless communications are examples of such systems. In a wireless communication system, the portability of the terminal implies that the received signal has a very wide dynamic range. This necessitates the use of an automatic gain control (AGC) circuit. Its function is to automatically adjust the gain of the receive path so that the signal processed by the baseband section circuitry appears to be at a constant level regardless of the actual signal strength received at the antenna. The AGC contains mainly two blocks, a variable gain amplifier (VGA) and a signal strength detector which feeds back the control signal used to adjust the gain of the VGA. In modern wireless systems, all of the baseband signal processing is implemented digitally by a digital signal processor (DSP). A VGA controlled by an analog signal, will need additional digital-to-analog converter (DAC) in the AGC loop, increasing both complexity and delay. Hence, an essential requirement of the VGA is to be digitally controlled. The gain of the VGA should increase linearly on the decibel scale in order to achieve a wide gain control. Although traditional VGA topologies based on high open loop gain op-amps provide good results, they suffer from finite gain bandwidth product. Third generation wireless communication systems utilize wide band code division multiple access (WCDMA) techniques.¹³ Thus, the transmitted signal is to be spread over a wider range of bandwidth. It is thus necessary to investigate new CMOS amplifier-based VGA structures that can provide large bandwidth independent of the gain. This can be done by using the OFC-based voltage-mode digitally controlled VGA.

5.6.2. Circuit description

The novel voltage-mode digitally controlled VGA configuration is shown in Fig. 27. It depends on the voltage amplifier configuration shown in Fig. 17. Taking the effect of the finite transimpedance gain, Z_t , and using the finite transimpedance single pole model, from Eqs. (18b) and (20), the voltage gain of the first stage is given by:

$$\text{Voltage gain of the first stage } (A_{v_1}) = \frac{V_{o_1}}{V_i} = \left(1 + \frac{R_{f_1}}{R_1}\right) \left(\frac{1}{1 + sR_{f_1}C_p}\right). \quad (29)$$

It is clear from Eq. (29) that the gain of the first stage amplifier can be varied independently of the bandwidth by changing the resistance R_1 . Similarly, from Eq. (30), the gain of the second stage amplifier can be varied independently of the bandwidth by changing the resistance R_2 . To achieve the required gain control range and step, two VGA stages are cascaded. The first stage operates in a 6-dB step (coarse gain control) while the second VGA stage provides the precise 1-dB gain stepping (fine gain control). The VGA circuit is thus operating in a coarse and fine arrangement.

$$\text{Voltage gain of the second stage } (A_{v_2}) = \frac{V_o}{V_{o_1}} = \left(1 + \frac{R_{f_2}}{R_2}\right) \left(\frac{1}{1 + sR_{f_2}C_p}\right). \quad (30)$$

The digital control structure of the resistors R_1 and R_2 is shown in Figs. 28 and 29, respectively. The resistance R_1 is given by¹⁴:

$$R_1 = \overline{d_{10}}R_{11} + \overline{d_{11}}\{R_{12} + \overline{d_{12}}\langle R_{13} + \overline{d_{13}}(R_{14} + \overline{d_{14}}[R_{15} + \overline{d_{15}}(R_{16} + \overline{d_{16}}\{R_{17} + \overline{d_{17}}R_{18}\}])\rangle\}, \quad (31)$$

where R_{1i} ($i = 1, 2, 3, \dots, 8$) are polysilicon resistors and d_{1n} ($n = 0, 1, 2, \dots, 7$) are the digital inputs that control the value of R_1 . Table 5 shows the values of

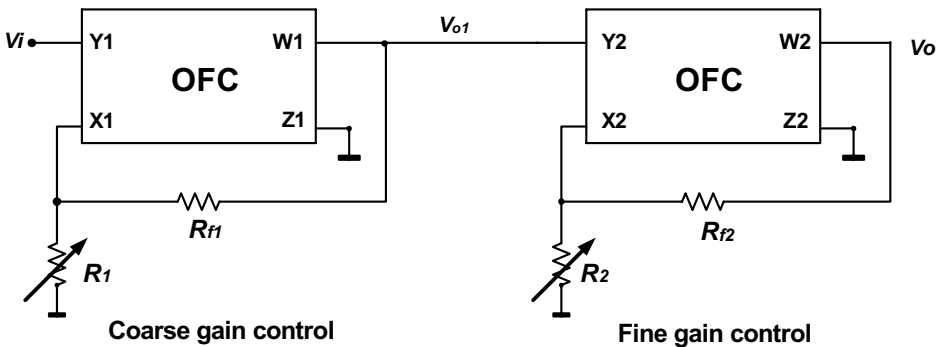


Fig. 27. The voltage-mode digitally controlled VGA using the OFC.

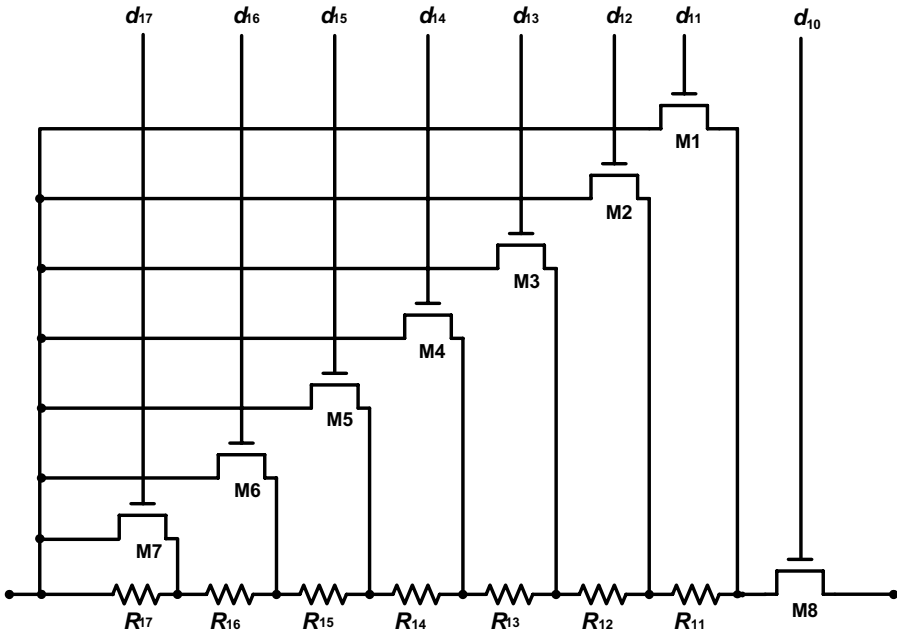


Fig. 28. The digitally controlled resistance R_1 .¹⁴

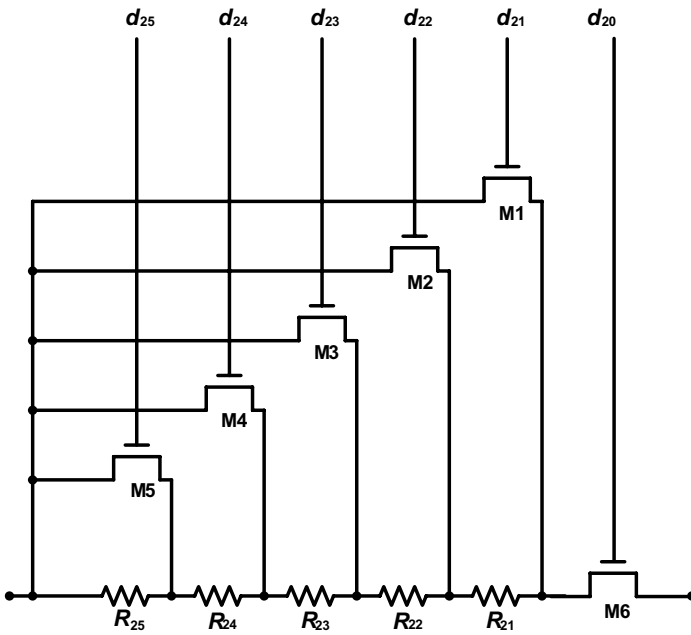


Fig. 29. The digitally controlled resistance R_2 .¹⁴

Table 5. The values of the resistors used to control the resistance R_1 of the first stage of the voltage-mode digitally controlled VGA shown in Fig. 2.

Resistor	Value
R_{11}	$0.008 R_{f1}$
R_{12}	$0.008 R_{f1}$
R_{13}	$0.016 R_{f1}$
R_{14}	$0.034 R_{f1}$
R_{15}	$0.076 R_{f1}$
R_{16}	$0.191 R_{f1}$
R_{17}	$0.667 R_{f1}$

Table 6. The digital inputs and the corresponding gain of the first stage of the voltage-mode digitally controlled VGA shown in Fig. 27.

Gain (dB)	d_{10}	d_{11}	d_{12}	d_{13}	d_{14}	d_{15}	d_{16}	d_{17}
0	0	1	0	0	0	0	0	0
6	1	0	0	0	0	0	0	0
12	1	0	0	0	0	0	0	1
18	1	0	0	0	0	0	1	0
24	1	0	0	0	0	1	0	0
30	1	0	0	0	1	0	0	0
36	1	0	0	1	0	0	0	0
42	1	0	1	0	0	0	0	0

these resistors in terms of the feedback resistor R_{f1} . The digital inputs and the corresponding gains are shown in Table 6. Similarly, the resistance R_2 is given by¹⁴:

$$R_2 = \overline{d_{20}}R_{21} + \overline{d_{21}}\{R_{22} + \overline{d_{22}}(R_{23} + \overline{d_{23}}[R_{24} + \overline{d_{24}}(R_{25} + \overline{d_{25}}R_{26})])\}, \quad (32)$$

where $R_{2i}(i = 1, 2, 3, \dots, 6)$ are polysilicon resistors and $d_{2n}(n = 0, 1, 2, \dots, 5)$ are the digital inputs that control the value of R_2 . Table 7 shows the values of these resistors in terms of the feedback resistor R_{f2} . The digital inputs and the corresponding gains are shown in Table 8.

5.6.3. Simulation results

The voltage-mode digitally controlled VGA is simulated using $R_{f1} = 4\text{ k}\Omega$ and $R_{f2} = 4\text{ k}$. The circuit is compensated by using capacitors $C_1 = 0.5\text{ pF}$ (connected between the output terminal of the first stage (V_{o1}) and its input $X1$ terminal) and $C_2 = 0.5\text{ pF}$ (connected between the output terminal of the second stage (V_o) and its input $X2$ terminal). The aspect ratios of all transistors used are identical ($W = 100\text{ }\mu\text{m}$ and $L = 0.5\text{ }\mu\text{m}$). Figure 30 shows the different gains of the overall VGA circuit ranging from 5 dB to 47 dB with a 6-dB gain step. It is clear that the bandwidth is about 42 MHz for the maximum gain of 47 dB and the average

Table 7. The values of the resistors used to control the resistance R_2 of the second stage of the voltage-mode digitally controlled VGA shown in Fig. 27.

Resistor	Value
R_{21}	$1.285 R_{f2}$
R_{22}	$0.425 R_{f2}$
R_{23}	$0.714 R_{f2}$
R_{24}	$1.438 R_{f2}$
R_{25}	$4.335 R_{f2}$

Table 8. The digital inputs and the corresponding gain of the second stage of the voltage-mode digitally controlled VGA shown in Fig. 27.

Gain (dB)	d_{20}	d_{21}	d_{22}	d_{23}	d_{24}	d_{25}
0	0	1	0	0	0	0
1	1	0	0	0	0	0
2	1	0	0	0	0	1
3	1	0	0	0	1	0
4	1	0	0	1	0	0
5	1	0	1	0	0	0

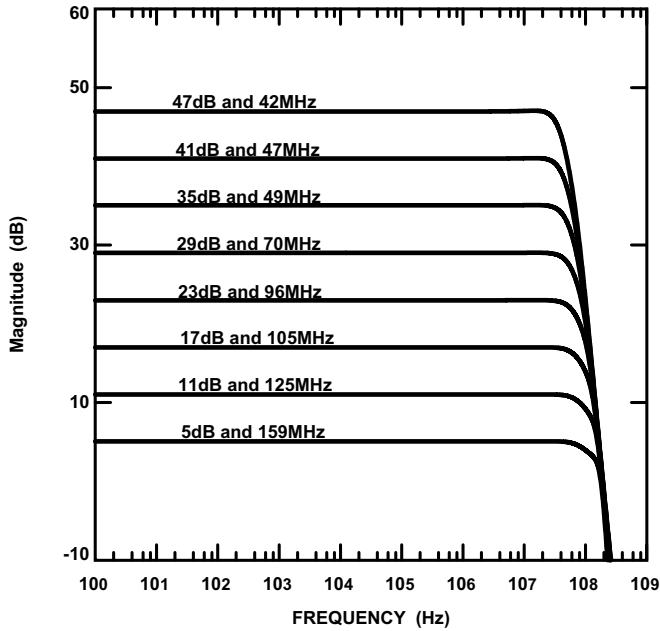


Fig. 30. Frequency characteristics of the overall voltage-mode digitally controlled VGA shown in Fig. 27 with different gains from 5 dB to 47 dB with 6 dB gain step.

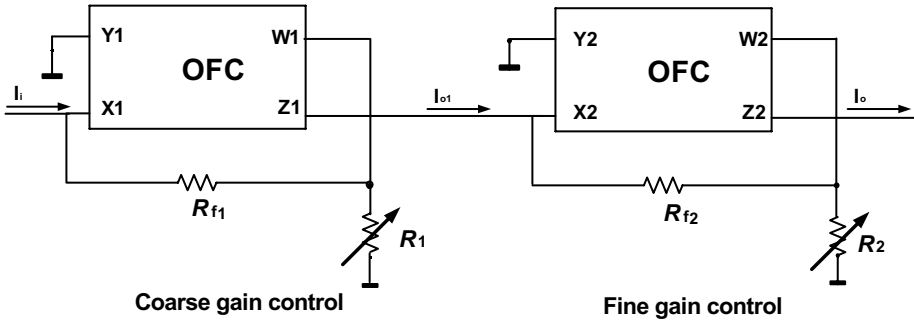


Fig. 31. The current-mode digitally controlled VGA using the OFC.

bandwidth is about 96 MHz at a gain of 23 dB. The average gain error is about 0.19 dB. The power dissipation of the circuit is about 3.12 mW.

5.7. Novel current-mode digitally controlled variable gain amplifier

5.7.1. Circuit description

A current-mode digitally controlled variable gain amplifier (VGA) is shown in Fig. 31. It is similar to the voltage-mode digitally controlled VGA introduced in Sec. 5.6. The two resistors R_1 and R_2 are the same as the two digitally controlled resistors R_1 and R_2 shown in Figs. 28 and 29, respectively. The digital inputs and the corresponding gains are similar to that given by Tables 6 and 8.

5.7.2. Simulation results

The current-mode digitally controlled VGA is simulated using $R_{f1} = 4\text{ k}\Omega$ and $R_{f2} = 4\text{ k}\Omega$. The circuit is compensated by using capacitors $C_1 = 0.5\text{ pF}$ (connected between the output terminal $W1$ of the first stage and its input $X1$ terminal) and $C_2 = 0.5\text{ pF}$ (connected between the output terminal $W2$ of the second stage and its input $X2$ terminal). Figure 32 shows the different gains of the overall current-mode digitally controlled VGA circuit ranging from 5 dB to 47 dB with a 6-dB gain step. It is clear that the bandwidth is about 39 MHz for the maximum gain of 47 dB and the average bandwidth is about 60 MHz at a gain of 23 dB. The average gain error is about 0.12 dB. The power dissipation of the circuit is about 3.12 mW.

6. Conclusion

This paper presents novel CMOS realizations of the operational floating conveyor (OFC) based on novel block diagrams. The OFC combines the features of CCII and CFOA. The proposed OFC realizations provide wide bandwidth at higher gain values. Different applications based on OFC are introduced such as: non-inverting voltage amplifier, inverting current amplifier, transresistance amplifier,

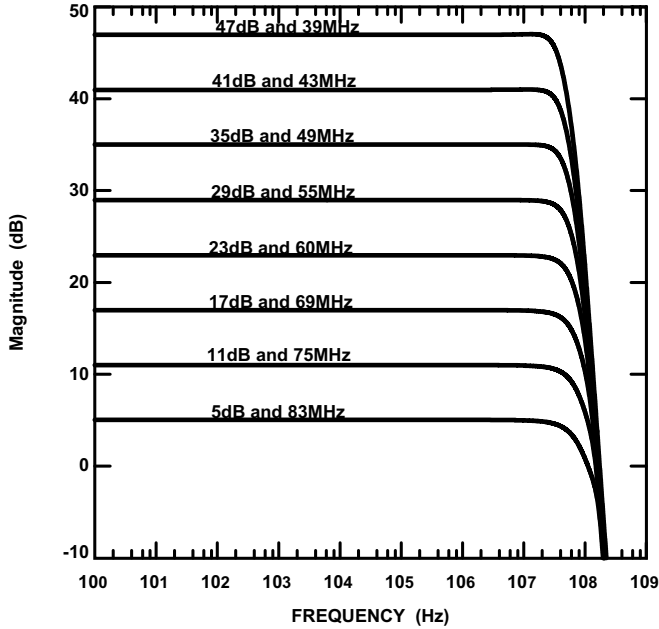


Fig. 32. Frequency characteristics of the overall current-mode digitally controlled VGA shown in Fig. 31 with different gains from 5 dB to 47 dB with 6 dB gain step.

transconductance amplifier, positive second generation current conveyor (CCII⁺), voltage-mode digitally controlled variable gain amplifier (VGA) and current-mode digitally controlled variable gain amplifier (VGA). Simulation results are presented and discussed.

References

1. K. C. Smith and A. Sedra, The current conveyor — A new circuit building block, *IEEE Proc.* **56** (1968) 1368–1369.
2. A. Sedra and K. C. Smith, A second generation current conveyor and its applications, *IEEE Trans. Circuit Theory* **17** (1970) 132–134.
3. F. Gohh, G. W. Roberts and A. Sedra, The current conveyor: History progress and new results, *IEE Proc.-G* **137** (1990) 63–77.
4. C. Toumazou, A. Payne and F. Lidgley, Operational floating conveyor, *Electron. Lett.* **27** (1991) 651–652.
5. H. O. Elwan, A. M. Soliman and M. Ismail, A CMOS Norton amplifier based digitally controlled VGA for low power wireless applications, *IEEE Trans. Circuits Syst. II* **48** (2001) 460–463.
6. G. Palmisano and G. Palumbo, A simple CMOS CCII⁺, *Int. J. Circuit Theor. Appl.* **23** (1995) 599–603.
7. A. F. Arbel and L. Goldminz, Output stage for current-mode feedback amplifiers, theory and applications, *Analog Integrated Circuits and Signal Processing* **2** (1992) 234–255.

8. M. A. Youssef and A. M. Soliman, A modified CMOS balanced output transconductor with extended linearity, *Analog Integrated Circuits and Signal Processing* **36** (2003) 239–244.
9. Y. H. Ghallab, M. A. El-Ela and M. K. El-Said, Operational floating current conveyor: Characteristics, modelling and experimental results, *The Eleventh International Conference on Microelectronics (ICM '99)*, November 1999, pp. 59–62.
10. J. Duque-Carillo, P. Malcovati, F. Maloberti, R. Perez-Aloe, A. Reyes, E. Sanchez-Sinecio, G. Torelli and J. Valverde, An acoustically programmable and adjustable CMOS mixed-mode signal processor for hearing aid applications, *IEEE J. Solid-State Circuits* **31** (1996) 634–645.
11. A. A. El-Adawy, A. M. Soliman and H. O. Elwan, Low-voltage fully differential CMOS voltage-mode digitally controlled variable gain amplifier, *Microelectron. J.* **31** (2000) 139–146.
12. R. Gomez and A. Abidi, A 50 MHz CMOS variable gain amplifier for magnetic data storage systems, *IEEE J. Solid-State Circuits* **27** (1992) 935–939.
13. G. Palmisano, G. Palumbo and S. Pennisi, A CMOS operational floating conveyor, *Proc. 37th Midwest Symp. Circuits Syst.*, Vol. 2, August 1994, pp. 1289–1292.
14. R. Harjani, A low-power CMOS VGA for 50 Mb/s disk drive read channels, *IEEE Trans. Circuits Syst. II* **42** (1995) 370–376.