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# A Low-Voltage Low-Power Rail-to-Rail Constant $g_m$ Transconductance Amplifier

**AHMED M. ELTAWIL*** **AND AHMED M. SOLIMAN**

*Department of Electronics and Communication Engineering, Cairo University, Egypt*

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**Abstract.** In this paper, a low-voltage low-power rail-to-rail constant $g_m$ transconductance amplifier (TA) is introduced. The supply voltages are set at ($\pm$ 1.5 V). The circuit depends on selecting the maximum transconductance ($g_m$) to achieve an almost constant $g_m$ over the entire common-mode (CM) range. The circuit is then used to realize a second-order 4 MHz lowpass filter consuming 530 $\mu$W, and a fifth-order 450 kHz lowpass elliptic filter consuming 2.3 mW. Both filters can be integrated on silicon without any external connections.

**Key Words:** analog VLSI, analog filters, low-power, low-voltage, transconductance amplifiers

## I. Introduction

The interest in low-power low-voltage integrated circuit (IC) has grown tremendously over the past few years. This is due to the development of portable hand-held electronic equipment like, for instance, portable computers and telecommunication equipment. Also there has been an increasing demand on highly efficient, ultra low power processing chips which integrate both analog and digital blocks.

From the technical point of view, decreasing the power supply has become a necessity, not just a commodity due to the decrease of the minimum feature size which places a bound on the maximum electric field that can be sustained. Once the critical electric field is reached any further decrease in feature size must be compensated for by a decrease in the supply voltage. All these reasons have motivated analog designers to perfect low-voltage analog circuit techniques.

In the field of communications, complete RF CMOS transceivers have been introduced [1,2] encompassing both analog RF front end signal processing blocks and digital processing core. Although switched capacitance (SC) provide an attractive solution in discrete time analog signal processing they are difficult to deal with at low voltages. $g_m$-C filters on the other hand are versatile blocks that can be easily controlled, however $g_m$-C filters fall short when a high degree of accuracy is required. This is not a very serious drawback because several existing communication systems do not require a high degree of accuracy. For example in code division multiple access (CDMA) systems a 4 to 8 bit representation of the data is enough for an acceptable signal to noise ratio [3]. Ever since the $g_m$-C integrator was introduced [4] several techniques for synthesizing different filters were presented [5–7].

In Section II of this paper a rail-to-rail low-voltage low-power CMOS TA is introduced and analyzed. Section III presents simulations of the circuit. Two lowpass filter configurations and their simulations are introduced in Section IV.

## II. Proposed Transconductor

### A. *Principle of Operation*

Several techniques for obtaining a constant low-voltage rail-to-rail TA have been presented. The traditional method is to control the DC tail currents of the differential input stages. This can be basically divided into two main methods, the first is to keep the sum of the tail currents flowing through both n- and p-type input pairs constant, thus achieving a constant transconductance [8]. Bipolar circuits using this technique are presented in [8,9] while weak inversion

*Present address: Department of Electrical Engineering, University of California, Los Angeles (UCLA), USA

CMOS circuits are presented in [10,11]. The second method is suited for MOS circuits operating in the strong inversion. The principle of operation depends on keeping the sum of the square roots of the tail currents constant thus achieving constant transconductance [11–14]. A more general approach which is independent of the input transistor types and their operating region is to select only the currents that provide maximum $g_m$ thus achieving constant rail-to-rail operation [15]. In [16] a circuit is presented that implements this concept. The circuit consists of an n-type V-I converter cell connected in parallel with a p-type V-I converter cell to achieve common-mode rail-to-rail operation. Two maximum-current selection circuits and an output current subtraction circuit are utilized to generate a constant $g_m$ output current.

The proposed TA implements the same functionality as the circuit presented in [16] with different circuit structures. The core of the TA is a simple differential pair. Equations of the total instantaneous currents of a simple differential pair are well known and can be found in many references [17,18].

The currents in the two transistors of the pair are expressed by

$$Io_{1,2} = \frac{I_T}{2} \pm g_m \frac{V_{id}}{2} \tag{1}$$

where $I_T$ is the tail current, $g_m$ is the transconductance, $V_{id}$ is the differential input voltage.

The CM input voltage range of a p-channel differential input stage is restricted to a range from the negative rail voltage up to the positive rail voltage minus the gate-source voltage and the saturation voltage of the tail current source. The CM input voltage range of a n-channel differential input stage is restricted to a range from the positive rail voltage down to the negative rail voltage plus the gate-source voltage and the saturation voltage of the tail current source as shown in Fig. 1.

Therefore by combining together two complementary input stages as shown in Fig. 2, rail-to-rail operation can be achieved. Ignoring the body effect, andusing the quadratic equations of an MOS in saturation (strong inversion) the input common-mode voltage $V_{CM}$ of this input stage is limited to

$$V_{CM,\min} = V_{SS} + \sqrt{\frac{I_{Tp}}{K_n}} + V_{Tn} - |V_{Tp}| \tag{2}$$

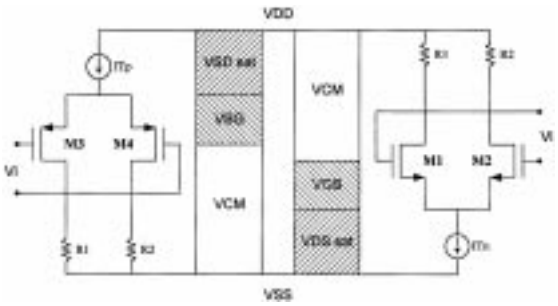


*Fig. 1.* CM range of P and N type CMOS differential stages.

$$V_{CM,\max} = V_{DD} - \sqrt{\frac{I_{Tn}}{K_p}} + V_{Tn} - |V_{Tp}| \tag{3}$$

where $I_{Tn,p}$ is the n- and p-tail current, respectively. $V_{Tn,p}$ is the n- and p-transistor threshold voltages, respectively.

$$K_n = \mu_n C_{ox} \left(\frac{W}{L}\right)_n$$

where $\mu_n$ is the electron mobility, $C_{ox}$ is the gate oxide capacitance, $(W/L)_n$ is the aspect ratio of the NMOS transistors $M_1$, $M_2$.

$$K_p = \mu_p C_{ox} \left(\frac{W}{L}\right)_p$$

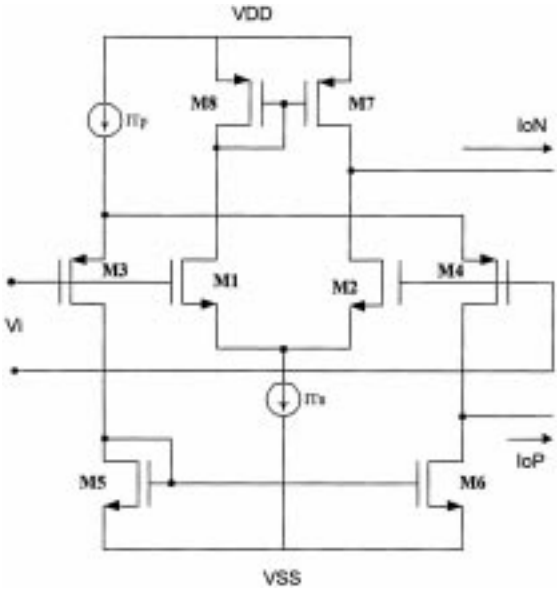


*Fig. 2.* Complementary CMOS rail-to-rail transconductance.

where $\mu_p$ is the electron mobility, $C_{ox}$ is the gate oxide capacitance, $(W/L)_p$ is the aspect ratio of the PMOS transistors $M_3$, $M_4$.

$V_{DD}$ and $V_{SS}$ are the positive and negative supply rails, respectively.

The rail-to-rail operation can be further improved by using a folded cascode configuration for the input stage.

The currents in the transistors forming the differential pair in Fig. 2 can be expressed as

$$I_{n1} = \frac{I_{Tn}}{2} + g_{mn}\frac{V_{id}}{2} \tag{4}$$

$$I_{n2} = \frac{I_{Tn}}{2} - g_{mn}\frac{V_{id}}{2} \tag{5}$$

$$I_{p3} = \frac{I_{Tp}}{2} - g_{mp}\frac{V_{id}}{2} \tag{6}$$

$$I_{p4} = \frac{I_{Tp}}{2} + g_{mp}\frac{V_{id}}{2} \tag{7}$$

where
$I_{n1}$ is the drain current of $M_1$,
$I_{n2}$ is the drain current of $M_2$,
$I_{p3}$ is the drain current of $M_3$,
$I_{p4}$ is the drain current of $M_4$.

The CM input range can be divided into three regions as shown in Fig. 3.

The equations describing the currents in these regions are as follows:

*Region 1*. With $V_{CM}$ close to the negative rail, the p input stage is fully functional drawing a current equal to the maximum tail current, however the n input stage does not reach the maximum value of the tail current.

Thus

$$I_{Tn} < I_{Tp} \qquad g_{mn} < (g_{mp} = g_{mmax}) \tag{8}$$

$$I_{n1} = \frac{I_{Tn}}{2} + g_{mn}\frac{V_{id}}{2} \tag{9}$$

$$I_{n2} = \frac{I_{Tn}}{2} - g_{mn}\frac{V_{id}}{2} \tag{10}$$

$$I_{p3} = \frac{I_{Tp}}{2} - g_{m\,max}\frac{V_{id}}{2} \tag{11}$$

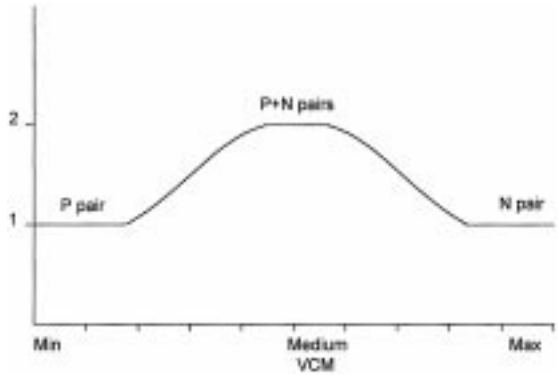


*Fig. 3*. Transconductance versus CM voltage of a rail-to-rail complementary CMOS stage.

$$I_{p4} = \frac{I_{Tp}}{2} + g_{m\,max}\frac{V_{id}}{2} \tag{12}$$

*Region 2*. With $V_{CM}$ close to the middle rail, both stages are fully functional drawing the maximum tail currents. This region exists only under the condition that $V_{DD} - V_{SS} > V_{Tn} + V_{Tp}$.

Thus

$$I_{Tn} = I_{Tp} \qquad g_{mn} = g_{mp} = g_{m\,max} \tag{13}$$

The current equations are identical to equations (4)–(7) where each $g_{mn}$ or $g_{mp}$ is replaced by $g_{m\,max}$.

*Region 3*. With $V_{CM}$ close to the positive rail, the N input stage is fully functional drawing a current equal to the maximum tail current, however the P input stage does not reach the maximum value of the tail current.

Thus

$$I_{Tp} < I_{Tn} \qquad g_{mp} < \left(g_{mn} = g_{m\,max}\right) \tag{14}$$

$$I_{n1} = \frac{I_{Tn}}{2} + g_{m\,max}\frac{V_{id}}{2} \tag{15}$$

$$I_{n2} = \frac{I_{Tn}}{2} - g_{m\,max}\frac{V_{id}}{2} \tag{16}$$

$$I_{p3} = \frac{I_{Tp}}{2} - g_{mp}\frac{V_{id}}{2} \tag{17}$$

$$I_{p4} = \frac{I_{Tp}}{2} + g_{mp}\frac{V_{id}}{2} \tag{18}$$

Over the entire CM range by processing the instantaneous currents and selecting only those having $g_{m=g_{mmax}}$, an almost constant rail-to-rail transconductance is achieved [15].

### *B. Maximum Selection Circuit*

Two circuit implementations are proposed for the maximum selection circuit. The first implementation is a simple 5 transistor cell as shown in Fig. 4. Assuming without loss of generality that $I_1 > I_2$. $M_1$ will be operating in the saturation region and the diode connected transistor $M_3$ will be on with zero current. In the other branch $M_2$ will have to operate in the triode region due to the applied $V_{gs}$ set by $M_1$. This in turn will turn off $M_4$. Finally the output current will therefore be equal to the maximum current which is in this case $I_1$. The dynamic operation of this circuit will be limited to a rather narrow bandwidth. The reason is that the node at the gate of $M_1$, $M_2$ has a relatively large time constant.

Another circuit based on the same principle can be envisioned as shown in Fig. 5. By connecting the drains of $M_3$, $M_4$ to the supply and providing a path to ground via $M_6$ the new circuit has a much wider bandwidth, thus improving the overall performance of the TA. This modification slightly increases the power budget of the circuit but drastically improves the performance.

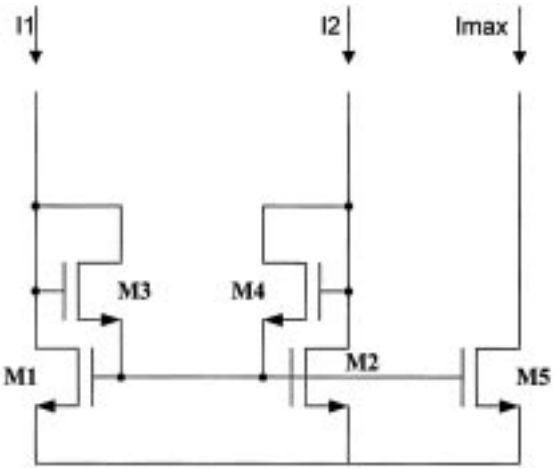


*Fig. 4.* Maximum selection circuit.

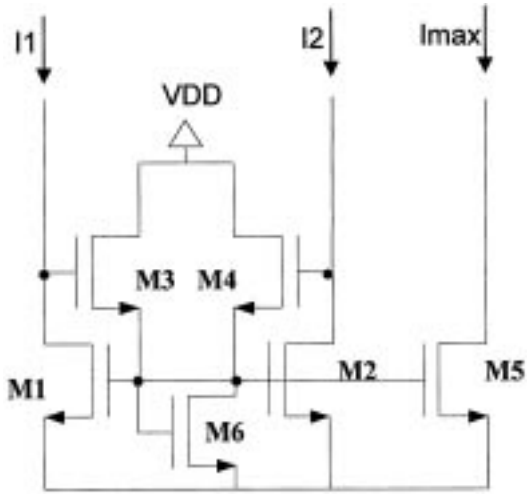


*Fig. 5.* Modified maximum selection circuit.

Fig. 6 presents a transient simulation in which $I_1$ is a sinusoidal input of amplitude 20 $\mu$A while $I_2$ is a sinusoidal input of amplitude 10 $\mu$A. Both inputs have a DC component of 20 $\mu$A. The output then should select the maximum, which is 20 $\mu$A in the positive half-cycle and 10 $\mu$A in the negative half-cycle. The frequency of the input signals is 100 kHz.

### *C. Complete Circuit*

The complete circuit diagram is shown in Fig. 7. The currents from transistor $M_1$ (N pair) and $M_4$ (P pair) are compared and the maximum is selected by the transistors $M_8$–$M_{14}$. Similarly the currents from transistor $M_2$ (N pair) and $M_3$ (P pair) are compared and the maximum is selected by the transistors $M_{15}$–$M_{19}$, the current is then mirrored by the action of $M_{21}$ to the output transistors. The difference between the two output transistors then represents the final output current. The current mirrors are implemented as simple current mirrors, where each current mirror consists of a diode connected transistor and a replica output transistor. The circuit symbol is shown in Fig. 8. The sizing of all transistors is illustrated in Table 1. Table 2 presents the THD of a 0.6 $V_{pp}$ input signal at different operating frequencies.

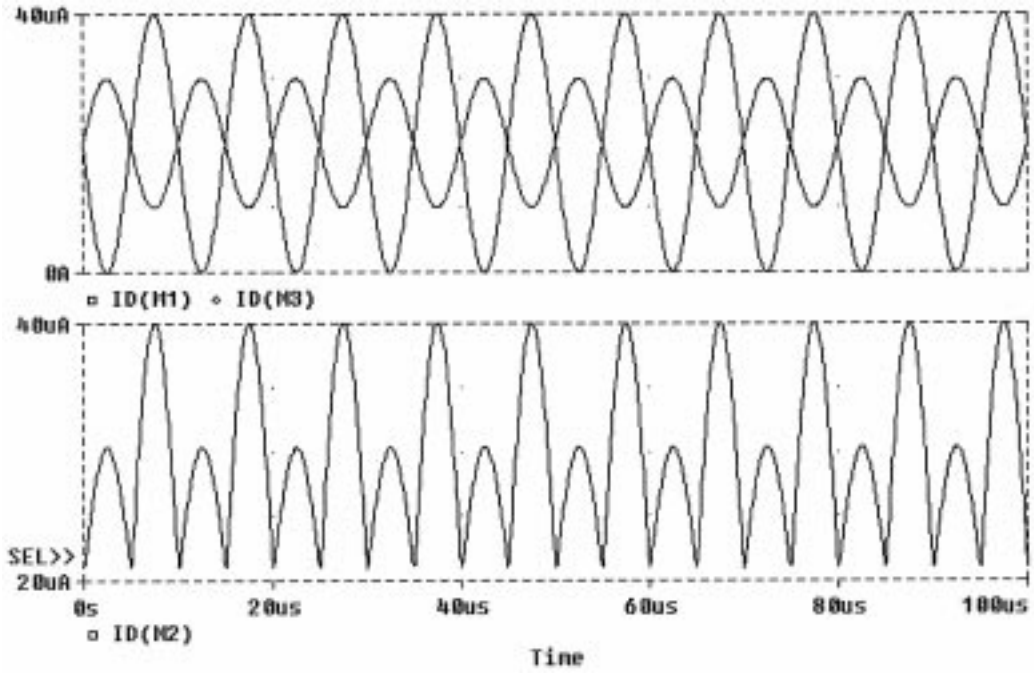


*Fig. 6.* Transient simulation of the maximum selection circuit.

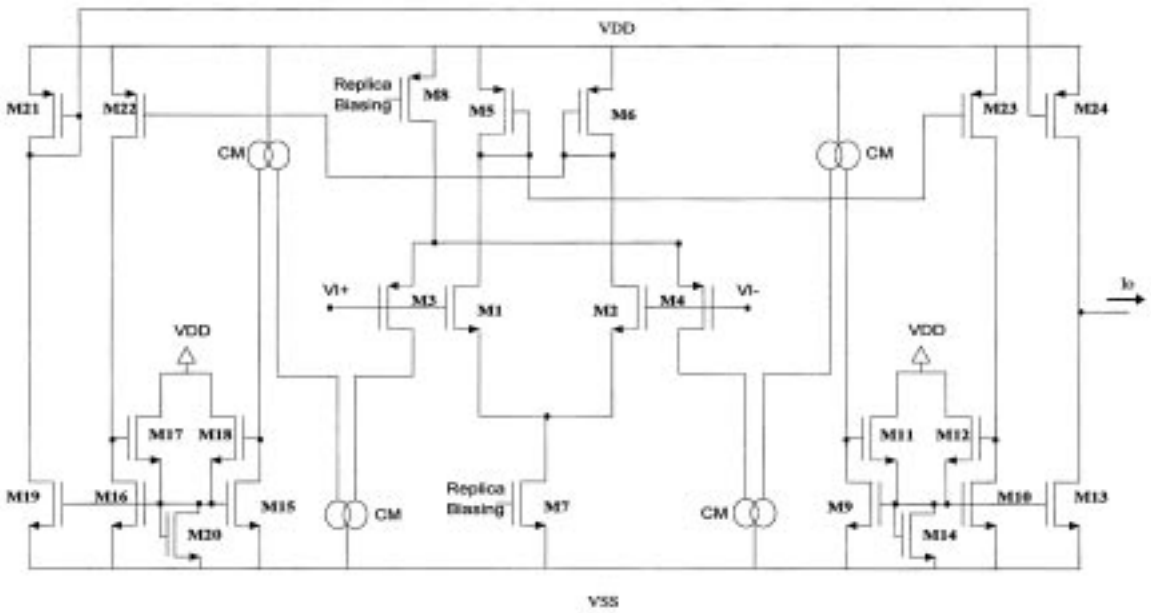


*Fig. 7.* Complete circuit diagram of the proposed TA.

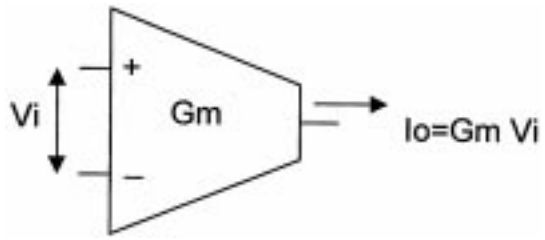


*Fig. 8.* TA symbol.

*Table 1.* Transistor sizing.

| Transistors | Sizes ($\mu$m) | | Function |
|---|---|---|---|
| | W | L | |
| $M_1$ $M_2$ | 1.8 | 1.2 | N Differential pair |
| $M_3$ $M_4$ | 4.8 | 1.2 | P Differential pair |
| $M_5$ $M_6$ $M_{21}$ $M_{22}$ $M_{23}$ $M_{24}$ | 96 | 2.4 | P Mirroring transistors |
| $M_9$ $M_{10}$ $M_{13}$ | 48 | 2.4 | Maximum selection circuit |
| $M_{11}$ $M_{12}$ | 4.8 | 2.4 | |
| $M_{14}$ | 12 | 1.2 | |
| N Current mirror (CM) | 48 | 2.4 | N Current mirror |
| P Current mirror (CM) | 96 | 2.4 | P Current mirror |
| $M_7$ | 8.4 | 2.4 | N Biassing transistor |
| $M_8$ | 44.4 | 2.4 | P Biassing transistor |

*Table 2.* THD simulation for a 0.6 Vpp signal.

| Input Frequency | THD |
|---|---|
| 100 kHz | 0.871% |
| 500 kHz | 0.876% |
| 1 MHz | 0.888% |
| 10 MHz | 1.53% |
| 30 MHz | 3.24% |

## III. Simulation Results

Simulation results using a 1.2 $\mu$m transistor model supplied by MOSIS are shown in Figs. 9–11. Fig. 9 shows the output current versus a DC sweep of the tail current from 16 to 22 $\mu$A in steps of 2 $\mu$A. Fig. 10 shows the output current for a rail-to-rail sweep of the CM voltage while fixing the differential input voltage at 0.2, 0.25 and 0.3 V, respectively. Clearly the $g_m$ is almost constant with a variation of less than 5%. The frequency response of the proposed circuit is shown in Fig. 11. The 3 dB frequency is 41 MHz at a VCM of zero volt. The bandwidth of the TA is a function of the available power. By increasing the power dissipation a higher 3 dB frequency can be achieved.

## IV. Applications

The proposed TA was used to implement two different lowpass circuits. A second order lowpass maximally flat response filter with a cutoff frequency of 4 MHz [5] suitable for wide band applications. The filter consumes 530 $\mu$W. The second filter simulated is a fifth order elliptic filter with a cutoff frequency of 450 kHz [16]. The filter consumes 2.3 mW. Due to the rail-to-rail feature of the TA it is insensitive to its position in the circuit which eliminates the need for DC level shifting.

The capacitance values can be easily calculated using an LC realization and either direct element replacement or signal flow graph methods to perform the mapping to a $g_m$-C filter [5–7].

Fig. 12 shows the circuit diagram of the second order low pass filter, Fig. 13 shows the frequency response of the filter when operating at different CM voltages. The values of the capacitance used are as follows:

$$\text{C1} = 1.8564 \text{ pF C2} = 0.9282 \text{ pF}$$

The maximum capacitance used in the second order low pass filter is only 1.86 pF.

Fig. 14 shows the circuit diagram of the fifth order elliptic low pass filter, Fig. 15 shows the frequency response of the filter when operating at different CM voltages. The values of the capacitance used are as follows:

$$\text{C1} = 14.07\,\text{pF},\ \text{C2} = 0.57\,\text{pF}$$

$$\text{C3} = 17.57\,\text{pF},\ \text{C4} = 1.97\,\text{pF}$$

$$\text{C5} = 8.95\text{pF},\ \text{CL2} = 24.1\,\text{pF}$$

$$\text{CL4} = 15.21\,\text{pF}$$

The maximum capacitance used in the filter is only 24 pF.

Due to the small values of the capacitors both circuits can be integrated easily on an integrated circuit without any external components.

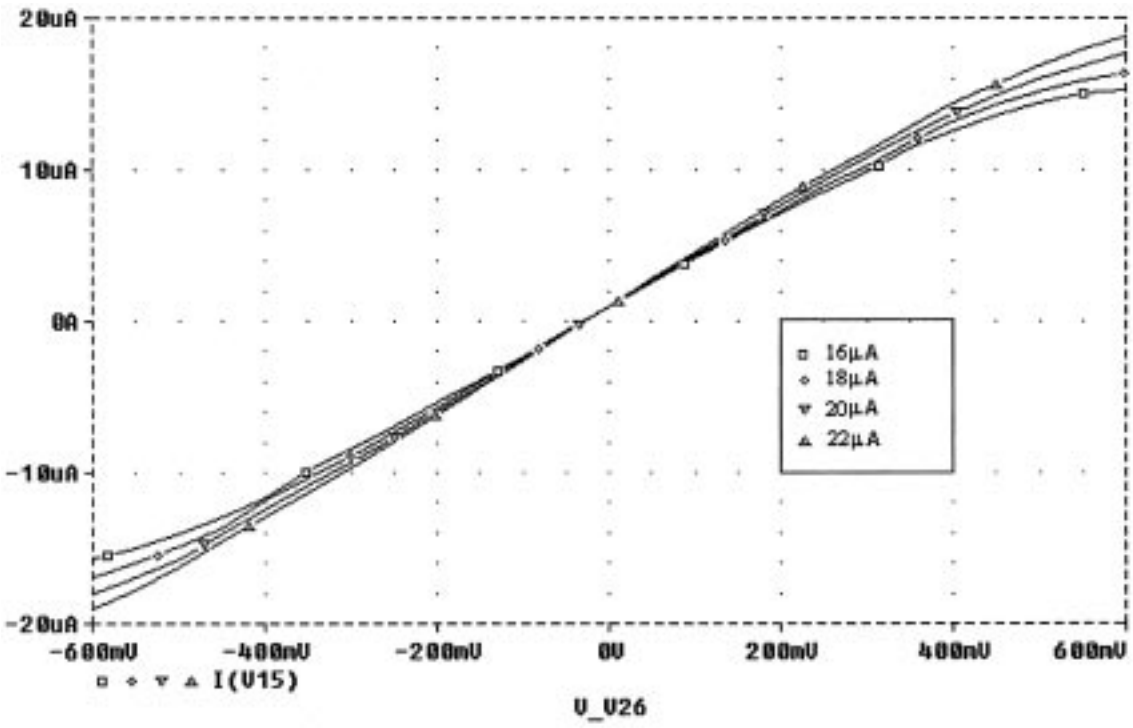


*Fig. 9.* Output current vs. step sweep of control current.

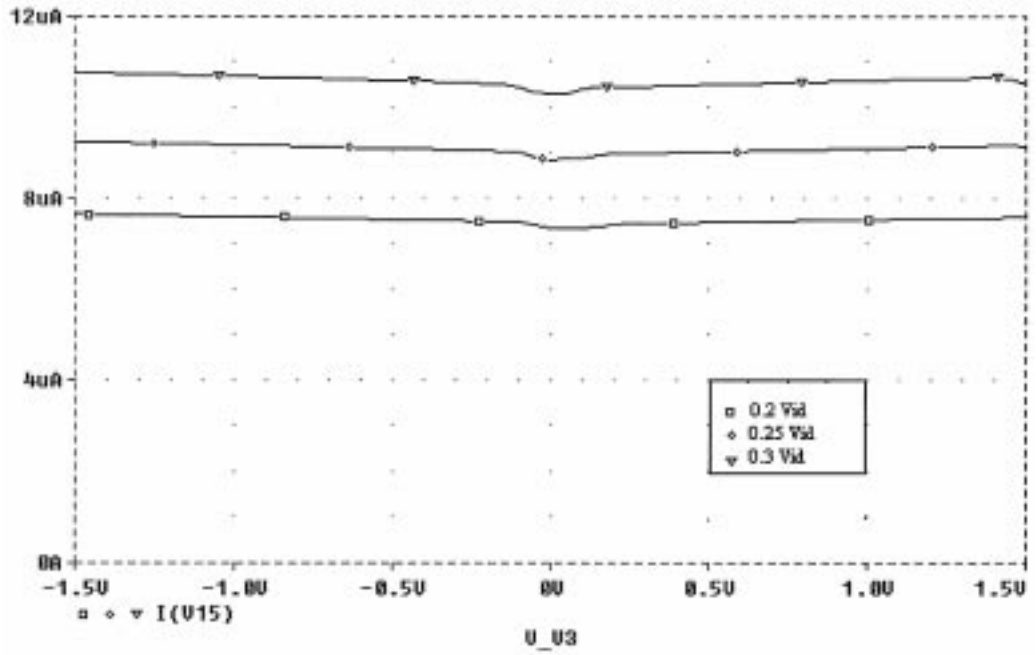


*Fig. 10.* Output current vs. a rail-to-rail sweep of the CM voltage at fixed differential input.

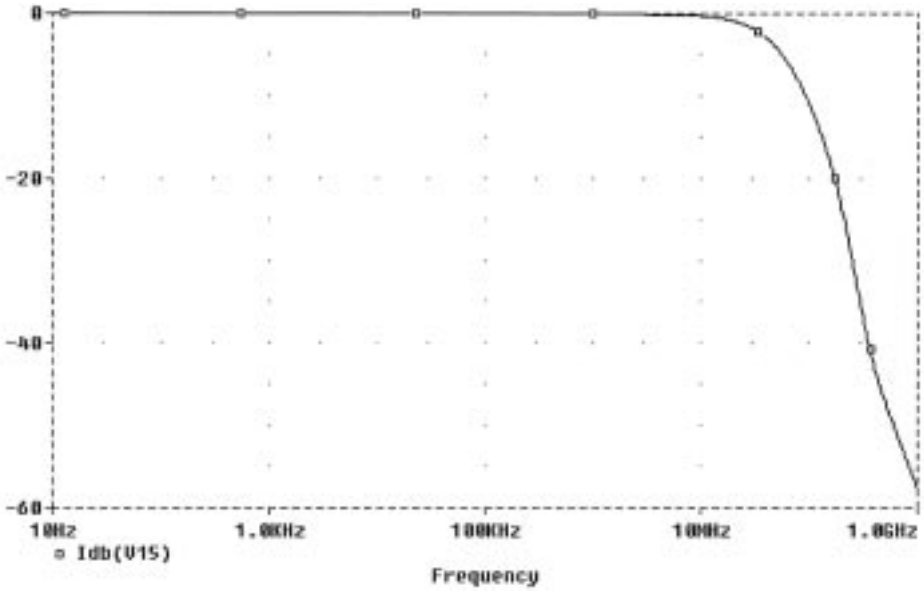


*Fig. 11.* Frequency response of the TA for different values of the CM voltage.

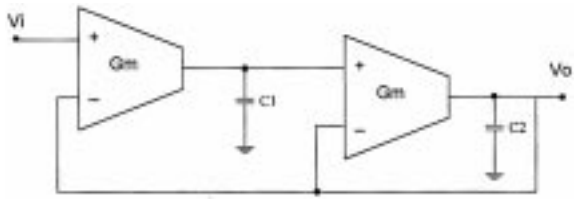


*Fig. 12.* Second order filter circuit diagram.

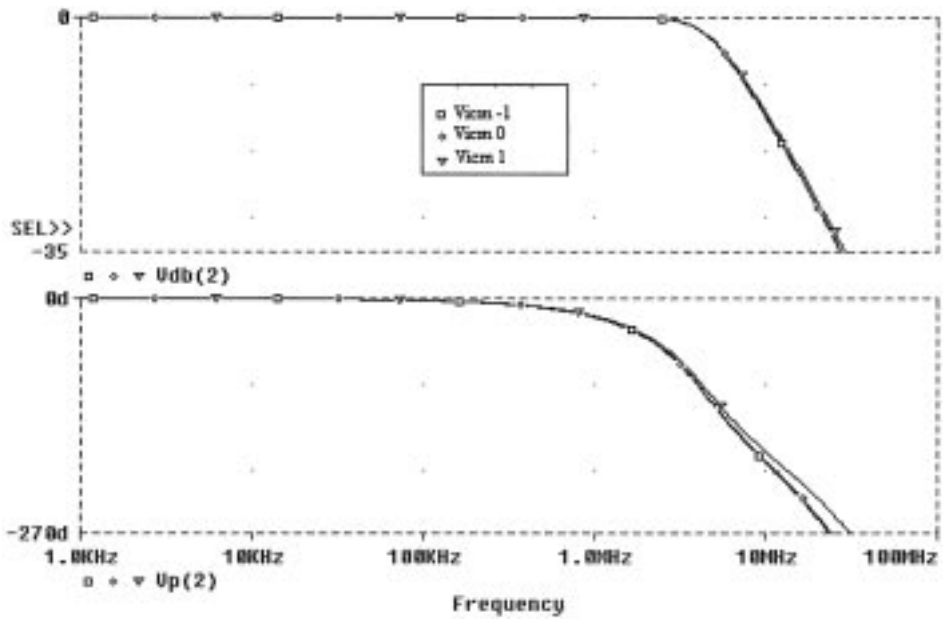


*Fig. 13.* Frequency response of the 2nd order filter for different values of the CM voltage.

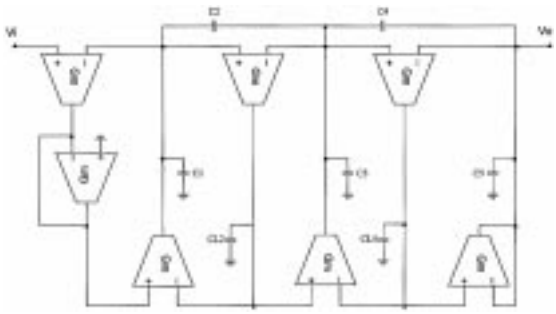

*Fig. 14.* Fifth order elliptic filter circuit diagram.

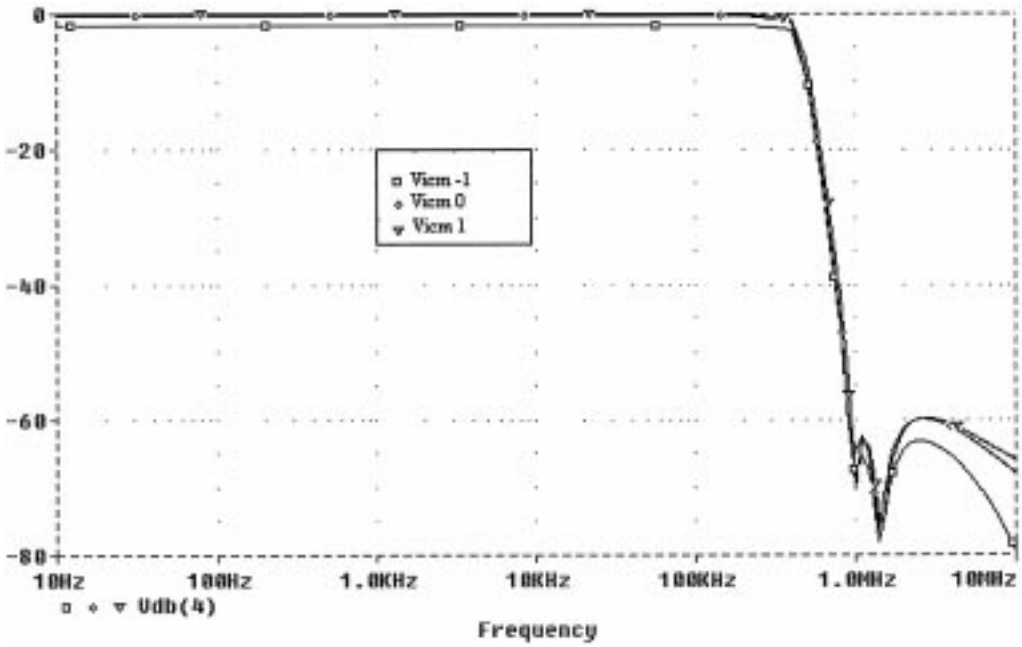


*Fig. 15.* Frequency response of the 5th order filter for different values of the CM voltage.

## V. Conclusion

In this paper a robust low power low voltage rail-to-rail CMOS TA was presented. The equations describing the operation of the circuit in different regions of the CM voltage were discussed. Due to the rail-to-rail feature of the TA it is insensitive to its position in the circuit which eliminates the need for DC level shifting. The TA was used to implement two different lowpass filters and the simulated responses were plotted for different CM voltages. The presented TA is a versatile circuit that can be used to build a large family of $g_m$-C filters.

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**Ahmed M. Eltawil** received his B.Sc. with honors from the Electronics and Communications Department, Cairo University, Egypt in 1997. In the same year he joined the VLSI wireless research group at Cairo University where he conducted research in low power, low voltage circuits for wireless applications. He was granted his M.Sc. degree in 1999 from the same university. He then joined the Electrical Engineering Department, University of California, Los Angeles (UCLA) where he is currently working towards his Ph.D. degree. He is a member of the wireless systems research laboratory at UCLA where his primary research interest is the development of highly flexible low power VLSI ASICs for wireless communication systems. He has held a summer intern position at the British Broadcasting Corporation (N. Ireland), Technical Division (BBC).

**Ahmed M. Soliman** was born in Cairo, Egypt, on November 22, 1943. He received the B.Sc. degree with honors from Cairo University, Egypt, in 1964, the M.Sc. and Ph.D. degrees from the University of Pittsburgh, Pittsburgh, PA, U.S.A. in 1967 and 1970, respectively, all in electrical engineering.

He is currently Professor and Chairman, Electronics and Communications Engineering

Department, Cairo University, Egypt. From 1985–1987, Dr. Soliman served as Professor and Chairman of the Electrical Engineering Department, United Arab Emirates University, and from 1987 to 1991 he was the Associate Dean of Engineering at the same University.

He has held visiting academic appointments at San Francisco State University, Florida Atlantic University and the American University in Cairo.

He was a visiting scholar at Bochum University, Germany (Summer 1985) and with the Technical University of Wien, Austria (Summer 1987).

In 1977, Dr. Soliman was decorated with the First Class Science Medal, from the President of Egypt, for his services to the field of Engineering and Engineering Education.