Current Conveyor Chaos Generators

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***Abstract*—New RC chaos generators that utilize the second-generation current conveyor (CCII) as the active building block are presented. The very small input resistance associated with the current conveyor low-impedance input terminal is shown to be responsible for stimulating the circuits' chaotic nature. The proposed chaotic oscillators originate from two sinusoidal oscillator circuits which are modified for chaos by replacing one of the linear resistors with a nonlinear resistor of antisymmetric current–voltage characteristics and adding a single capacitor. The elementary linear design equations of the sinusoidal oscillators are used as a start point for chaos modification to estimate all component values and identify tunable elements. Mathematical models of the proposed generators are derived and further modified to demonstrate chaotic behavior with odd symmetrical nonlinearities. Suitability for VLSI integration is discussed. PSpice circuit simulations, numerical simulations of the derived models, and experimental results are included.**

***Index Terms*—Chaos generations, current conveyors.**

I. Introduction

The second-generation current conveyor (CCII) [1] is a versatile analog building block that presents an alternative method of implementing analog systems which traditionally have been based on voltage op amps. Conveyor-based implementations offer improved performance to the voltage op amp based implementations in terms of accuracy, bandwidth, and convenience due to the inherent local feedback of the follower based structure of the device and its very attractive combined voltage–current capabilities. The voltage–current describing matrix of the CCII is given by

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix} \tag{1}$$

which indicates that the voltage at the low-impedance input node (X) follows that at the high-impedance input node (Y), while the input current at node (X) is mirrored (conveyed) to the high-impedance output node (Z). There are different methods to transform an op amp circuit to its CCII equivalent circuit [2], [3]. A theorem relating a class of op amp and current conveyor circuits was also introduced in [4].

Recently, chaotic signals have shown to be very useful in applications such as signal encryption and secure communication. A considerable amount of analog and digital signal processing is usually required for such applications. Hence, chaotic oscillators that are suitable for VLSI integration are advantageous [5], [6]. Novel chaotic oscillators based on an operational transconductance amplifier (OTA) have been introduced in [7] and [8]. Such oscillators can be integrated. It is the aim of the work presented here to introduce two new RC chaos generators that utilize a single CCII device as the active building block. The CCII was originally introduced in bipolar technology [1]. However, most recently, attractive CMOS CCII realizations have been reported in [9] and [10]. In particular, using any of the low-power low-voltage realizations of [10] in the proposed chaos generators is of benefit to communication applications. Moreover, developing interest in investigating the possible chaotic nature of well-known sinusoidal oscillator circuits has been observed. It was first shown in [11] that the Colpitts oscillator can behave chaotically. The nonlinearity in this oscillator, introduced by a bipolar transistor operating in both the forward active and the cut-off regions, is antisymmetric and is modeled by two segment piecewise linear characteristics [12]. Different modifications of the Wien-bridge oscillator that lead to simple RC chaos generators have been also introduced [13]–[16]. Two more RC chaotic oscillators based on the Twin-T network were recently presented in [17]. The chaotic oscillators in this article are also based on two sinusoidal oscillator circuits.

In Section II the first chaotic oscillator is presented, with the procedure of obtaining it from the original sinusoidal oscillator circuit, making use of its linear design equations, emphasized. An antisymmetric nonlinearity formed by a junction field effect transistor (JFET) operating as a voltage-controlled resistor and modeled by two segment piecewise linear characteristics is used. The very small input resistance associated with the CCII (X) terminal is shown to be responsible for stimulating the chaotic behavior in opposition to other cases where the internal voltage op amp dominant pole was shown to play the same role [16]. A mathematical model that describes the observed behavior is derived, and further modified, to demonstrate chaos using a cubic nonlinearity.

In Section III, the second chaotic oscillator which is obtained from one of the canonic bandpass networks of [18] is introduced. Emphasis is given to the oscillator of Section II, however, similar results can be obtained for the circuit in this section. Suitability for VLSI implementation of both chaos generators is further discussed in Section IV. Mathematical models, PSpice simulations and experimental results are included.

II. The First CCII Chaos Generator

Shown in Fig. 1(a) is the first CCII chaos generator which requires a single CCII, three linear resistors, three capacitors, and a JFET connected as a diode, and thus operating in the triode region. If the JFET is replaced with a linear resistor (R_1) and capacitor C_3 is eliminated, the original CCII sinusoidal oscillator is retrieved. For this oscillator, the recommended design is to take

$$R_1C_1 = R_2C_2. \tag{2a}$$

In this case the condition and radian frequency of oscillation are given respectively by

$$\frac{2R_3}{R_4} = \frac{R_2}{2R_1} - 1 \quad \text{and} \quad \omega_o = \frac{1}{R_2C_2}. \tag{2b}$$

A simple design set that satisfies (2a) and (2b) is to take

$$R_1 = R_3 = R, \quad R_2 = 4R, \quad R_4 = 2R \quad \text{and} \quad C_1 = 4C_2. \tag{3}$$

In the modified for chaos circuit of Fig. 1(a), resistor R_1 has been replaced with a JFET and a capacitor C_3 has been added. Although JFET's suffer from a large manufacturing spread, and are rather temperature sensitive, they offer a simple means of implementing linear and nonlinear voltage-controlled resistors with good performance [19]. A JFET of the type J2N4338, especially suitable as a voltage-

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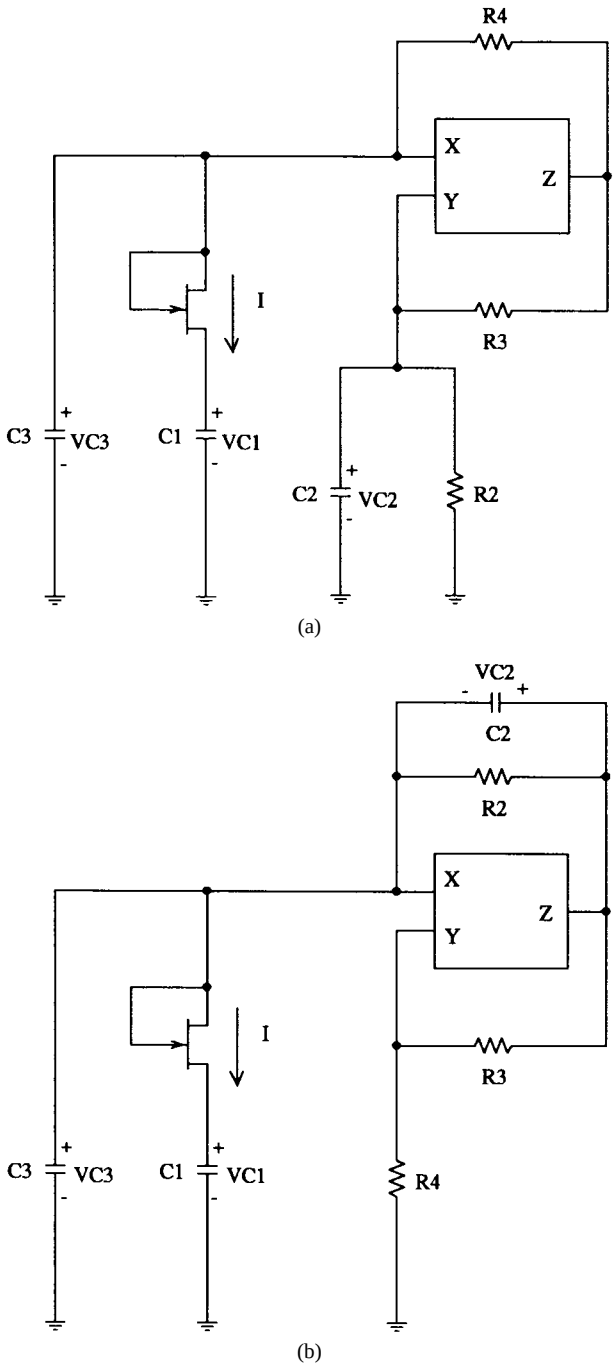


Fig. 1. The two proposed chaos generators using a single CCII.

controlled resistor, was chosen and used in PSpice simulations and experimental work. An approximate two-segment piecewise linear model of the JFET current–voltage characteristics is given by

$$I = \frac{1}{R_J}\begin{cases} V_{GD} & V_{GD} \geq V_T \\ V_T & V_{GD} < V_T \end{cases} \tag{4}$$

where R_J is the JFET small signal resistance at the operating point, V_{GD} is the JFET gate to drain voltage, and V_T is the threshold voltage approximately equal to (-0.66 V) for the J2N4338.

Adopting the design set of (3), then the values of R_2, R_3, and R_4 should be taken as around $4R_J$, R_J, and $2R_J$, respectively, whereas the sum of capacitors C_1 and C_3 should be taken four times C_2. The optimum choice was found to be $C_1 = C_3 = 2C$ and $C_2 = C$ with the value of C arbitrary chosen to define the frequency band of interest which can be estimated from (2b). The circuit has the advantage that all capacitors are in a grounded position and is tunable through the floating resistor R_4. It is also possible to interchange the position of the JFET with C_1 if a grounded nonlinearity is required.

Fig. 2 represents PSpice simulations of the JFET characteristics and a sample of the output waveform obtained with $R_2 = 2K\Omega$, $R_3 = 500\ \Omega$, $R_4 = 1090\ \Omega$, $C_1 = C_3 = 2$ nF, $C_2 = 1$ nF and using the commercial AD844A/AD as a CCII biased with ± 9 V, while Fig. 3 represents the observed phase space trajectories for the same values. It is worth noting that the AD844A/AD is based on a bipolar CCII followed by a buffering stage. Simulations were carried out using the commercial macromodel of this device whereas its transistor level schematic can be found in [20].

The major parasitic element inherent in a CCII device is the small input resistance (R_X) associated with the (X) terminal which is approximately equal to 65Ω for the commercial AD844A/AD. It was found evident that this resistance is responsible for stimulating the chaotic performance of the proposed circuit by allowing for a third- rather than second-order system to exist. The contribution of R_X can be identified from the upper trace in Fig. 3 where the V_{C_2}–V_{C_3} trajectory is plotted. For an ideal CCII, this trajectory would become a straight line since the X terminal voltage should follow that of the Y terminal. The role of parasitic elements has also been reported in [16] and [17], where it was necessary to include the internal voltage op amp dominant pole in the analysis in order to model the chaotic dynamics. However, since the op amp pole represents an extra capacitive effect in the system, some of the circuits in [16], [17] were modeled by a fourth-order system of differential equations, although only three physical capacitors were used. In the case of a CCII this is not possible, and the maximum system order is three. Although R_X is a device parasitic, it is possible to add an extra external resistance in series with R_X and adjust design parameters accordingly.

Including R_X into analysis, the circuit of Fig. 1(a) is described by the following set of equations:

$$\begin{aligned} &C_1\dot{V}_{C_1} = I \\ &\left(1+\frac{R_3}{R_4}\right)R_X C_2\dot{V}_{C_2} \\ &\quad = \left(1-\frac{R_X}{R_2}-\frac{R_X}{R_4}\left(1+\frac{R_3}{R_2}\right)\right)V_{C_2} - \left(1-\frac{R_X}{R_4}\right)V_{C_3} \\ &R_4 C_3\dot{V}_{C_3} \\ &\quad = R_3 C_2\dot{V}_{C_2} - R_4 C_1\dot{V}_{C_1} + \left(1+\frac{R_3}{R_2}+\frac{R_4}{R_X}\right)V_{C_2} \\ &\qquad - \left(1+\frac{R_4}{R_X}\right)V_{C_3} \end{aligned} \tag{5a}$$

where

$$I = \frac{1}{R_J}\begin{cases} V_{C_3}-V_{C_1} & V_{C_3}-V_{C_1} \geq V_T \\ V_T & V_{C_3}-V_{C_1} < V_T. \end{cases} \tag{5b}$$

In order to verify the circuit's chaotic behavior, (5) is transformed into a dimensionless form convenient for numerical simulation.

Setting $X = V_{C_1}/V_T$, $Y = V_{C_2}/V_T$, $Z = V_{C_3}/V_T$, $\alpha = R_2/R_J$, $t_n = t/R_2C_2$ and for the special case of $C_1 = C_3 = 2C$, $C_2 = C$ (5) becomes

$$\begin{aligned} \dot{X} &= \frac{\alpha}{2}\begin{cases} Z-X & Z-X \leq 1 \\ 1 & Z-X > 1 \end{cases} \\ \dot{Y} &= aY - bZ \\ \dot{Z} &= c\dot{Y} - \dot{X} + dY - eZ \end{aligned} \tag{6}$$

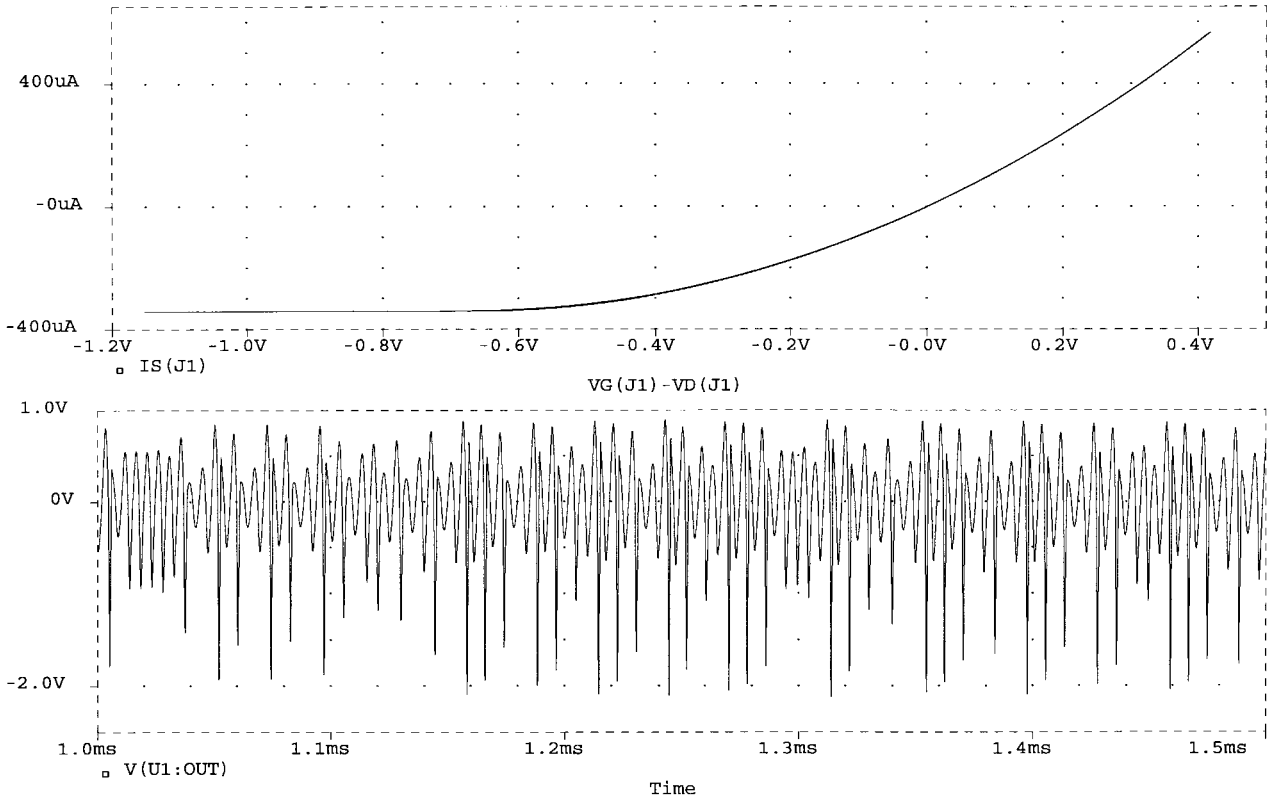


Fig. 2. The JFET characteristics and a sample of the output waveform of the first chaos generator obtained with $R_2 = 2$ KΩ, $R_3 = 500\ \Omega$, $R_4 = 1090\ \Omega$, $C_1 = C_3 = 2$ nF, and $C_2 = 1$ nF.

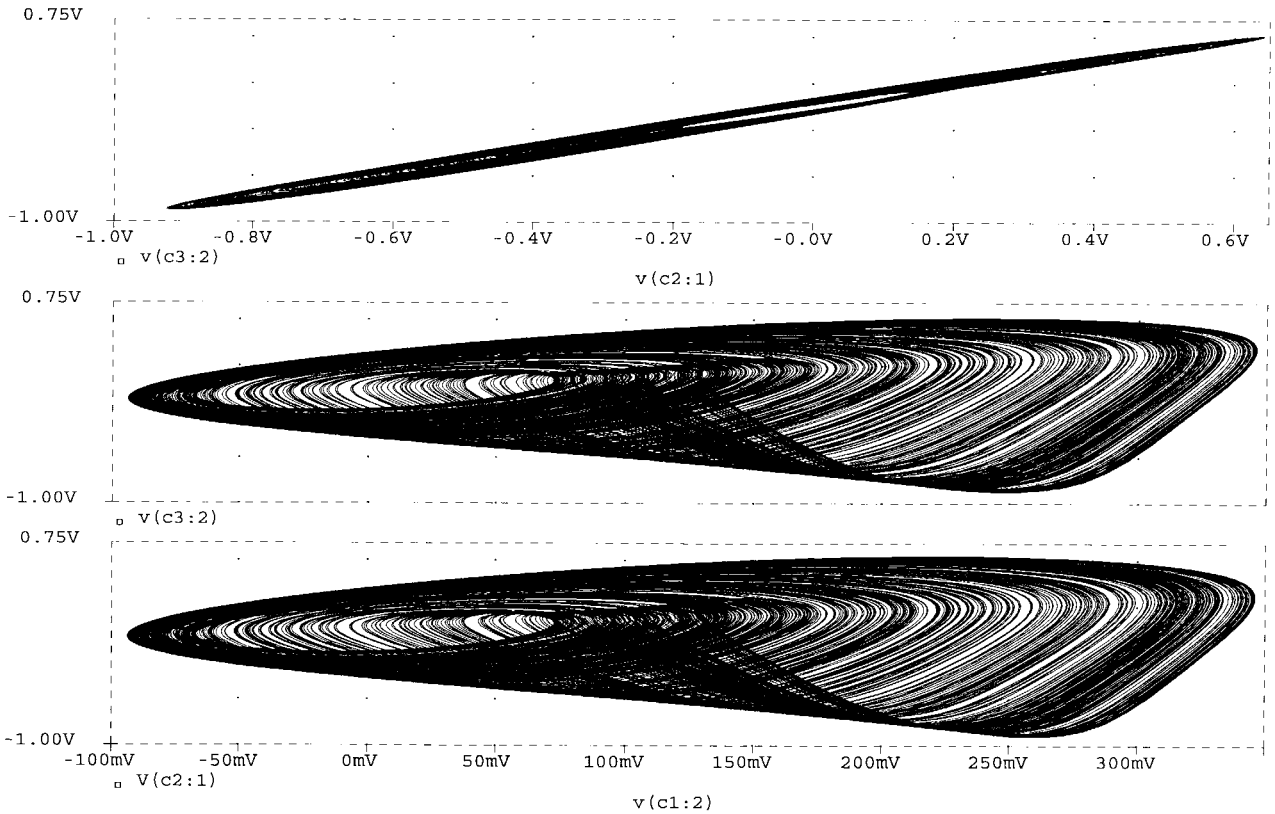


Fig. 3. The observed phase space trajectories of the first chaos generator obtained with $R_2 = 2$ KΩ, $R_3 = 500\ \Omega$, $R_4 = 1090\ \Omega$, $C_1 = C_3 = 2$ nF, and $C_2 = 1$ nF.

where

$$a = \frac{R_4}{R_3+R_4}\left(\frac{R_2}{R_X} - \frac{R_2+R_3}{R_4} - 1\right),$$
$$b = \frac{R_4}{R_3+R_4}\left(\frac{R_2}{R_X} - \frac{R_2}{R_4}\right), \quad c = \frac{R_3}{2R_4},$$
$$d = \frac{R_2}{2R_4}\left(1 + \frac{R_3}{R_2} + \frac{R_4}{R_X}\right), \quad \text{and} \quad e = \frac{1}{2}\left(\frac{R_2}{R_4} + \frac{R_2}{R_X}\right).$$

Numerical integration of (6) was carried out using a Runge–Kutta fourth-order algorithm [21] with a 0.005 step size. The obtained phase space trajectory is shown in Fig. 4(a) given for $\alpha = 2.67$, $a = 18.84$, $b = 20.4$, $c = 0.2$, $d = 16.12$, and $e = 16.3$.

Equation set (6) can be rewritten in the following form:

$$\begin{bmatrix}\dot{X}\\ \dot{Y}\\ \dot{Z}\end{bmatrix} = \begin{bmatrix}-\alpha_1 & 0 & \alpha_1\\ 0 & a & -b\\ \alpha_1 & ac+d & -bc-\alpha_1-e\end{bmatrix} + \begin{bmatrix}\alpha_2\\ 0\\ -\alpha_2\end{bmatrix} \tag{7a}$$

where

$$\begin{cases}\alpha_1 = \dfrac{\alpha}{2}, & \alpha_2 = 0 \quad Z - X \le 1\\ \alpha_1 = 0, & \alpha_2 = \dfrac{\alpha}{2} \quad Z - X > 1.\end{cases} \tag{7b}$$

Hence, the following eigenvalues are calculated for the above parameter values:

$$\begin{cases}-5.4383, \quad 0.61417 \pm j2.2279 & Z - X \le 1\\ 0, \quad -0.77 \pm j4.6 & Z - X > 1.\end{cases}$$

The circuit was experimentally tested taking $C_1 = C_3 = 2$ nF, $C_2 = 1$ nF, $R_2 = 5$ KΩ pot., $R_3 = 500\ \Omega$, R_4 as a 2 KΩ pot and using the AD844 biased with ±9 V. An oscilloscope photograph of the V_{C_1}–V_{C_2} trajectory is shown in Fig. 4(b).

The chaotic behavior of the dynamical system represented by (6) extends to the case where the nonlinearity possesses odd symmetrical characteristics. We demonstrate this behavior since it is possible to realize such nonlinearities as shown in [22] and recently in [23].

With a cubic nonlinearity (6) is modified such that

$$\dot{X} = \beta_1(Z - X) + \beta_2(Z - X)^3. \tag{8}$$

Two cases are demonstrated.

i) $\beta_1 > 0$ and $\beta_2 < 0$. Numerical integration of this case was carried out using a 0.005-step Runge–Kutta fourth-order algorithm with $a = 18.84$, $b = 20.4$, $c = 0.2$, $d = 16.15$, $e = 16.22$, $\beta_1 = 1.8$, and $\beta_2 = -2.7$. Fig. 5(a) and (b) represents the nonlinearity and the trajectory in X–Y–Z space, respectively. As can be seen, this trajectory is formed of two of the trajectories shown in Fig. 4 flipped and merged. This can be verified by restricting operation to either the positive or the negative half of the cubic curve which represent antisymmetric characteristics similar to the JFET characteristics.

ii) $\beta_1 < 0$ and $\beta_2 > 0$. Numerical integration of this case was carried out with the same settings of case i) taking $\beta_1 = -0.78$ and $\beta_2 = 1.17$. The obtained trajectory is plotted in Fig. 5(c) where it can also be seen that it is composed of two of the trajectories of Fig. 4 merged together, one with the same orientation and the other is flipped and mirrored.

III. The Second CCII Chaos Generator

The second CCII chaos generator is shown in Fig. 1(b). Retrieving the sinusoidal oscillator circuit, as explained in Section II, the condition of oscillation for this oscillator is given by

$$R_4 = R_1 + 2R_3\left(\frac{R_1}{R_2} + \frac{C_2}{C_1}\right) \tag{9}$$

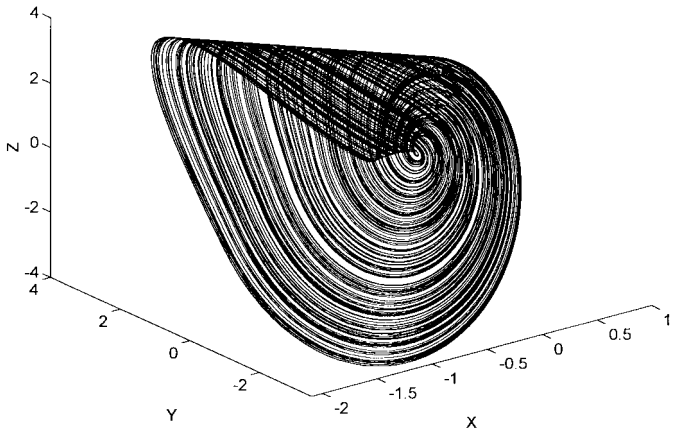
and the radian frequency of oscillation is given by

$$\omega_o = \sqrt{\frac{1 + \dfrac{R_2}{2R_3}}{R_1R_2C_1C_2}}.$$

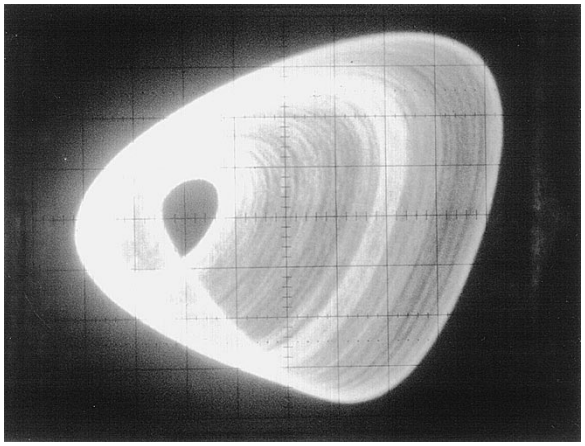
A convenient design set and the corresponding frequency of oscillation are given by

$$R_1 = R_2 = R_3 = R, \quad R_4 = 5R,$$
$$C_1 = C_2 = C \quad \text{and} \quad \omega_o\sqrt{\frac{3}{2}}\frac{1}{RC}. \tag{10}$$

Using the same procedure demonstrated in Section II and adopting the design set of (10), the modified for chaos oscillator is obtained. However, the optimum choice of the capacitors was found to be $C_1 = 0.4C$, $C_2 = C$, and $C_3 = 0.6C$ where C is arbitrarily chosen to define the signal frequency of interest which can be estimated from (10). Results identical to those given in Fig. 3 can be produced with $R_2 = 800\ \Omega$, $R_3 = 700\ \Omega$, $R_4 = 3.47$ KΩ, $C_1 = 4$ nF, $C_2 = 10$ nF, and $C_3 = 6$ nF. The circuit is also tunable by resistor R_4.



(a)



(b)

Fig. 4. (a) Numerical simulation of (6) given for $\alpha = 2.67$, $a = 18.84$, $b = 20.4$, $c = 0.2$, $d = 16.12$, and $e = 16.3$. (b) An experimental V_{C_1}–V_{C_2} trajectory from the first chaos generator.

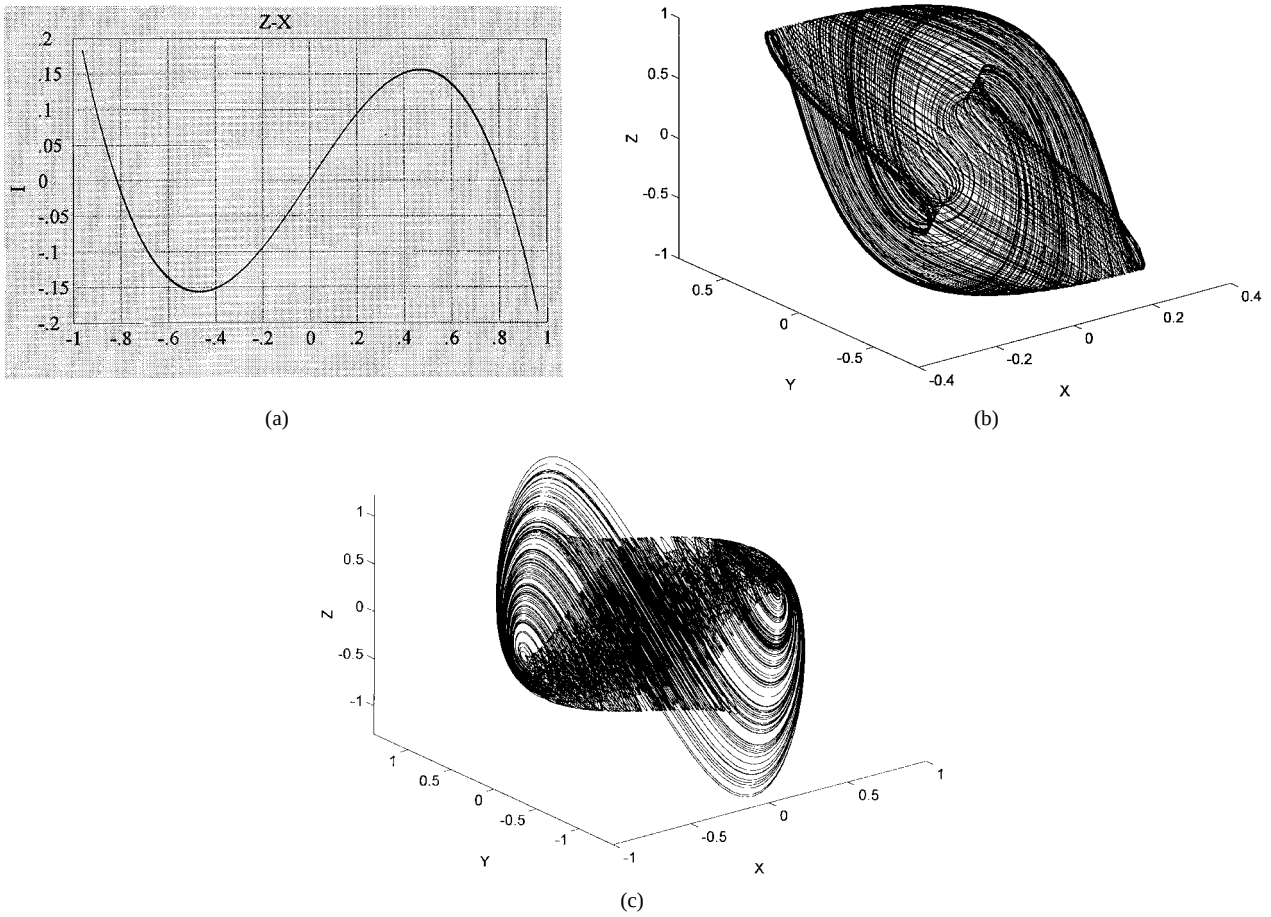


Fig. 5. (a), (b) A cubic nonlinearity and the corresponding trajectory in X–Y–Z space for the case of $\beta_1 > 0$ and $\beta_2 < 0$. (c) Chaotic attractor for a cubic nonlinearity with $\beta_1 < 0$ and $\beta_2 > 0$.

Including the input resistance R_X into analysis, the circuit is described by the following set of equations:

$$\begin{aligned} C_1\dot{V}_{C_1} &= I \\ R_X C_2\dot{V}_{C_2} &= R_X C_1\dot{V}_{C_1} + R_X C_3\dot{V}_{C_3} \\ &\quad - \left(\frac{R_X}{R_2} + \frac{R_4}{R_3+R_4}\right)V_{C_2} + \frac{R_3}{R_3+R_4}V_{C_3} \\ R_2 C_3\dot{V}_{C_3} &= \frac{2R_4 - R_X}{R_4 - R_X}(R_2 C_2\dot{V}_{C_2} + V_{C_2}) \\ &\quad - R_2 C_1\dot{V}_{C_1} + \frac{R_2}{R_4 - R_X}V_{C_3} \end{aligned} \tag{11}$$

where I is as given by (5b).

Setting $X = V_{C_1}/V_T$, $Y = V_{C_2}/V_T$, $Z = V_{C_3}/V_T$, $t_n = t/R_2C_2$, $\alpha = R_2/R_J$, $\varepsilon = C_1/C_2$, $K_1 = R_2/R_X$, $K_2 = R_4/(R_3 + R_4)$, $K_3 = R_4/(R_4 - R_X)$, $K_4 = R_2/(R_4 - R_X)$ and for the special case of $C_1 + C_3 = C_2$, (11) is transformed to the following dimensionless form:

$$\begin{aligned} \dot{X} &= \frac{\alpha}{\varepsilon}\begin{cases} Z - X & Z - X \le 1 \\ 1 & Z - X > 1 \end{cases} \\ \dot{Y} &= \left(\frac{K_1K_2}{K_3} - 1\right)Y - \frac{K_1 + K_4 - K_1K_2}{K_3}Z \\ \dot{Z} &= \frac{1}{1-\varepsilon}\left[\frac{K_1K_2(1+K_3)}{K_3}Y \right. \\ &\quad \left. + \left(K_4 - \frac{(K_1 + K_4 - K_1K_2)(1+K_3)}{K_3}\right)Z - \varepsilon\dot{X}\right]. \end{aligned} \tag{12}$$

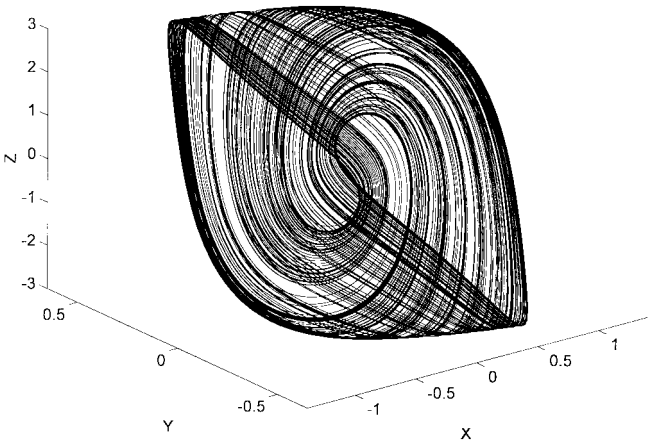


Fig. 6. Chaotic attractor obtained from the second CCII chaos generator by solving (12) and (13).

A chaotic attractor similar to that shown in Fig. 4 is obtained when numerically integrating (12) with $\alpha = 16/15$, $\varepsilon = 0.6$, $K_1 = 160/13$, $K_2 = 0.83$, $K_3 = 1$, and $K_4 = 0.24$.

The following eigen values have also been calculated:

$$\begin{cases} -7.3953, \quad 0.557 \pm j1.95 & Z - X \le 1 \\ 0, \quad -0.9223 \pm j4.0415 & Z - X > 1. \end{cases}$$

The chaotic performance of the system also extends to the case of odd symmetrical nonlinearities displaying similar results to those of the first oscillator circuit.

It is worth noting that a nonlinearity in the form of a sinusoidal function can also lead to chaotic behavior, in this case (12) is modified such that

$$\dot{X} = \frac{\alpha}{\varepsilon} \sin(Z - X). \tag{13}$$

Fig. 6 represents the trajectory for this case with $\alpha = 273/250$ and the rest of the constants as above.

IV. Suitability for VLSI Implementation

The proposed chaotic oscillators can be directly implemented in VLSI. In particular, a CMOS implementation can benefit from the CCII realizations of [10] which operate from a supply voltage as low as 1.1 V. Analysis of the chaotic behavior revealed the important role of the CCII input resistance R_X, which can be well controlled over a wide frequency range in CMOS implementations. In addition, floating and grounded voltage-controlled CMOS resistors can be realized [24]–[26]. With the appropriate combination of linear CMOS resistors and the MOS negative resistors of [27], nonlinear resistors of antisymmetric as well as symmetric characteristics can be implemented. It is worth noting that the chaotic oscillator of Fig. 1(a) is especially attractive for VLSI implementation, since all capacitors are grounded.

V. Conclusion

Simple RC chaos generators that utilize the CCII as the active building block have been introduced. The sequence of obtaining these generators from sinusoidal oscillators has been clarified. Chaotic behavior with nonlinearities of antisymmetric as well as odd symmetric characteristics was investigated. Suitability for VLSI integration has also been discussed.

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