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New CMOS Realization of the CCII−

I. A. Awad and A. M. Soliman

***Abstract*—New second-generation current conveyor negative (CCII−) realization suitable for very large scale implementation is described. The proposed architecture provides a very low impedance level at the X terminal and a wide dynamic voltage range, as well as a high current tracking accuracy. Simulations show that the CCII− current follower bandwidth extends beyond 100 MHz. Two compensation methods are discussed: the first results in voltage-offset cancellation, while the second results in voltage-offset compensation as well as Rx reduction.**

***Index Terms*—CMOS current conveyors.**

I. INTRODUCTION

The second-generation current conveyor (CCII) proposed by Sedra and Smith in [1] has proven to be a useful building block for high-frequency current mode applications. Recently, a great deal of attention has been directed toward designing high-performance current conveyors in terms of gain accuracy, impedance level, voltage, current offset, as well as bandwidth, and many CCII's for CMOS technologies have been reported [2]–[7]. Basically, the CCII is described as a combined voltage and current follower. The most straightforward implementation of this current follower in the case of the CCII+ is a simple current mirror, while two cross-coupled current mirrors are used in the case of the CCII−. These CCII− configurations suffer from the limitations imposed by the frequency response and mismatch of the transistor mirrors. A solution to the above problem has been suggested in [8], making use of a class A cascode stage called "floating current source" (FCS). This stage exhibits a high current tracking accuracy if complete isolation of the cell is provided and matched upper and lower current sources is used. In this brief, a novel CCII− realization is proposed. Low current tracking error is achieved by using the above-mentioned FCS stage to implement the current buffer between the X and the Z terminals. The voltage offset due to the channel-length modulation is discussed, and two compensation circuits are then developed. The first compensation circuit results in a DC-offset cancellation between the Y and the X terminals, while the second compensation circuit provides a voltage-offset cancellation independent of the level of the input current at the X terminal, hence reducing the resistance seen at the same terminal to a very small value.

II. THE PROPOSED CCII− REALIZATION

Fig. 1 shows the CMOS realization of the proposed class A CCII−. The input stage is implemented using a simple differential amplifier $(M1$–$M5)$, while the output stage is implemented using the class A FCS stage $(M6$–$M13)$. The voltage buffering is provided using negative feedback. This two-gain stage configuration allows independent control of the CCII− voltage-following and current-following dynamic ranges. Moreover, the use of two cascaded gain stages results in a very small impedance level at the input of the CCII−, as well as voltage and current gains very close to unity.

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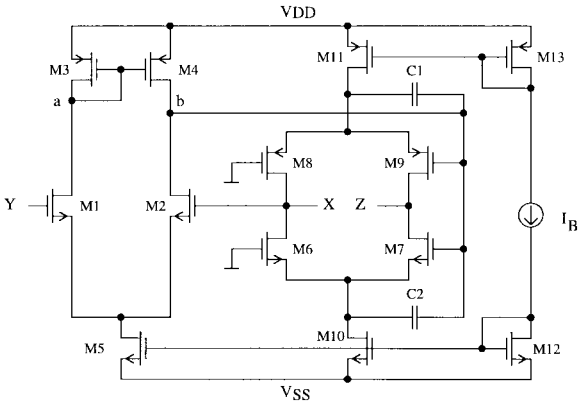

Fig. 1. The proposed CCII− CMOS realization.

Assuming that each of the following pairs $M1$–$M2$, $M3$–$M4$, $M6$–$M7$, and $M8$–$M9$ consists of two matched transistors, the low-frequency voltage transfer gain between nodes Y and X is given by

$$A_v = \frac{v_X}{v_Y} = \frac{1}{1 + \dfrac{(g_{d2} + g_{d4})(g_{d6} + g_{d8})}{g_{m2}(g_{m6} + g_{m8})}} \tag{1}$$

where g_{di} is the output conductance and g_{mi} is the transconductance with respect to V_{gsi} of the ith transistor, respectively.

As given by (1), the voltage transfer gain between the Y and the X terminal depends on the transconductance and the output impedance of both the input transconductor and the FCS output stage. Since the output conductance of a transistor can be made negligible with respect to its transconductance, the voltage gain of the proposed CCII− given by (1) can be made very close to unity.

The small signal input resistance seen at node X is given by

$$r_X = \frac{2(g_{d2} + g_{d4})}{g_{m2}(g_{m6} + g_{m8})} \left\| \left(\frac{2}{g_{d6} + g_{d8}} \right). \right. \tag{2}$$

The proposed CCII− operates in class A and the maximum input current to the X terminal is limited by the FCS biasing current I_B. The power consumption of the circuit is dependent on the level of I_B and the supply voltages according to the following equation:

$$P_{\rm SB} = 3I_{\rm B}(V_{\rm DD} - V_{\rm SS}). \tag{3}$$

The low-frequency current transfer gain between the X and Z nodes is given by

$$A_i = \frac{i_Z}{i_X} \approx -\frac{1 + \dfrac{g_{d10} + g_{d11}}{2(g_{m6} + g_{m8})}}{1 - \dfrac{g_{d10} + g_{d11}}{2(g_{m6} + g_{m8})}}. \tag{4}$$

As given by (4), the low-frequency current gain is very close to unity. The frequency response results in a peak in both the magnitude and the phase of the output current at high frequency. In order to eliminate that peak, two compensation capacitors (C_1 and C_2) are added between the gates and the sources of $M7$ and $M9$.

III. Compensation Methods

In the previous analysis, the voltage difference between the X and the Y terminals is assumed to be dependent only on the level of the current I_X. However, there exists another DC voltage offset resulting from the current transfer error of the simple current mirror formed by $M3$ and $M4$. This offset is mainly due to the channel-length modulation effect and is given by

$$\Delta V = V_X - V_Y \approx [\lambda(V_a - V_b)]\sqrt{\frac{I_B}{2K_1}} \tag{5}$$

where λ is the channel-length modulation parameter, and V_a and V_b are the voltages at the drains of $M1$ and $M2$, respectively.

In the uncompensated circuit of Fig. 1, V_b is held at a virtual ground for small values of I_X due to the relatively high transconsductance gain of the FCS stage. On the other hand, V_a is equal to the gate voltage of transistor $M4$, which is close to $V_{DD} - |V_{Tp}|$. This large difference between V_a and V_b results in a significant offset between V_X and V_Y, even for small values of I_X.

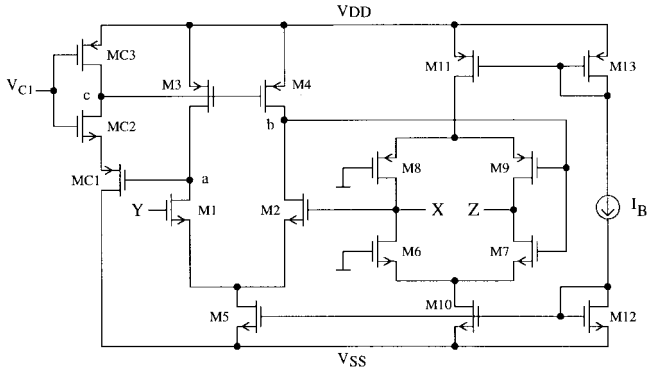

Fig. 2. The first compensated CCII−.

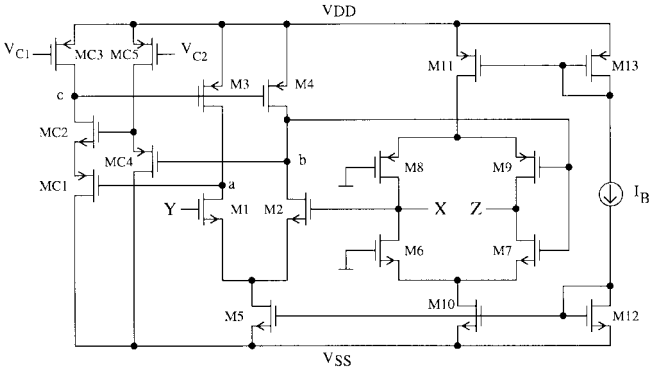

Fig. 3. The second compensated CCII−.

A. First Compensated Circuit

In order to minimize the voltage offset, V_a must be small and very close to V_b, which is approximately equal to zero for low values of I_X. This is achieved by replacing the unity-gain feedback between the gate and the drain of $M3$ by a relatively high-gain feedback circuit, as shown in Fig. 2. For proper operation, the bias voltage V_{C1} must be adjusted to make V_a equal to zero as follows:

$$V_{C_1} = \frac{\sqrt{K_{c3}}(V_{DD} - |V_{Tp}|) + \sqrt{K_{\rm eff}}\,V_{\rm eff}}{\sqrt{K_{c3}} + \sqrt{K_{\rm eff}}} \tag{6}$$

where

$$K_{\rm eff} = \frac{\sqrt{K_{c1}}\,\sqrt{K_{c2}}}{\sqrt{K_{c1}} + \sqrt{K_{c2}}} \tag{7}$$

and

$$V_{\rm eff} = V_{Tn} + |V_{Tp}|. \tag{8}$$

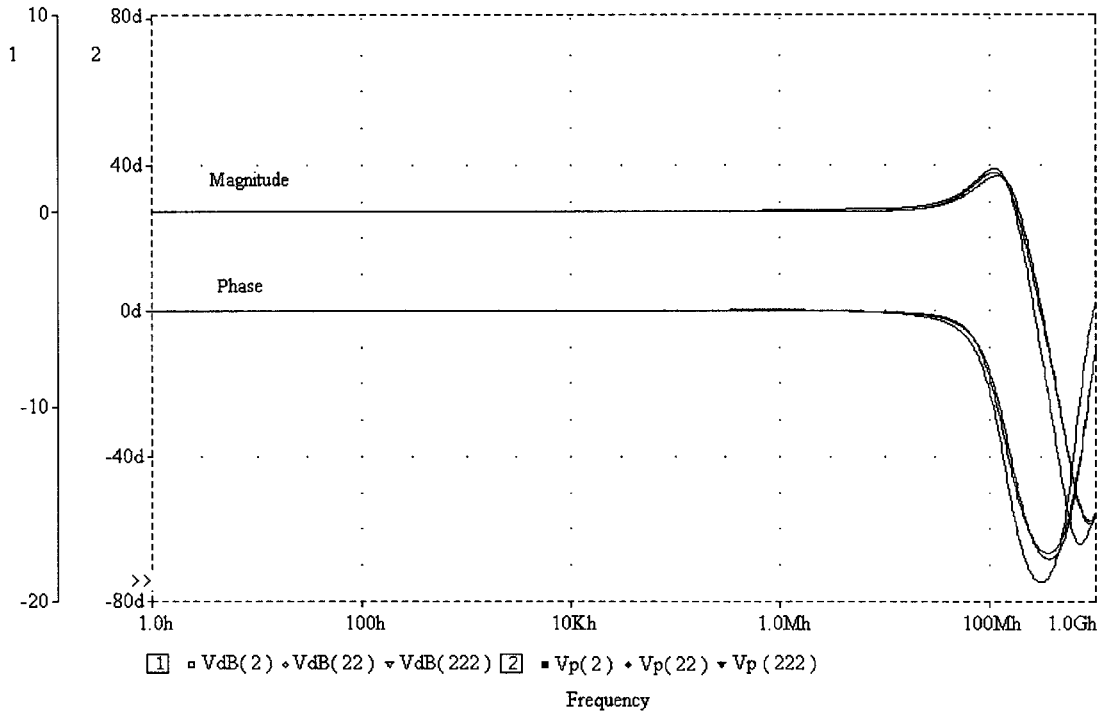

Fig. 4. The open-circuit AC transfer characteristics between the Y and the X terminals of the three CCII− circuits.

TABLE I
TRANSISTORS ASPECTS RATIOS . (a) PROPOSED CCII−. (b) FIRST MODIFICATION CIRCUIT. (c) SECOND MODIFICATION CIRCUIT

Transistors	W(μm) / L(μm)
M1,M2	3/3.6
M3,M4	90/3.6
M6,M7	60/1.2
M8,M9	120/1.2
M5,M10,M12	30/3.6
M11,M13	90/3.6

(a)

Transistors	W(μm) / L(μm)
MC1	90/3.6
MC2	60/3.6
MC3	6.6/3.6

(b)

Transistors	W(μm) / L(μm)
MC1,MC2	30/3.6
MC3	1.2/3.6
MC4,MC5	90/9.6

(c)

TABLE II
SIMULATIONS RESULTS OF THE THREE CCII− CIRCUITS

Parameter	unit	The proposed CCII-	The first compensated CCII-	The second compensated CCII-
Input voltage dynamic range (at $I_X = 0$)	Volt	-2.5 to 2.92	-2.5 to 0.9	-3 to 2
A_v (average value)	-	0.9994	0.9994	1
Max. deviation from A_v	-	1.8 %	1 %	0.05%
offset voltage variation (in the linear range)	mV	0.4 to 37	-0.9 to 15	0.009 to 0.27
f_{3db} of open circuit voltage transfer gain	MHz	256	245	222
R_x (average value)	Ω	26	26	0.003
Input current range	μA	±100	±100	±100
offset current variation	μA	-0.3 to 0.2	-0.3 to 0.2	-0.3 to 0.2
A_i (average value)	-	1.0015	1.0015	1.0015
Max. deviation from A_i	-	4.7 %	4.7 %	4.7 %
f_{3db} of short circuit current transfer gain	MHz	104	108	110

B. Second Compensated Circuit

Although the first compensation technique results in a small voltage offset, the level of R_X is unaffected by this compensation. This is mainly due to making V_a constant and independent of V_b. When I_X is changed, V_b is changed according to the transconductance of the FCS stage, resulting in an offset voltage between V_X and V_Y. A solution to this problem is to make V_a equal to V_b for any value of I_X. This is achieved by making the voltage at the gate of $M3$ (V_c) equal to the difference between V_a and V_b, multiplied by a very large gain. Hence, when V_c is set to a finite value, the difference between V_a and V_b will be approximately equal to zero and independent of I_X. The second compensated CCII− circuit is shown in Fig. 3. For proper operation, V_{c1} and V_{c2} must be chosen so that V_a is equal to V_b and according to the following equation:

$$\sqrt{K_{c3}}V_{C_1} - \sqrt{K_{\text{eff}}}V_{C_2} = \sqrt{K_{c3}}(V_{\text{DD}} - |V_{Tp}|) - \sqrt{K_{\text{eff}}}(V_{\text{DD}} - V_{\text{eff}}). \quad (9)$$

IV. SIMULATIONS RESULTS

PSPICE simulations were carried out with model parameters of 1.2-μm CMOS process provided by MOSIS (AMI). The supply voltages were equal to ±3.3 V and the bias current was set to 100 μA. The transistors aspect ratios of the proposed CCII− and the two modification circuits are given in Table I. Simulation results are given in Table II. A current transfer gain very close to unity was

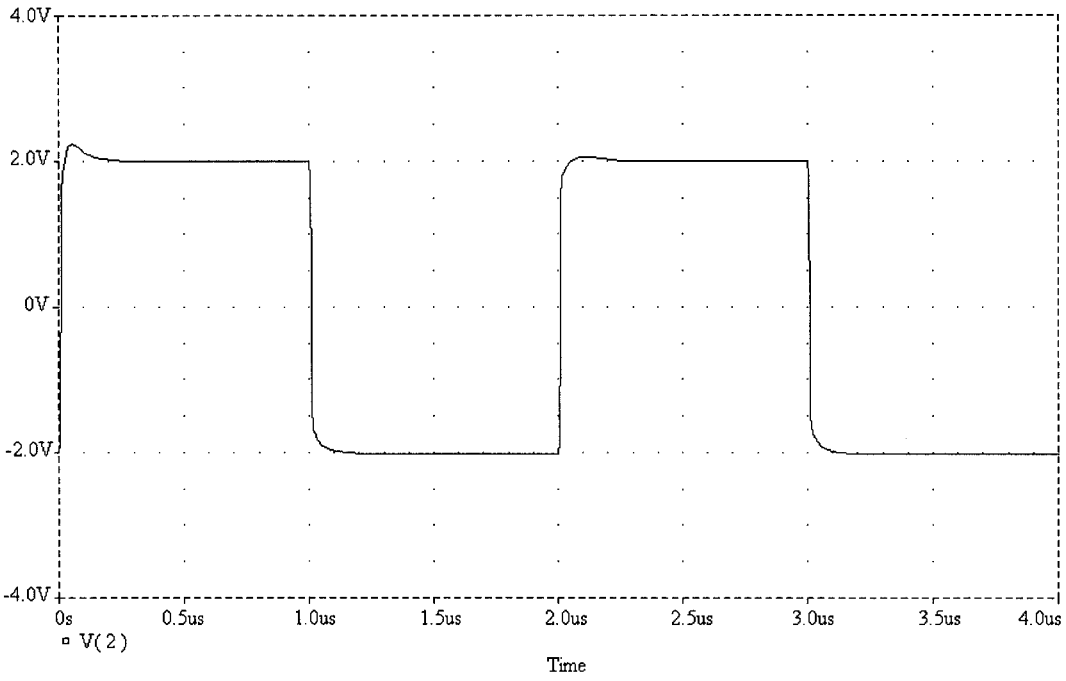

Fig. 5. The transient response of second proposed CCII−.

obtained in accordance with (3). The offset current variation was from -0.3 to 0.2 μA over a range of ± 100-μA input current. This offset is mainly due the channel-length modulation effect on the current mirrors $(M10$–$M12)$ and $(M11$–$M13)$. The short-circuit frequency response between the X and the Z terminal showed a 3-dB frequency of 104 MHz when C_1 and C_2 were equal to 1 pF.

In the first compensated CCII−, V_{c1} was set to 1.71 V, resulting in a voltage-offset cancellation over a limited range, and the same R_X of the unmodified CCII− (26 Ω). In the case of the second compensated circuit, V_{c1} and V_{c2} were set to 1.6 and 1.75 V, respectively. The offset voltage variation was between 13 – 171 μV over the input range (-3 – 2 V). An enhancement in the voltage-following gain and a reduction of the R_X value to 3 mΩ were also obtained.

Fig. 4 shows the open-circuit frequency response between the X and the Y terminals in the case of the three CCII− circuits. A 2-pF capacitor was added between the gate and the drain of $M3$ of the second compensated circuit in order to minimize the peak existing in the magnitude response. The stability of the second compensated CCII− voltage follower is verified by simulating the transient response to a ± 2-V input step of 1-ns rise time, and the corresponding result is shown in Fig. 5.

V. Conclusion

New CCII− CMOS realization was presented. The proposed architecture profits from the high-current tracking accuracy of the FCS output stage in order to realize the CCII− current follower. On the other hand, a simple input stage was used and resulted in a high dynamic input range between the Y and the X terminals. The voltage offset between the Y and the X terminals was evaluated by taking the channel-length modulation effect into consideration. The compensation of this voltage offset was discussed and modified CCII− realizations were presented. The second compensated circuit results in a significant reduction in the input impedance, seen at the X terminal. Simulation results were included to illustrate the high performance of the proposed design.

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