Square root domain differentiator

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Abstract: A square root domain differentiator is proposed based roughly on the concept of gyrators in linear filters. The differentiator is evaluated independently and a method for its inclusion in larger filters is proposed. The differentiator is used to design a third–order lowpass elliptic filter as an example of filters with finite zeros.

1 Introduction

Square root domain filters are a family of externally linear internally non-linear (ELIN) filters. Square root domain filters enjoy a number of advantages including an excellent linearity–bandwidth compromise as well as tunable operation [1, 2]. Yet square root domain circuits suffer from sever limits on design and on filters that can be implemented.

One such impediment to complete freedom in the implementation of square root domain filters is the lack of a square root domain differentiator. This translates into a limit on the number of ways that filters with finite zeroes can be realised. Although such filters can be realised by signal subtraction and addition, this still limits the design choices and may lead to inaccurate results in large circuits [3, 4]. The same problem is also encountered in log-domain filters and manifests itself in the absence of good log-domain elliptic filters. Elliptic filters are important examples of functions with finite zeroes. Therefore many attempts were made to realise such filters, either empirically [3], or by signal subtraction [4]. No attempts were made to realise elliptic square root domain filters. A log-domain highpass filter was designed by Frey in [5] but a standalone differentiator was not reported.

2 Square root domain differentiator

In a linear filter (e.g. G_m-C), differentiators may be realised by using gyrators (positive impedance inverters). A gyrator is employed in differentiation by inverting the impedance of the integrating capacitor. This leads to an inductive impedance being seen, which transforms the integrator into a differentiator [5]. For the case of G_m-C, the differentiator may be realised as in Fig. 1. The back-to-back transconductor pair preceding the capacitor perform the gyration function.

$$I_1 = G_m V_{in} = G_m V_C \tag{1}$$

$$I_2 = G_m V_1 = C\dot{V}_C \tag{2}$$

Differentiating (1) and substituting (2):

$$G_m \dot{V}_{in} = \frac{G_m^2}{C} V_1 \tag{3}$$

$$V_1 = \frac{C}{G_m} \dot{V}_{in} \tag{4}$$

This result can also be deduced by viewing the gyrator alone as performing the following impedance inversion:

$$Z_{in} = \frac{1}{G_m^2 Z_L} \tag{5}$$

So if Z_L is a capacitor, then the input impedance seen is an inductor L whose value is $\frac{C}{G_m^2}$, therefore:

$$V_1 = LG_m \dot{V}_{in} = \frac{C}{G_m} \dot{V}_{in}$$

This result may suggest (falsely) that a gyrator can be used in square root domain filters since it can simply be considered an impedance inverter. But the fact is that simple linear inversion will not work with square root domain filters. Square root domain filters are internally non-linear, this non-linearity will not allow simple gyrators to perform their intended function.

From Fig. 2 (where 'square root transconductor' denotes a cascade of squarer divider and geometric mean cells):

$$I_{in}\sqrt{\frac{I_A}{I_1}} = G_m V_C \tag{6}$$

Equation (2) still applies. The effect of non-linearity is clear in (6), differentiating the equation will be an arduous task due to the presence of $\sqrt{I_1}$, moreover it will not yield an overall linear differentiation between I_{in} and I_1.

A true square root domain differentiator will thus have to comply with the non-linearities inherent to the filter core; namely, the $\sqrt{I_1}$ in the denominator of (6) has to be dealt with. A good attempt for the differentiator would be to replace the linear transconductors in Fig. 2 with square root domain transconductors, thus leading to Fig. 3.

Defining I_1 and I_2 as:

$$I_1 = \frac{K_1}{2} V_1^2 \tag{7}$$

$$I_2 = \frac{K_2}{2} V_C^2 \tag{8}$$

$$I_{in}\sqrt{\frac{I_A}{I_1}} = I_2\sqrt{\frac{I_B}{I_1}} \tag{9}$$

$$I_{in}\sqrt{I_A} = I_2\sqrt{I_B} \tag{10}$$

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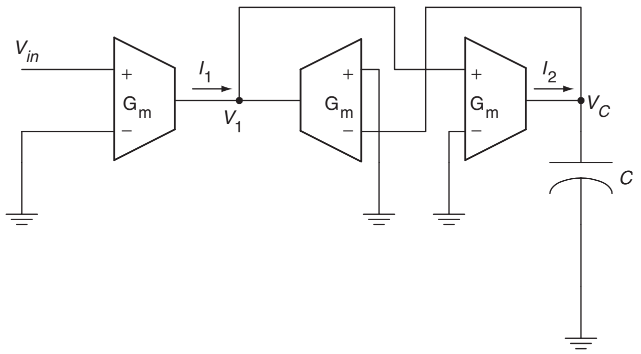

Fig. 1 *Gyrators in G_m-C filters*

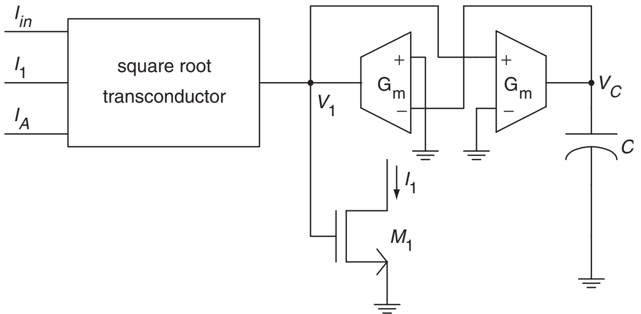

Fig. 2 *Attempt to use gyrators in square root domain filters*

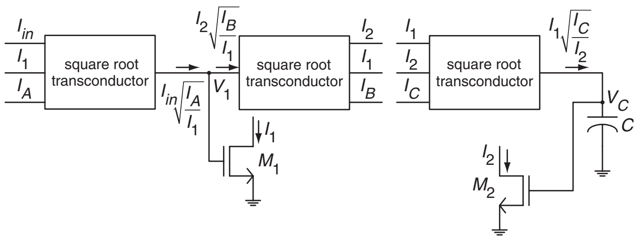

Fig. 3 *Square root domain differentiator*

$$I_1\sqrt{\frac{I_C}{I_2}} = C\dot{V}_C \tag{11}$$

From (8) and substituting in (11):

$$I_1 = \frac{C}{\sqrt{2K_2I_C}}\dot{I}_2 \tag{12}$$

Differentiating (10):

$$\dot{I}_{in}\sqrt{I_A} = \dot{I}_2\sqrt{I_B}$$

And from (12):

$$I_1 = \dot{I}_{in}C\sqrt{\frac{I_A}{2K_2I_BI_C}} \tag{13}$$

Therefore linear differentiation is indeed realised between the input and output terminals.

Proper operation of the differentiator necessitates the use of accurate building blocks. Early simulations showed that channel length modulation in particular can be detrimental to proper operation. Thus the geometric mean cell from [1] based on a stacked topology was slightly modified through M_7 which cascodes the output transistor, thus immunising it from channel length modulation, and also M_5 which reduces channel length modulation on M_4. The modified cell is shown in Fig. 4. The squarer divider used was adapted from the geometric mean cell, with the output exchanged with one of the inputs. The circuit is shown in Fig. 5.

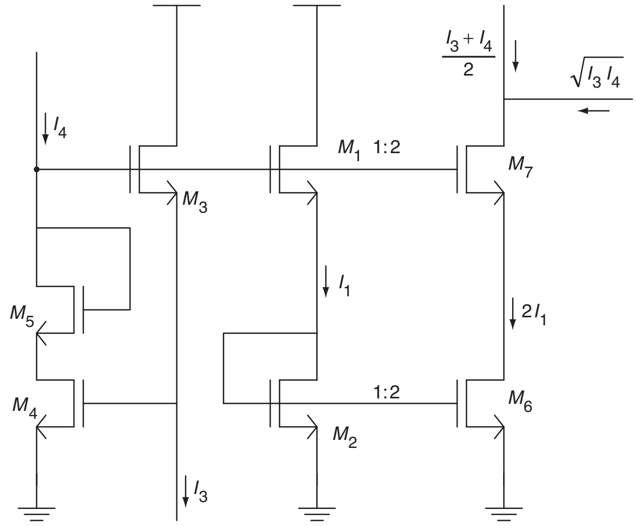

Fig. 4 *Modified geometric mean*

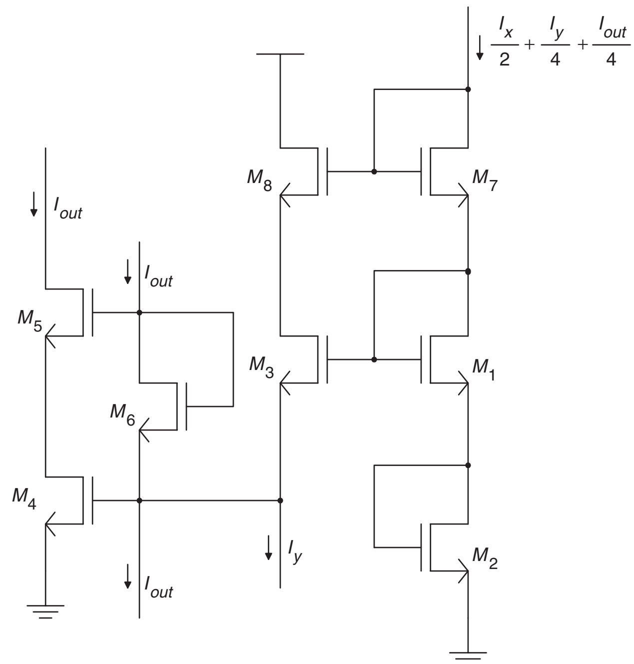

Fig. 5 *Squarer divider*

The response of the differentiator in the range of interest is shown in Fig. 6. The response on a wider scale is shown in Fig. 7. The peak seen at high frequency and the drop seen from thereon can be directly attributed to the presence of parasitic poles. This is inevitable, so when designing one must take into consideration this upper limit on validity. Even more crucial is the slight flattening seen at low frequency. This somehow mysterious flattening is compounded (and explained) if the differentiator is implemented using unmodified building blocks. The differentiator is a very sensitive circuit where building blocks can be benchmarked, Fig. 8 shows the result for a differentiator using the building blocks from [1]. Clearly the flat area of the response is more pronounced in this case, the effect is that the differentiator is valid only over slightly more than a decade. Since the only difference between this circuit and the one implemented using the modified building blocks is

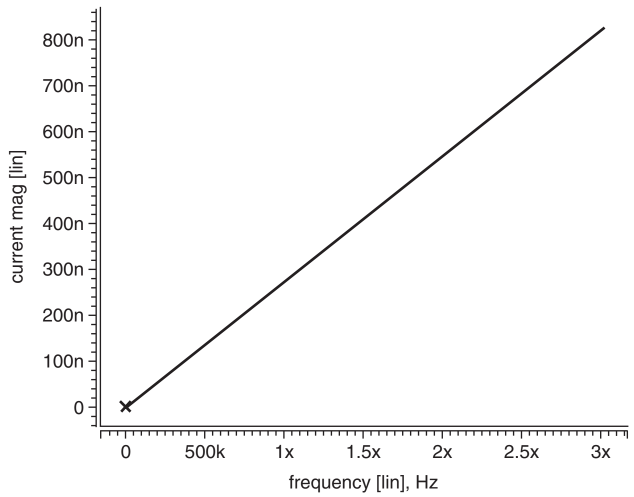

Fig. 6 *Differentiator magnitude response*

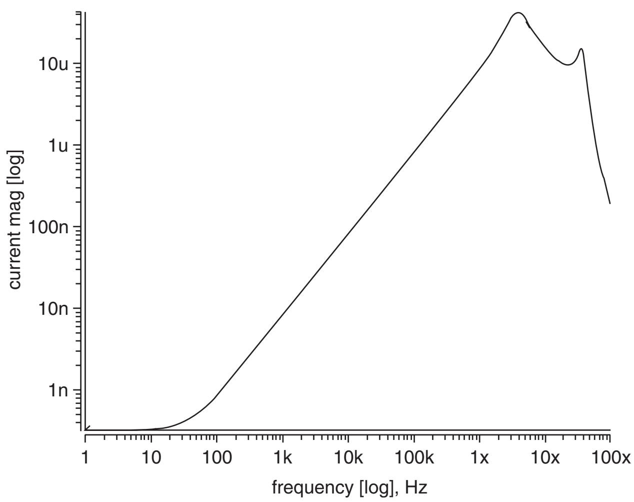

Fig. 7 *Differentiator magnitude response on a large frequency scale*

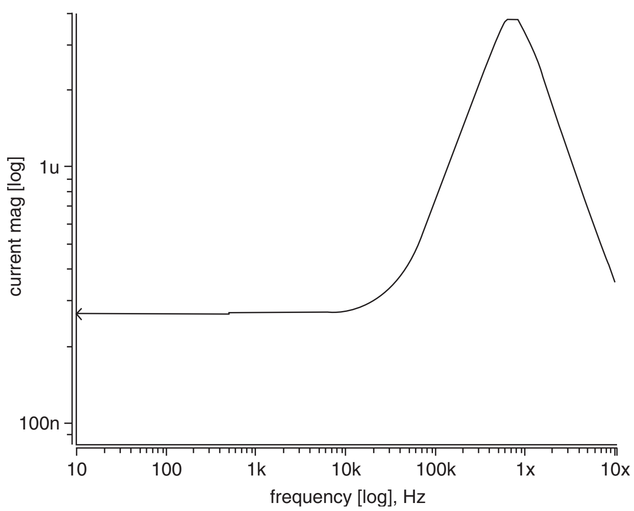

Fig. 8 *Differentiator magnitude response with unmodified building blocks*

that the latter is free from channel length modulation, then this secondary effect has to be responsible for the degradation in behaviour. Therefore the differentiator is realistically modeled by the passive circuit in Fig. 9. Simulation shows that this circuit has identical behaviour (in terms of shape) to the actual differentiator. The parallel capacitance C models parasitic capacitance and limits the maximum frequency at which the circuit can operate. The series resistance R models channel length modulation and essentially represents finite coil quality factor. This resistance degrades differentiator behaviour at low frequency and manifests itself in various ways depending on the circuit being considered.

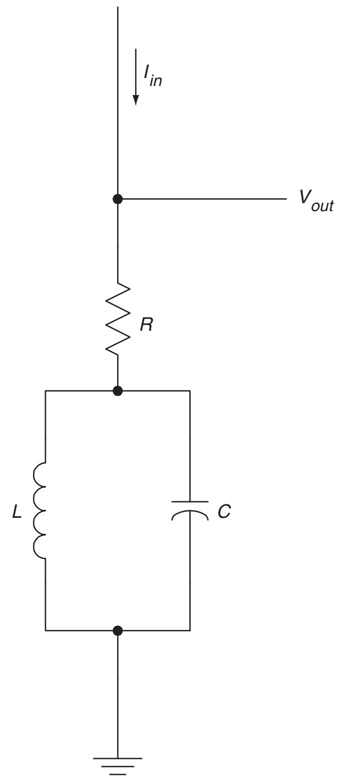

Fig. 9 *Passive model of the differentiator*

3 Differentiators in filters

Behaviour of the differentiator as part of a larger circuit can be tested by applying it to a circuit with finite zeroes. The simplest example is a first-order highpass filter. One way to realise a highpass filter is to replace the capacitor in a traditional first-order lowpass square root domain filter by an effective inductor. This is equivalent to inserting the two square root transconductors performing the non-linear inversion suggested earlier before the capacitor. This yields the circuit in Fig. 10.

Equation (12) applies. For the V_1 node:

$$I_{in}\sqrt{\frac{I_A}{I_1}} - \sqrt{I_1 I_D} = I_2\sqrt{\frac{I_B}{I_1}} \qquad (14)$$

$$I_{in}\sqrt{I_A} - I_1\sqrt{I_D} = I_2\sqrt{I_B} \qquad (15)$$

Differentiating (15):

$$\dot{I}_{in}\sqrt{I_A} - \dot{I}_1\sqrt{I_D} = \dot{I}_2\sqrt{I_B} \qquad (16)$$

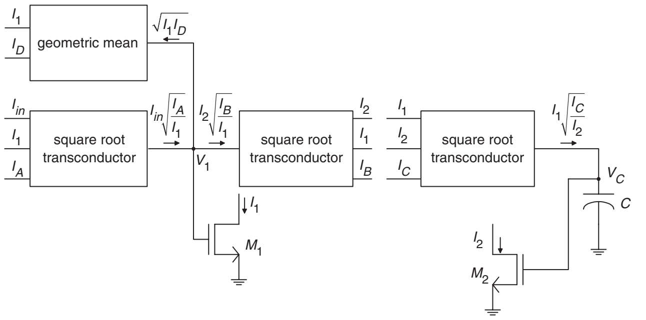

Fig. 10 *First-order highpass filter*

And substituting in (16) from (12):

$$\dot{I}_{in}\sqrt{I_A} - \dot{I}_1\sqrt{I_D} = \frac{\sqrt{2K_2 I_B I_C}}{C} I_1 \qquad (17)$$

This gives the transfer function:

$$\frac{I_1}{I_{in}} = \frac{s\sqrt{\dfrac{I_A}{I_D}}}{s + \dfrac{1}{C}\sqrt{\dfrac{2K_2 I_B I_C}{I_D}}} \qquad (18)$$

Simulation results for this filter are shown in Fig. 11; the filter has a cutoff frequency of 38.9 kHz for a designed cutoff of 40 kHz. Although the filter represents a fairly accurate representation of a highpass filter at low frequency it starts rolling off above 10 MHz due to the parasitic pole.

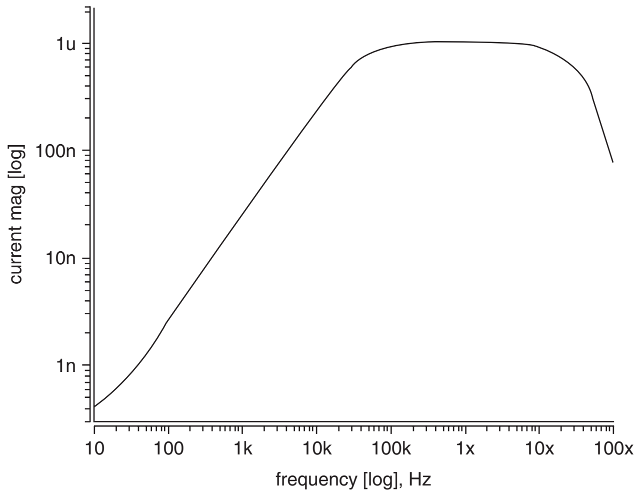

Fig. 11 *Highpass magnitude response*

If the filter was implemented using unmodified building blocks the effect would have been a decrease in loss at low frequency. This manifests itself by a constant component (not DC but constant) passing for a considerable band below cutoff. The method used to convert the LPF into an HPF may have been intuitive but a more systematic approach is needed if differentiators are to be part of larger circuits.

To propose such an approach, a particular case will be considered. The following equation represents a fairly general case, and results can be adopted in almost all cases:

$$\dot{I}_1 = AI_3 - BI_1 + D\dot{I}_{in} \qquad (19)$$

I_1 is the current being evaluated by this filter fragment, that is to say it is the result of the integration. I_3 is a normal current input, it will be integrated as part of the process of obtaining I_1. I_{in} is the differentiated input.

One way in which equation (19) can be applied is to consider the process of differentiating I_{in} an independent step. So the result of differentiation will be used as a new input current to the block performing (19). This outlook leads to the implementation in Fig. 12. The result of differentiating I_{in} (which is clearly implemented independently) is called I_{ind} and is used as a new input current.

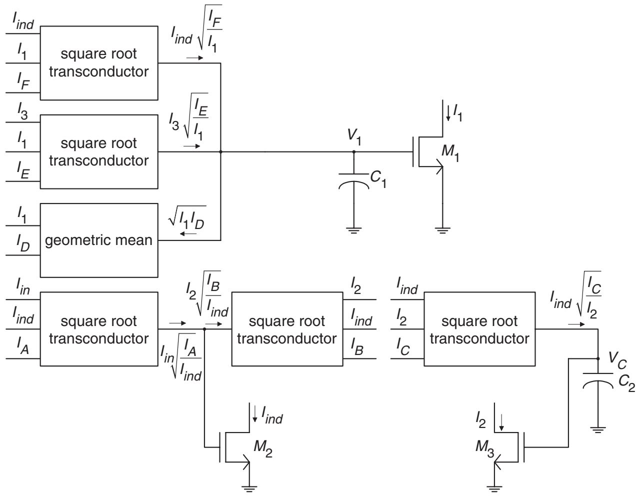

Fig. 12 *Differentiators in filters – method 1*

Verifying that this circuit performs (19) is simple. First I_{ind} can be related to I_{in} through

$$I_{ind} = \dot{I}_{in} C_2 \sqrt{\frac{I_A}{2K_3 I_B I_C}} \qquad (20)$$

And by performing KCL at V_1:

$$I_3\sqrt{I_E} + I_{ind}\sqrt{I_F} = I_1\sqrt{I_D} + \frac{C_1}{\sqrt{2K_1}}\dot{I}_1 \qquad (21)$$

And substituting from (20) in (21), the equation resembles (19) and the implementation is verified.

The highpass filter raises an important question about the uniqueness of the method used above to include differentiators. The highpass filter is a special case of (19) with I_3 equal to zero. The filter in Fig. 10 was implemented using a single capacitor that performed both the differentiation and integration processes. Therefore there must be an alternative way to implement (19). Further consideration leads to the conclusion that Fig. 13 represents that alternative implementation.

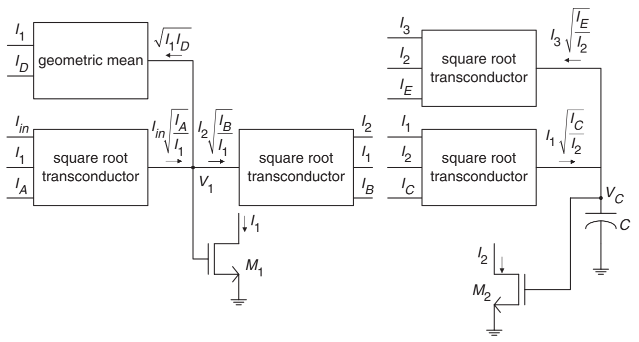

Fig. 13 *Differentiators in filters – method 2*

Verification is again simple. Writing KCL equations at V_1 and V_C:

$$I_{in}\sqrt{I_A} = I_1\sqrt{I_D} + I_2\sqrt{I_B} \tag{22}$$

$$I_1\sqrt{I_C} = I_3\sqrt{I_E} + \frac{C}{\sqrt{2K_2}}\dot{I}_2 \tag{23}$$

Differentiating (22) and substituting for $\dot{I}_2$ from (23) leads to:

$$\dot{I}_1 = \frac{I_3}{C}\sqrt{\frac{2K_2 I_B I_E}{I_D}} - \frac{I_1}{C}\sqrt{\frac{2K_2 I_B I_C}{I_D}} + \dot{I}_{in}\sqrt{\frac{I_A}{I_D}} \tag{24}$$

Which again resembles (19).

4 Design example: third-order elliptic filter

A design that has always been challenging in the log domain is elliptic filters. Due to the absence of log-domain differentiators, designers have always resorted to approximations or signal subtraction to solve this problem [3, 4]. With a square root domain differentiator at hand it is interesting to see how challenging the design will be, and how closely the results will follow the ideal case.

To simplify design equations, a third-order lowpass elliptic filter is considered, having the passive structure shown in Fig. 14. The state equations for this filter are

$$L\dot{I} = V_1 - V_2 \tag{25}$$

$$C_1\dot{V}_1 = \frac{V_{in} - V_1}{R_S} - I - C_2(\dot{V}_1 - \dot{V}_2) \tag{26}$$

$$C_3\dot{V}_2 = I + C_2(\dot{V}_1 - \dot{V}_2) - \frac{V_2}{R_L} \tag{27}$$

The SFG for this passive filter is shown in Fig. 15.

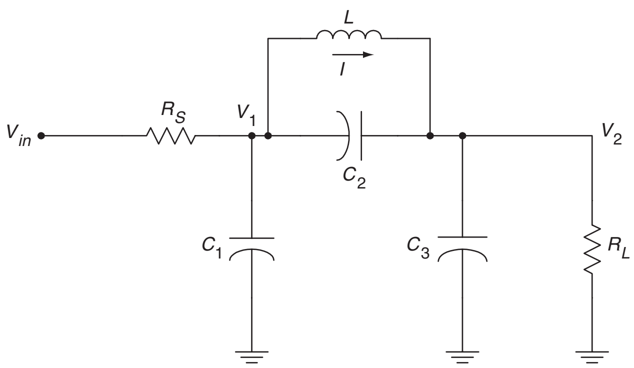

Fig. 14 *Passive third-order elliptic filter*

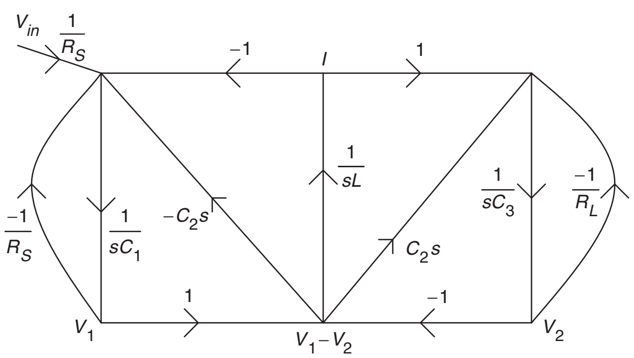

Fig. 15 *Signal flow graph of the elliptic filter*

To deduce the square root domain counterpart of this passive filter, (25), (26) and (27) must be transformed so that all variables are either currents or voltages. Let

$$V_1 = I_1 R_1 \tag{28}$$

$$V_2 = I_2 R_2 \tag{29}$$

$$V_{in} = I_{in} R_{in} \tag{30}$$

The values of all these resistances is arbitrary but for simplicity let

$$R_1 = R_2 = R_{in} = R_S = R_L = R \tag{31}$$

All the above transform the state equations into

$$\dot{I} = \frac{R^2}{L}\left(\frac{I_1}{R} - \frac{I_2}{R}\right) \tag{32}$$

$$\dot{I}_1 = \frac{1}{C_1}\left(\frac{I_{in}}{R} - \frac{I_1}{R} - \frac{I}{R} - C_2(\dot{I}_1 - \dot{I}_2)\right) \tag{33}$$

$$\dot{I}_2 = \frac{1}{C_3}\left(\frac{I}{R} + C_2(\dot{I}_1 - \dot{I}_2) - \frac{I_2}{R}\right) \tag{34}$$

Finally take:

$$C = \frac{L}{R^2} \tag{35}$$

and substituting in (32):

$$\dot{I} = \frac{1}{C}\left(\frac{I_1}{R} - \frac{I_2}{R}\right) \tag{36}$$

So equations (33), (34) and (36) are ready for a square root domain implementation. Taking all Rs equal is equivalent to taking all bias currents and expanding transistor aspect ratios in the circuit equal. This is neither a constraining nor an unusual approach, so the assumption was justified. The result is that each branch in the passive SFG in Fig. 15 with a multiplier value $\pm 1/R$ has an equivalent in the square root domain of $\pm\sqrt{2KI_{Bias}}$ where I_{BIAS} is the unified bias current used for all square root transconductors and K is the aspect ratio of the corresponding expanding transistor.

A question arises about which of the methods for assimilating differentiators into filters should be employed. The equations may suggest that the second method (the one used for the highpass filter) should be used, this can also be enticing since it would save on capacitors. However, close examination of either (34) or (33) reveals that this approach imposes a new constraint, namely that $C_1 = C_2 = C_3$. In general $C_1 = C_3$ is a property of elliptic filters but the additional constraint on C_2 is highly undesirable (namely it limits the maximum stopband attenuation obtainable using realistic capacitor ratios).

The circuit is not shown due to its complexity but the structure is rather straightforward. There are four capacitor nodes, only the one responsible for the differentiator is special. This part is designed as normally as the single input differentiator, the only difference is that this circuit has two inputs, namely I_1 and I_2. It is the (signal) difference between these currents that is the real differentiated variable. The output from this circuit is a new current equal to $C_2R(I_1 - I_2)\dot{}$. This current is considered an input to the integrating nodes of C_1 and C_3. The rest of the circuit is drawn directly from rules of conversion stated in Section 5. DC solution is found to be unique and sensible as long as the differentiator is taken care of.

To test the circuit a specific case was considered:
Cutoff frequency is 14.8 kHz
Maximum loss in passband is −2 dB
Minimum loss in stopband is −20 dB

Source and load resistance of 39.8 kΩ

These parameters yield (through any of a number of computer tools) capacitor and inductor values as follows:

$$C_1 = C_3 = 539.18\,\text{pF} \quad C_2 = 336.84\,\text{pF} \quad L = 0.199\,\text{H}$$

The value of resistance chosen is so that bias currents are all $4\,\mu\text{A}$ and expanding transistor aspect ratios are all unity.

From (35) and inductor and resistor values:

$$C = 125.91\,\text{pF}$$

HSPICE was used to simulate the circuit. The corresponding passive filter was used as an indicator of the ideal case. Simulation results in Fig. 16 show that the square root domain filter almost exactly follows the passive filter. Figure 17 shows more clearly where the two deviate. Particularly at high frequency the parasitic pole in the square root domain filter starts having an effect and causes some deviation but for all frequencies of interest the results are almost coincident with the ideal.

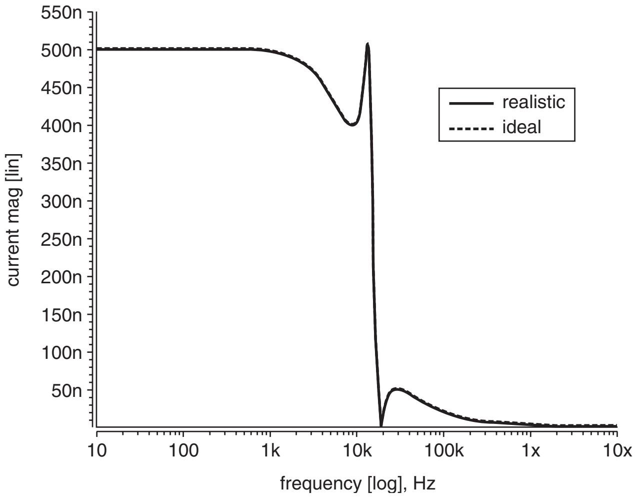

Fig. 16 *Elliptic filter magnitude response on a linear scale*

Simulations on this filter using basic stacked topology building blocks (from [1]) again follow the lead of differentiators and highpass filters in exhibiting channel length modulation. In this case the filter would not work at all. At most it manages to give a semblance of the stopband ripple but would never allow it to give much attenuation after cutoff and doesn't exhibit the sharp transition characteristic of elliptic filters.

A comparison of this filter with those in other sources turns out to be difficult. As mentioned earlier there are no examples of square root elliptic filters with which to compare. One could compare with the log-domain filters

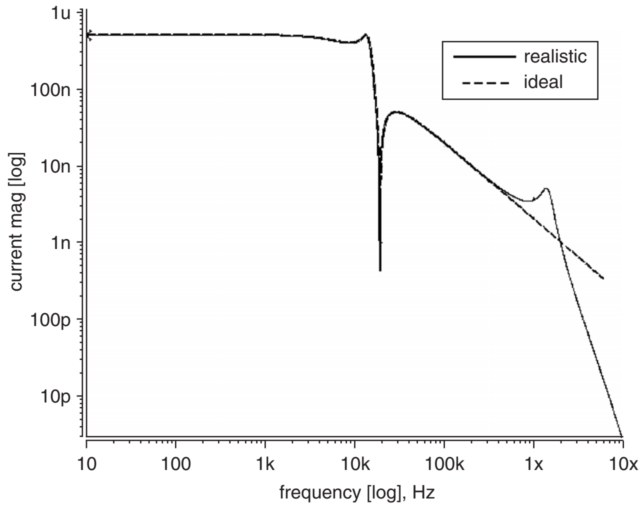

Fig. 17 *Elliptic filter magnitude response on a log scale*

of [3] and [4], in which case the results in Fig. 16 are quite superior in terms of accuracy. But a comparison between BJT and CMOS filters is unfair. For example the filters in [3] and [4] work at much higher frequencies than this filter (almost totally due to the fact that they are BJT).

5 Conclusions

A square root domain differentiator is proposed based on the principle of gyration. The differentiator takes into consideration the internal non-linearity of square root domain filters and thus achieves true input output differentiation. Two approaches to including differentiators in filters were proposed. A third-order elliptic lowpass filter was then designed to demonstrate the viability of the differentiator. All circuits were verified through HSPICE simulations.

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