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Long Tail Pair Based Positive CMOS Current Conveyors: A Review

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Abstract – A review on high performance long tail pair based CMOS CCII$^+$ realizations is made in this paper. For every circuit in the paper, CMOS realization is figured, principle of operation is discussed, equations that govern the operation are included, and simulation results are tabulated, figured and analyzed. Also, in some cases, the block diagram of the examined circuit is figured and discussed. Moreover, a fair comparison criterion is adopted while designing all the circuits in this paper. Its aim is to make the reader able to compare the simulation results of the CCII realizations fairly.

Index Terms – Analog Circuits, Current Conveyors, CCII

I. Introduction

In 1968 Smith and Sedra introduced the first generation current conveyor (CCI) [1] and in 1970 the second generation current conveyor (CCII) was proposed by the same two authors [2]. Since then CCII, which is essentially a combined voltage and current buffer, has proved to be functionally flexible and versatile, rapidly gaining acceptance as both a theoretical and practical building block [3, 4]. Current conveyors and related current-mode circuits have begun to emerge as an important class of circuits with properties that enable them to rival their voltage-mode counterparts in a wide range of applications. Current-mode circuits are suitable to operate under low voltage supplies since voltage swings are substituted by current swings in signal propagation. Key performance features of current-mode signal processing are wideband capability and a wide dynamic range under low power operation [5].

Firstly, CCII was realized in bipolar technologies and, recently high-performance CCII circuits have been designed in CMOS process [6-28]. It should be mentioned that current conveyors present an alternative method of implementing analog systems, which traditionally have been based on the voltage op-amp (VOA). Circuits based on the VOA are generally easy to design since the behavior of the VOA can be approximated by a few simple design rules. This is also true for current conveyors, and once the appropriate design rules are defined, conveyor based circuits can be designed in an easy way as in the case of the VOA case. A theorem relating a class of voltage op-amps and current conveyors was introduced in [29] making it possible to transform a conventional VOA based circuit into a CCII based circuit. Many authors have proved the versatility and flexibility of the CCII in analog circuit design for many applications [30-39].

The second generation current conveyor (CCII) symbol is shown in **Fig. 1**. It is a three terminal building block which is ideally defined by the following matrix equation:

$$\begin{bmatrix} i_y \\ v_x \\ i_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} v_y \\ i_x \\ v_z \end{bmatrix} \quad (1)$$

The voltage at terminal X follows the voltage at terminal Y. The current at terminal Z follows the current at terminal X. In equation (1), the (plus/minus) sign specifies the type of the current conveyor (CCII$^+$ or CCII$^-$). By convention, positive is taken to mean that the currents at the X and Z terminals are both flowing towards or away from the conveyor [6]. Throughout this paper the abbreviation CCII will be used instead of CCII$^+$ for simplicity. In practice, because of imperfections the CCII behavior deviates from ideality. A model for the non-ideal CCII is shown in **Fig. 2**.

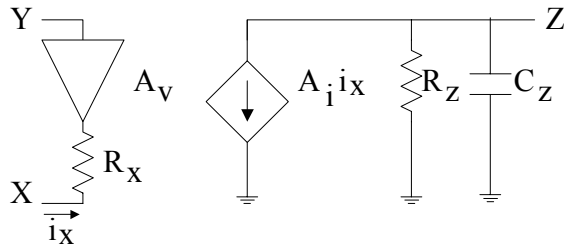

Fig. 2. Model of non-ideal CCII

Some of the high performance metrics of the CCII are: wide input voltage and current ranges, high accuracy in voltage and current transfer (gain equals to unity and offset is cancelled), wide voltage and current transfer bandwidths, low input impedance at terminal X, and high output impedance at terminal Z.

The CMOS realizations of the CCII can be classified into two categories: long tail pair based realizations and non long tail pair based realizations. In this paper, a review on high performance long tail pair based CMOS CCII$^+$ circuits is made. The examined CCII circuits are reported by Surakampontorn et al. [7], Liu et al. [8], Palmisano and Palumbo [9], Ismail and Soliman [10], Yodprasit [11], Laopoulos et al. [12], and Elwan and Soliman [13]. All these circuits operate in class-A mode except Laopoulos CCII which operates in class-AB mode.

In order to make the reader able to compare the simulation results of the CCII realizations fairly, a fair comparison criterion is adopted while designing all the circuits in this paper. This criterion has the following constraints [14]. Firstly, all circuits operate under the same supply voltages. The supply voltages are equal to 1.5V and -1.5V. Secondly, aspect ratios of equivalent transistors are equal and equivalent current sources are identical. The reference DC current source I_B is taken as 100μA. Thirdly, simulations are carried out with the same model and under the same circumstances. TOP SPICE simulations were carried out with level 8 model parameters of 0.5μm CMOS process provided by MOSIS (AGILENT). Terminal Z is grounded in all simulations, terminal X is open circuited while simulating the voltage transfer characteristics and terminal Y is grounded while simulating the current transfer characteristics.

Fig. 1: Symbol of the CCII

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Table 1: Simulation results of the circuits proposed in [7–13]

Parameter	Unit	Fig. 3	Fig. 5	Fig. 7	Fig. 9	Fig. 11	Fig. 12	Fig. 13
Input voltage range	V	-0.73 to 0.2	-0.5 to 0.8	-0.3 to 0.7	-0.4 to 0.9	-0.5 to 0.2	-0.5 to 0.7	-1.46 to 0.85
A_v (average value)	_	0.99385	0.99998	1.00014	0.989	0.999998	0.99996	0.99995
Voltage offset variation	mV	-4.52 to 2.27	-0.078 to -0.056	-0.642 to 0.506	-4.77 to 12.34	-0.0025 to -0.00047	-0.066 to -0.007	-0.771 to -0.043
F_{3db} of voltage transfer gain	MHz	776	1660	1800	589	7.5	2.7	1995
Input current range	µA	-100 to 100	-100 to 100	-100 to 100	-200 to 200	-100 to 100	-150 to 150	-100 to 100
A_i (average value)	_	1.0037	0.99991	0.9946	1.0038	1.01034	0.99998	0.99995
Current Offset variation	µA	-1.04 to -0.0006	-0.0035 to 0.006	0.583 to 2.35	1.05 to 3.08	-2.23 to -0.044	-0.001 to 0.0036	-0.004 to 0.0058
F_{3db} of current transfer gain	MHz	66	95	94.5	66.8	6.6	23	115
R_x	Ω	5.9	10.46	14.63	6.92	0.1	3.5	9.14

II. The Long Tail Pair Based Positive CCII circuits

1. Surakampontorn et al. CCII

1.1 Circuit Description

The CMOS realization of the CCII proposed in [7] is shown in **Fig. 3**. The transistor pairs (M_1 and M_2), (M_3 and M_4), (M_6 and M_7), as well as (M_9 and M_{10}) are matched. Assuming that all the transistors operate in their saturation regions, the operation of the circuit can be explained as follows. M_8, M_9 and M_{10} serve as DC current sources. M_8 holds $2I_B$ while each of M_9 and M_{10} holds I_B. The structure is based on the long tail pair (M_1 and M_2). The current mirror formed by M_3 and M_4 forces equal currents (I_B) in the transistors M_1 and M_2.

This operation drives the gate-to-source voltages of M_1 and M_2 to be equal and, consequently, forces the voltage at terminal X to follow the voltage at terminal Y. Transistor M_5, is connected in the form of a source follower. The X terminal current is conveyed to the Z terminal by the current mirroring action of the transistors M_6 and M_7.

The block diagram of the CCII proposed in [7] is shown in **Fig. 4**. The scheme includes two transconductance amplifiers with differential inputs. The first is implemented by the long tail pair (M_1 and M_2) where $G_1 = g_{m1} = g_{m2}$. The second is implemented by the transistor M_5 where $G_2 = g_{m5}$ and the current mirror (M_6 and M_7) which is responsible for providing a replica of the output current of the transconductance to the Z terminal. The voltage following action is the result of the negative-feedback closed-loop structure implemented by blocks G_1 and G_2. In this manner, both accuracy in the voltage transfer gain and low resistance at terminal X are achieved for high open loop gains.

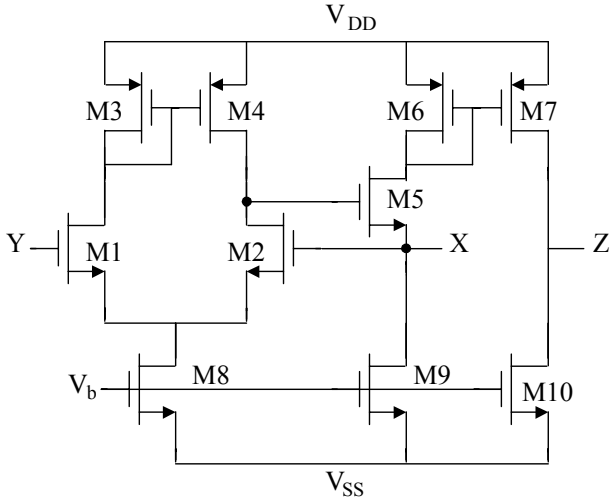

Fig. 3: CCII realization proposed in [7]

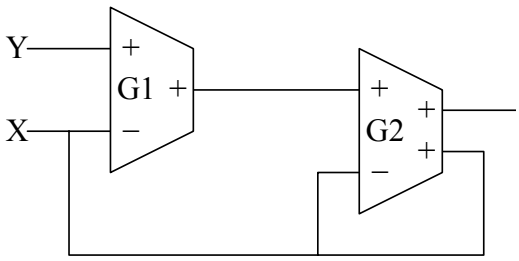

Fig. 4: Block diagram of the circuit shown in Fig. 3

Taking the finite value of transistor transconductance g_m and drain to source conductance g_d into consideration, the small signal voltage transfer gain from the Y terminal to the X terminal is approximately given by:

$$\frac{v_x}{v_y} = \frac{g_{m1}}{g_{m1} + g_{d2} + g_{d4}} \tag{2}$$

where $g_{m1} = g_{m2}$.

The input resistance at terminal X and the output resistance at terminal Z are:

$$r_x = \frac{g_{d2} + g_{d4}}{g_{m5}\left(g_{m1} + g_{d2} + g_{d4}\right)} \tag{3}$$

$$r_z = \frac{1}{g_{d7} + g_{d10}} \tag{4}$$

1.2 Simulation Results

The aspect ratio of M_1 and M_2 is 60µm/1µm. The aspect ratio of M_3, M_4, M_6, M_7, and M_8 is 100µm/2.5µm. The aspect ratio of M_5 is 20/0.5µm. The aspect ratio of M_9 and M_{10} is 50µm/2.5µm. The circuit is compensated by using a capacitor C = 1.5pF (connected between the drain of M_2 and terminal X). Simulation results are tabulated in **Table 1**. These results can be described as follows. The input voltage range is from -0.73V to 0.2V. The average value of the open circuit voltage transfer gain equals 0.99385.

The voltage offset varies from -4.52mV to 2.27mV within the input voltage range. The open circuit voltage transfer bandwidth exhibits a 3-dB frequency of 776MHz. The input current range equals 200µA. The average value of the short circuit current transfer gain equals 1.0037. The current offset varies from -1.04µA to -0.0006µA within the input current range. The short circuit current transfer bandwidth exhibits a 3-dB frequency of 66MHz. The input resistance at terminal X at D.C equals 5.9 Ω. Finally, the total harmonic distortion (THD) for an input sinusoid of frequency 100KHz and amplitude 0.5V p-p is 0.09003%.

2. Liu et al. CCII

2.1 Circuit Description

The simplified CMOS realization of the CCII proposed in [8] is shown in **Fig. 5** (the cascoding is removed and ordinary current mirrors are used instead of the CCI cells in order to maintain fair tradeoffs for comparison). The transistor pairs (M_1 and M_2), (M_3 and M_4), (M_5 and M_6), as well as (M_8 and M_9) are matched. Assuming that all the transistors operate in their saturation regions, the operation of the circuit can be explained as follows. M_7, M_8 and M_9 serve as DC current sources. M_7 holds $2I_B$ while each of M_8 and M_9 holds I_B. The structure is based on the long tail pair (M_1 and M_2). The current mirror formed by M_3 and M_4 forces equal currents I_B in the transistors M_1 and M_2. This operation drives the gate-to-source voltages of M_1 and M_2 to be equal and, consequently, forces the voltage at terminal X to follow the voltage at terminal Y. The two common source transistors M_5 and M_6 are responsible for conveying the X terminal current to the Z terminal.

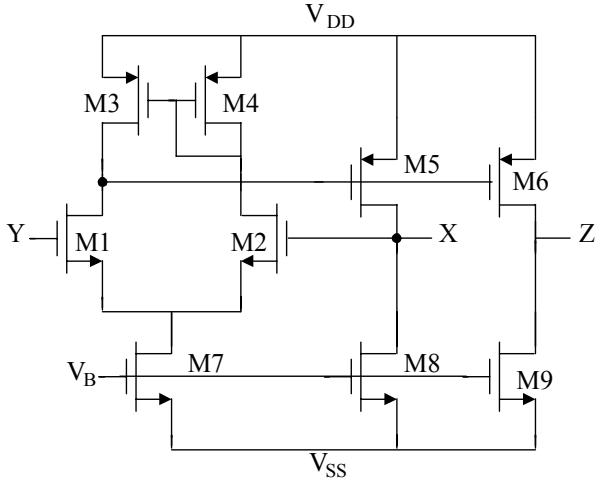

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Fig. 5: CCII realization proposed in [8]

The following offset cancellation technique can be applied to the circuit. The voltage offset is given by the following relation [15]:

$$\Delta V = V_x - V_y \approx \left[\lambda_n (V_{D1} - V_{D2})\right] \sqrt{\frac{I_B}{\mu_n C_{ox} \frac{W_1}{L_1}}} \tag{5}$$

where λ_n is the channel length modulation parameter, V_{D1} and V_{D2} are the drain voltages of M_1 and M_2 respectively. This offset can be cancelled by making V_{D1} equal to V_{D2}.

$$V_{D1} - V_{D2} = \sqrt{\frac{I_{D4}}{\mu_p C_{ox} \frac{W_4}{L_4}}} - \sqrt{\frac{I_{D5}}{\mu_p C_{ox} \frac{W_5}{L_5}}} \tag{6}$$

It is seen from equation (6) that the offset cancellation is achieved by matching M_4 and M_5 and by making $I_{D4} = I_{D5} = I_B$. But, unfortunately, this can only be achieved at $I_X = 0$A otherwise the circuit exhibits larger offset. In other words, the offset cancellation is dependent on the input current at terminal X which is a critical disadvantage. A second disadvantage is the constraint put on the value of I_{D7} as it should equal $2I_{D8}$. This doubling can't be achieved precisely as long as the drains of M_7 and M_8 are at different voltage levels. Hence, even the voltage offset cancellation at zero input current won't be of relatively high performance.

The block diagram of the CCII proposed in [8] is shown in **Fig**. 6. The scheme includes three main blocks: a transconductance amplifier with a differential input which is implemented by

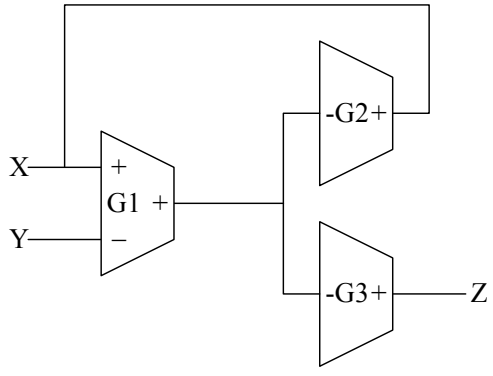

Fig. 6: Block diagram of the circuit shown in Fig. 5

the long tail pair (M_1 and M_2) where $G_1 = g_{m1} = g_{m2}$ and two matched inverting transconductance output stages connected in parallel which are implemented by transistors M_5 and M_6 where $G_2 = g_{m5} = G_3 = g_{m6}$ and $r_{o2} = r_{o3}$.

The voltage following action is the result of the negative-feedback closed-loop structure implemented by blocks G_1 and G_2. Note that to maintain stability, the feedback action was made on the positive input terminal of G_1 (terminal X in this case). Another advantage of the common source stage (M_5 and M_8) is that it can give larger open loop gain in addition to the ordinary buffering action performed by the source follower in Surakampontorn CCII [7] (section 2.1). Consequently, higher accuracy in the voltage transfer gain is achieved. Low input resistance is achieved thanks to the high open loop gain negative feedback mechanism. G_3 is responsible for taking a replica of the X terminal current to deliver it to the Z terminal.

The small signal voltage transfer gain from the Y terminal to the X terminal is approximately given by:

$$\frac{v_x}{v_y} = \frac{g_{m1}g_{m5}}{g_{m1}g_{m5} + (g_{d1} + g_{d3})(g_{d5} + g_{d8})} \tag{7}$$

where $g_{m1} = g_{m2}$.

The input resistance at the X terminal is approximately given by:

$$r_x = \frac{g_{d1} + g_{d3}}{g_{m1}g_{m5}} \tag{8}$$

The output resistance at the Z terminal is given by:

$$r_z = \frac{1}{g_{d6} + g_{d9}} \tag{9}$$

2.2 Simulation Results

The aspect ratio of M_1 and M_2 is 60µm/1µm. The aspect ratio of M_3 to M_7 is 100µm/2.5µm. The aspect ratio of M_8 and M_9 is 50µm/2.5µm. Simulation results are tabulated in **Table 1**. These results can be described as follows. The input voltage range is from -0.5V to 0.8V. The average value of the open circuit voltage transfer gain equals 0.99998. The voltage offset varies from -0.078mV to -0.056mV within the input voltage range. The voltage offset increases considerably for non zero input current. The open circuit voltage transfer bandwidth exhibits a 3-dB frequency of 1660MHz. The input current range equals 200µA. The average value of the short circuit current transfer gain equals 0.99991. The current offset varies from -0.0035µA to 0.006µA within the input current range. The short circuit current transfer bandwidth exhibits a 3-dB frequency of 95MHz. The input resistance at terminal X at D.C equals 10.46 Ω. Finally, the total harmonic distortion (THD) for an input sinusoid of frequency 100KHz and amplitude 0.5V p-p is 0.01742%.

3. Palmisano and Palumbo CCII

3.1 Circuit Description

The CMOS realization of the CCII proposed in [9] is shown in **Fig. 7**. The transistor pairs (M_1 and M_2), and (M_4 and M_6) are matched. Assuming that all transistors operate in their saturation regions, the operation of the circuit can be explained as follows. M_3, M_5 and M_7 serve as DC current sources. M_5 holds $2I_B$ while each of M_3 and M_7 holds I_B. The structure is based on the long tail pair (M_1 and M_2). The current flowing through M_2 is forced to be equal to that flowing through M_1 and equals I_B causing the gate-to-source voltages of M_1 and M_2 to be equal. As a result the voltage at terminal X follows that at terminal Y. The two common source transistors M_4 and M_6 are responsible for conveying the X terminal current to terminal Z.

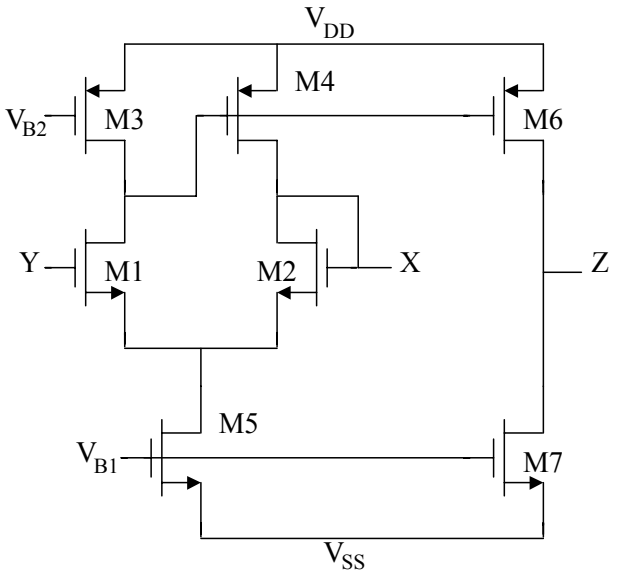

Fig. 7: CCII realization proposed in [9]

The block diagram of the CCII proposed in [9] is shown in **Fig. 8**. It can be seen that it is similar to the block diagram of Liu CCII [8] (**Fig. 6**). The differences here are the local negative feedback on G_1 and the implementation of G_1 itself. It is still implemented by the long tail pair (M_1 and M_2) but the current mirror transistors are removed and only a current source transistor M_3 is used instead. This gives a simple realization using minimum number of transistors which is the main advantage of the circuit. Consequently the value of G_1 differs from the case of Liu CCII. $G_1 = ½\ g_{m1}$, $G_2 = g_{m4}$ and $G_3 = g_{m5}$. However, high accuracy in voltage transfer gain and low input resistance at terminal X are still achieved thanks to the high open loop gain negative feedback mechanism.

The small signal voltage transfer gain from terminal Y to terminal X is approximately given by:

$$\frac{v_x}{v_y} = \frac{g_{m1}}{g_{m1} + g_{d1} + \dfrac{g_{d4}(g_{d1} + 2g_{d3})}{g_{d3} + g_{m4}}} \tag{10}$$

where $g_{m1} = g_{m2}$.

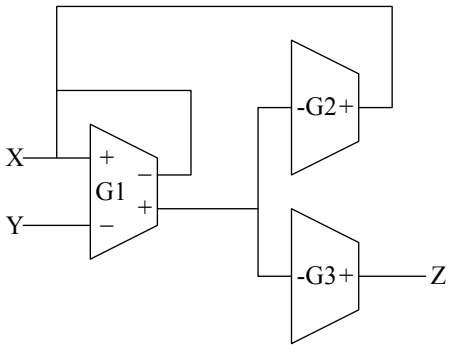

Fig. 8: Block diagram of the circuit shown in Fig. 7

The input resistance at terminal X is approximately given by:

$$r_x = \frac{g_{d1} + 2g_{d3}}{(g_{m1} + g_{d1})(g_{m4} + g_{d3}) + g_{d4}(g_{d1} + 2g_{d3})} \quad (11)$$

The output resistance at terminal Z is given by:

$$r_z = \frac{1}{g_{d6} + g_{d7}} \quad (12)$$

3.2 Simulation Results

The aspect ratio of M_1 and M_2 is 60µm/1µm. The aspect ratio of M_3 to M_6 is 100µm/2.5µm. The aspect ratio of M_7 is 50µm/2.5µm. Simulation results are tabulated in Table 1. These results can be described as follows. The input voltage range is from -0.3V to 0.7V. The average value of the open circuit voltage transfer gain equals 1.00014. The voltage offset varies from -0.642mV to 0.506mV within the input voltage range. The open circuit voltage transfer bandwidth exhibits a 3-dB frequency of 1800MHz. The input current range equals 200µA. The average value of the short circuit current transfer gain equals 0.9946. The current offset varies from 0.583µA to 2.35µA within the input current range. The short circuit current transfer bandwidth exhibits a 3-dB frequency of 94.5MHz. The input resistance at terminal X at D.C equals 14.63Ω. Finally, the total harmonic distortion (THD) for an input sinusoid of frequency 100KHz and amplitude 0.5V p-p is 0.05539%.

4. Ismail and Soliman CCII

4.1 Circuit Description

The CMOS realization of the CCII proposed in [10] is shown in **Fig. 9**. The groups of transistors (M_1-M_4), (M_5-M_{8b}) as well as (M_9-M_{11}) are matched. Assuming that all the transistors operate in their saturation regions, the operation of the circuit can be explained as follows. M_9, M_{10} and M_{11} serve as DC current sources holding equal currents of $2I_B$. The circuit consists of two long tail pairs (M_1 and M_3) and (M_2 and M_4). It can be easily noted that the transistors (M_3-M_6) form the first generation current conveyor CCI introduced in [1]. It conveys the voltage from the source of the transistor M_3 to the source of the transistor M_4 and the current from the transistor M_6 to the transistor M_5. Hence, the voltage at terminal Y is conveyed to terminal X. The current coming from X is reproduced at Z by the action of the common source transistors (M_7-M_{8b}).

The block diagram of the CCII proposed in [10] is shown in **Fig.** 10. This circuit achieves low input resistance at terminal X. Two matched differential input transconductor amplifiers (G_1 and G_6) are used. They are implemented by the two long tail pairs (M_2 and M_4) and (M_1 and M_3) respectively. Note that in this architecture $G_2 = G_4 = G_5 = ½\ G_3$ for successful current conveying to take place.

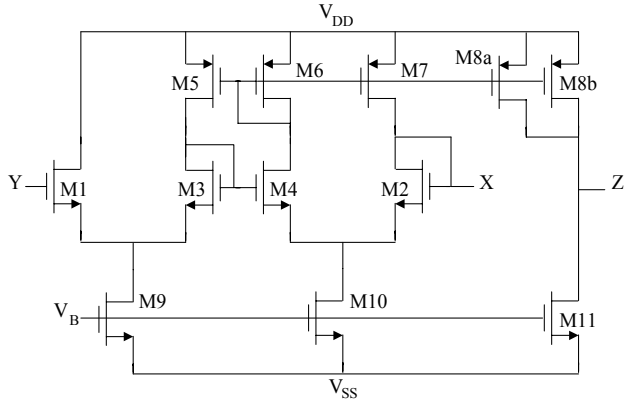

Fig. 9: CCII realization proposed in [10]

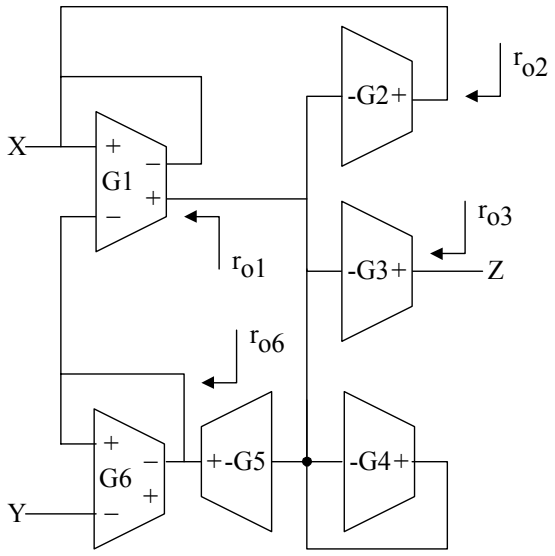

Fig. 10.: Block diagram of the circuit shown in Fig. 9

The small signal voltage transfer gain from terminal Y to terminal X is approximately given by [10]:

$$\frac{v_x}{v_y} = \frac{1}{1 + \frac{g_{d3} + g_{d5}}{g_{m1}} + \frac{(g_{d3} + g_{d5})(g_{d2} + g_{d7})}{2g_{m1}^2}} \quad (13)$$

The input resistance at terminal X is approximately given by [10]:

$$r_x = \frac{g_{d3} + g_{d5}}{2g_{m1}(g_{m1} + g_{d3} + g_{d5})} \quad (14)$$

The output resistance at terminal Z is given by:

$$r_z = \frac{1}{g_{d8} + g_{d11}} \quad (15)$$

4.2 Simulation Results

The aspect ratio of M_1 to M_4 is 60µm/1µm. The aspect ratio of M_5 to M_{11} is 100µm/2.5µm. Simulation results are tabulated in Table 1. These results can be described as follows. The input voltage range is from -0.4V to 0.9V. The average value of the open circuit voltage transfer gain equals 0.989. The voltage offset varies from -4.77mV to 12.34mV within the input voltage range. The open circuit voltage transfer bandwidth exhibits a 3-dB frequency of 589MHz.

The circuit is designed following the fair comparison criterion adopted throughout the paper. To maintain the same long tail pair tail current as the rest of the circuits equals to $2I_B$, the DC current of the output stage must be $2I_B$ instead of I_B. Consequently, the circuit showed an input current range of 400µA instead of 200µA.

The average value of the short circuit current transfer gain equals 1.0038. The current offset varies from 1.05µA to 3.08µA

within the input current range. The short circuit current transfer bandwidth exhibits a 3-dB frequency of 66.8MHz. The input resistance at terminal X at D.C equals 6.92Ω. This is less than the input resistance of Palmisano CCII which equals 14.63Ω. Finally, the total harmonic distortion (THD) for an input sinusoid of frequency 100KHz and amplitude 0.5V p-p is 0.02173%.

5. Yodprasit CCII

5.1 Circuit Description

The simplified CMOS realization of the CCII proposed in [11] is shown in **Fig.** 11 (the cascode current mirrors are removed and ordinary current mirrors are used instead in order to maintain fair

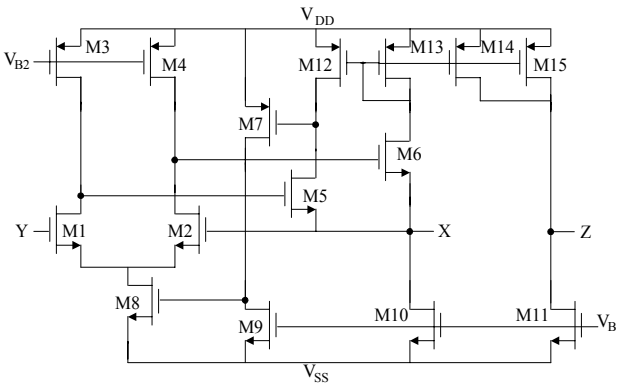

Fig. 11: CCII realization proposed in [11]

tradeoffs for comparison). The groups of the transistors (M_1 and M_2), (M_3 and M_4), (M_5 and M_6), (M_7 and M_{12}-M_{15}) as well as (M_{10} and M_{11}) are matched. Assuming that all the transistors operate in their saturation regions, the operation of the circuit can be explained as follows. M_3, M_4, M_9, M_{10} and M_{11} serve as DC current sources. M_3, M_4, M_{10} and M_{11} holds I_B each, while M_9 holds $0.5I_B$. The circuit utilizes a long tail pair (M_1 and M_2) to transfer V_Y to V_X. The voltage transfer occurs because the source terminals of M_1 and M_2 are at the same potential and they are biased by equal currents I_B. Current mirrors M_{12}-M_{15} are responsible for conveying the X terminal current to terminal Z.

The circuit comprises a high-precision voltage follower. It adopts the offset cancellation technique applied on Liu CCII [8] (section 2.2). However, this time the offset cancellation is independent of the input current I_X. Hence, it overcomes the first disadvantage of the case of Liu CCII. The voltage offset is given by equation (5). This offset can be cancelled by making V_{D1} equal to V_{D2}.

$$V_{D1} - V_{D2} = \sqrt{\frac{I_{D5}}{\mu_n C_{ox} W_5/L_5}} - \sqrt{\frac{I_{D6}}{\mu_n C_{ox} W_6/L_6}} \tag{16}$$

Also, there are no constraints on the values of I_{D3} or I_{D4} (yet they are taken I_B to maintain fair comparisons). It is seen from equation (16) that the offset cancellation is achieved by matching M_5 and M_6 and by making $I_{D5} = I_{D6}$. Their currents are held equal by a current mirror (M_{12} and M_{13}). As in the case of the long tail pair, the drain voltages of M_5 and M_6 need to be as equal as possible to achieve precise current mirroring. Therefore, a common source amplifier (M_7 and M_9) is used to keep the drain voltage of M_5 in a range close to the drain of M_6. This way the circuit overcomes the second disadvantage of the case of Liu CCII. However, although the circuit introduces an elegant technique to make full voltage offset cancellation, unfortunately, the technique is dependent on the voltage of terminal X. In other words, as the voltage of the X terminal increases M_5 and M_6 leave their saturation regions resulting in a narrow input voltage range. This is a disadvantage in the examined architecture. Also, the circuit sacrifices the bandwidth for high voltage tracking accuracy. However, it should be stated that the author used high swing cascode current mirrors to increase the current tracking accuracy.

The feedback loop is closed by applying negative feedback locally around the long tail pair. The small signal voltage transfer gain is approximately given by [11]:

$$\frac{v_x}{v_y} = \frac{g_{m5}g_{m7}g_{m8}}{g_{m5}g_{m7}g_{m8} - g_{d3}g_{d5}g_{d7}} \tag{17}$$

where $g_{m1} = g_{m2}$.

The input resistance at terminal X is approximately given by [11]:

$$r_x = \frac{g_{d1}g_{d5}g_{d7}}{g_{m1}g_{m5}g_{m7}g_{m8}} \tag{18}$$

The output resistance at terminal Z is given by:

$$r_z = \frac{1}{g_{d11} + g_{d14} + g_{d15}} \tag{19}$$

5.2 Simulation Results

The aspect ratio of M_1 and M_2 is 60µm/1µm. The aspect ratio of M_3, M_4, M_7, M_8, and M_{12} to M_{15} is 100µm/2.5µm. The aspect ratio of M_5 and M_6 is 20µm/0.5µm. The aspect ratio of M_9 is 25µm/2.5µm. The aspect ratio of M_{10} and M_{11} is 50µm/2.5µm. The circuit is compensated by using a capacitor C = 20PF (connected between the drains of M_2 and M_6). Simulation results are tabulated in Table 1. These results can be discussed as follows. The input voltage range is from -0.5V to 0.2V. The average value of the open circuit voltage transfer gain equals 0.999998. The voltage offset varies from -0.0025mV to -0.00047mV within the input voltage range. The open circuit voltage transfer bandwidth exhibits a 3-dB frequency of 7.5MHz. The input current range equals 200µA. The average value of the short circuit current transfer gain equals 1.01034. The current offset varies from -2.23µA to -0.044µA within the input current range. The short circuit current transfer bandwidth exhibits a 3-dB frequency of 6.6MHz. The input resistance at terminal X at D.C equals 0.1Ω. Finally, the total harmonic distortion (THD) for an input sinusoid of frequency 10KHz and amplitude 0.5V p-p is 0.018%.

Compared to the previous circuits, Yodprasit CCII exhibits the highest accuracy in voltage following regarding the transfer gain and offset, and the lowest input resistance. However, the circuit features the lowest input voltage range and the lowest voltage and current transfer bandwidths.

6. Laopoulos et al. CCII

6.1 Circuit Description

The CMOS realization of the CCII proposed in [12] is shown in **Fig.** 12. The transistor pairs (M_1, M_2 and M_6), (M_3-M_5 and M_{14}), (M_9-M_{11}), as well as (M_{12}, M_{13} and M_{15}) are matched. Assuming that all the transistors operate in their saturation regions, the

operation of the circuit can be explained as follows. M_7 and M_8 serve as DC current sources. M_7 holds $3I_B$ while M_8 holds I_B. The structure is based on the long tail pair (M_1 and M_2). The current mirror formed by M_3 and M_4 forces equal currents in the transistors M_1 and M_2. This operation drives the gate-to-source voltages of M_1 and M_2 to be equal and, consequently, forces the voltage at terminal X to follow the voltage at terminal Y. Since the current flowing in M_{11} equals to that flowing in M_9 and the current flowing in M_{15} equals to that flowing in M_{13}, the X terminal current is conveyed to the Z terminal successfully.

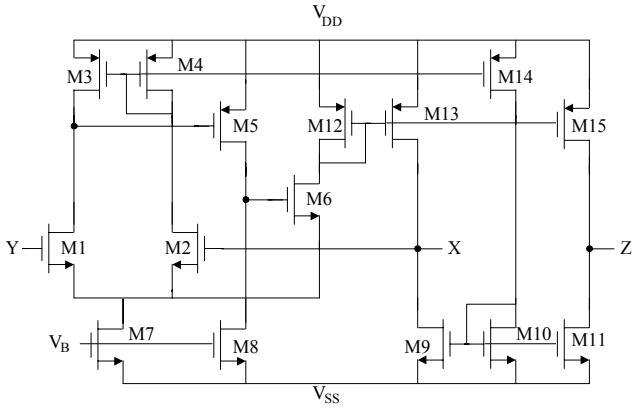

Fig. 12: CCII realization proposed in [12]

The same offset cancellation technique which is applied on Liu CCII [8] (section 2.2) is applied on this circuit. The voltage offset is given by equation (5). This offset can be cancelled by making V_{D1} equal to V_{D2}.

$$V_{D1} - V_{D2} = \sqrt{\frac{I_{D4}}{\mu_p C_{ox} W_4/L_4}} - \sqrt{\frac{I_{D5}}{\mu_p C_{ox} W_5/L_5}} \qquad (20)$$

It is seen from equation (20) that the offset cancellation is achieved by matching M_4 and M_5 and by making $I_{D4} = I_{D5} = I_B$. Similar to the case of Liu CCII, this offset cancellation can only be achieved at $I_X = 0$ otherwise the circuit exhibits larger offset. In other words, the offset cancellation is dependent on the input current at terminal X which is the first disadvantage. A second disadvantage in this technique is the constraint put on the value of I_{D7} as it should equal $3I_{D8}$ where this tripling can't be achieved precisely as long as the drains of M_7 and M_8 are at different voltage levels. Hence, even the voltage offset cancellation at zero input current won't be of relatively high performance. This disadvantage appeared secondly in the case of Liu CCII.

At zero I_X the current flowing in M_{12} is forced to be equal to that flowing in M_3 and M_4 and equals to I_B (one third the tail current of the long tail pair). That is due to the current mirroring action done by transistors (M_4, M_{14}), (M_{10}, M_9) and (M_{13}, M_{12}) and tying the source of M_6 to those of M_1 and M_2. Note that it is not a must that M_{14} has the same dimensions of M_3 and M_4. The ratio of current transfer from M_4 to M_{14} can be controlled taking care that the reverse ratio must be used in current transfer from M_{13} to M_{12} to ensure proper operation.

This circuit does not operate in class-A mode like the five circuits discussed so far. It uses a class-AB current transfer stage. Here, the ratios of current transfer from M_4 to M_{14} and from M_{13} to M_{12} are taken unity. Hence, the push-pull action of transistors M_9 and M_{13} can be easily noticed from the following DC equations.

$$I_9 = I_B + \frac{1}{3} I_X \qquad (21)$$

$$I_{13} = I_B - \frac{2}{3} I_X \qquad (22)$$

6.2 Simulation Results

The aspect ratio of M_1, M_2 and M_6 is 60µm/1µm. The aspect ratio of M_3 to M_5 and M_{12} to M_{15} is 100µm/2.5µm. The aspect ratio of M_7 is 150µm/2.5µm. The aspect ratio of M_8 to M_{11} is 50µm/2.5µm. The circuit is compensated by using 2 capacitors C_1 = 1.5pF (connected between the drain of M_1 and terminal X) and C_2 = 10nF (connected between the drain of M_1 and V_{SS}). Simulation results are tabulated in Table 1. These results can be described as follows. The input voltage range is from -0.5V to 0.7V. The average value of the open circuit voltage transfer gain equals 0.99996. The voltage offset varies from -0.066mV to -0.007mV within the input voltage range. Similar to Liu CCII, the voltage offset increases significantly for non zero input current.

The circuit is designed to feature a standby current of I_B = 100µA to achieve voltage offset cancellation at zero input current. Though, the input current ranges from $-3I_B$ to $1.5I_B$ it is reported that it ranges from $-1.5I_B$ to $1.5I_B$ (300µA). The reasons are as follows. The voltage offset increases noticeably when the input current ranges from $-3I_B$ to $-1.5I_B$. It ranges from -0.6mV to -2.8mV. The second reason is to report an input current range which is symmetrical around the zero. This criterion in obtaining the input current range of any CCII is adopted throughout the thesis.

The open circuit voltage transfer bandwidth exhibits a 3-dB frequency of 2.7MHz. The average value of the short circuit current transfer gain equals 0.99998. The current offset varies from -0.001µA to 0.0036µA within the input current range. The short circuit current transfer bandwidth exhibits a 3-dB frequency of 23MHz. The input resistance at terminal X at D.C equals 3.5Ω. Finally, the total harmonic distortion (THD) for an input sinusoid of frequency 10KHz and amplitude 0.5V p-p is 0.0252%.

Compared to Yodprasit CCII, the circuit exhibits more voltage offset, and higher input resistance at the X terminal. However, the circuit features higher input voltage and current ranges as well as lower current offset. The voltage and current transfer bandwidths are still much lower than the first four circuits examined in this paper.

7. Elwan and Soliman CCII

7.1 Circuit description

The CMOS realization of the CCII proposed in [13] is shown in **Fig.** 13. The groups of the transistors (M_1 and M_2), (M_3-M_6), (M_8 and M_9), (M_{10} and M_{11}) as well as (M_{12}-M_{15}) are matched. Assuming that all the transistors operate in their saturation regions, the operation of the circuit can be explained as follows. Transistors M_7, M_8, M_9 and M_{16} serve as DC current sources. M_7 holds $1.3I_B$. M_{16} holds $0.5I_B$. Each of M_8 and M_9 holds I_B. The structure is based on two long tail pairs to provide a rail to rail operation at the Y and X terminals. Transistors M_1 and M_2 conduct till the positive supply rail, while transistors M_{10} and M_{11} conduct for signal swing down to the negative supply rail. By the current mirroring action of transistors M_{12}, M_{13} and M_{14}, M_{15} the currents are summed at the drains of M_1 and M_2. Transistors M_3 and M_4 force these currents to be equal. Hence, the voltage at terminal X follows that at terminal Y. The two common source transistors M_5 and M_6 are responsible for conveying the X terminal current to the Z terminal.

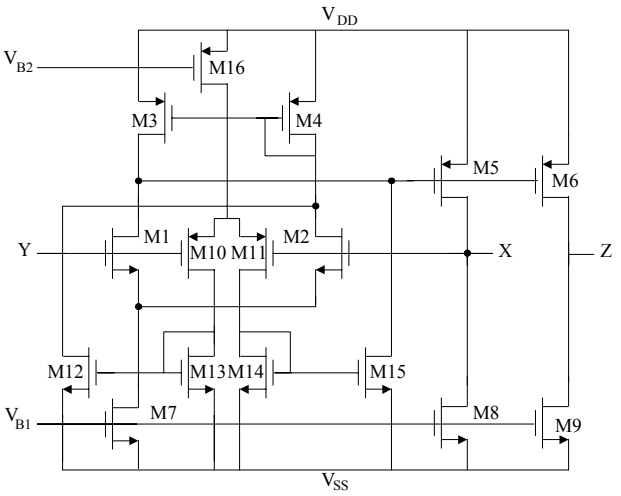

Fig. 13: CCII realization proposed in [13]

The circuit is considered to be the rail to rail version of Liu CCII [8] (section 2.2). The same offset cancellation technique applied on Liu CCII is used here. However, unfortunately, the two disadvantages that appear in Liu CCII reappear here. Firstly, the voltage offset cancellation is dependent on the input current. The circuit is designed to cancel the offset at zero input current only. Also, to achieve offset cancellation at zero input current the following equation should be satisfied.

$$I_{D4} = \frac{1}{2}\left(I_{D7} + I_{D16}\right) = I_8 = I_B \qquad (23)$$

According to the reported realization, this equation is hardly achieved with a high level of precision. This is the second disadvantage.

7.2 Simulation Results

The aspect ratio of M_1, M_2, M_{10} and M_{11} is 60µm/1µm. The aspect ratio of M_3 to M_6 is 100µm/2.5µm. The aspect ratio of M_7 is 65µm/2.5µm. The aspect ratio of M_8, M_9 and M_{12} to M_{16} is 50µm/2.5µm. The circuit is compensated by using a capacitor C = 100PF (connected between the drain of M_7 and terminal X). Simulation results are tabulated in Table 1. These results can be described as follows. The input voltage range is from -1.46V to 0.85V. The average value of the open circuit voltage transfer gain equals 0.99995.

The voltage offset varies from –0.771mV to -0.043mV within the input voltage range. The voltage offset increases considerably for non zero input current. The open circuit voltage transfer bandwidth exhibits a 3-dB frequency of 1995MHz. The input current range equals 200µA. The average value of the short circuit current transfer gain equals to 0.99995. The current offset varies from -0.004µA to 0.0058µA within the input current range. The short circuit current transfer bandwidth exhibits a 3-dB frequency of 115MHz. The input resistance at terminal X at D.C equals 9.14Ω. Finally, the total harmonic distortion (THD) for an input sinusoid of frequency 100KHz and amplitude 0.5V p-p is 0.0175%.

This circuit is characterized by supporting the rail to rail operation. It shows the largest input voltage range so far. Compared to Liu CCII, the circuit provides higher input voltage range and higher voltage and current transfer bandwidths while keeping all other parameters in the same range.

Conclusions

A survey on long tail pair based CMOS CCII$^+$ circuits was made in this paper. High performance CCII$^+$ realizations that were proposed by Surakampontorn et al. [7], Liu et al. [8], Palmisano and Palumbo [9], Ismail and Soliman [10], Yodprasit [11], Laopoulos et al. [12], and Elwan and Soliman [13] are reviewed. Simulation results that verify the theoretical analysis were included.

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