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Low distortion CMOS transconductance amplifier

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A novel low distortion CMOS linearized transconductor circuit is developed for analogue signal processing. The circuit gives a very low distortion level and a wide linearity range when compared with other reported topologies. Simulation results based on using the 0.5 μm CMOS process show that this approach gives an exceptional linearity and an excellent performance.

1. Introduction

Transconductance elements are useful building blocks in analogue signal processing systems, especially in continuous time filters and four-quadrant multipliers (Babanezhad and Temes 1985, Seevinck and Wassenaar 1987, Wilson and Chan 1990, Sevenhans and Van Paemel 1991, Raut 1992, Ismail and Soliman 1999, Mahmoud and Soliman 1999). Many implementations have been reported in the literature for obtaining highly linear transconductors. Among these realizations are those based on the long tail differential pair (LTP) which have received great interest since they offer a relatively low level of distortion because of second order effects such as body-effect and mobility degradation (Nedungadi and Viswanathan 1984, Wilson and Chan 1990). In addition, the power consumption of these structures is usually limited compared with other realizations. Several techniques have been described to extend the linearity range of the LTP (Nedungadi and Viswanathan 1984, Babanezhad and Temes 1985, Wilson and Chan 1990, Sevenhans and Van Paemel 1991, Kimura 1994, Ismail *et al.* 1999). The cross-coupled technique was first proposed by Khorramabadi (1985); this properly scales the aspect ratios of the differential pair and the bias current used. Then the adaptively biased CMOS differential pair was introduced by Nedungadi *et al.* (1984). Other techniques have been reported in the literature (Wang and Guggenbuhl 1990, Kimura 1994, Ismail *et al.* 1999).

In Wilson and Chan (1991), different topologies for current tail-based realizations of linear transconductors have been studied and it has been shown by simulations that the total harmonic distortion (THD) resulting from second order effects (mainly the body effect and mobility reduction effect) is a minimum for the 'antiphase common-source' topologies. In addition, the obtained differential mode linearity range is a maximum. However, the price paid for such advantages was an increased number of transistors; also a negative feedback stabilization action on the source node of the differential pair is necessary by means of an amplifier stage.

In this paper, a new realization for a low distortion CMOS transconductor based on the antiphase common source topology is introduced. In this realization, no

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amplifier stages are required. Instead, a current feedback action is used to control the voltage of the source node. Analysis is then developed to show the errors owing to the second order effects. Simulation results prove that the new circuit gives a considerably wide linearity range in addition to a very low distortion level.

2. Circuit description

Consider the circuit shown in figure 1. Ml and M2 form the main differential pair of the transconductor. The output current I_{OUT} is produced at the drains of M2 and M4. The main idea is to clamp V_S to a certain dc level tracking the common mode voltage of V_1 and V_2.

Assuming that the transistor square law characteristic is given by

$$I = \frac{K_n}{2}(V_{GS} - V_T)^2 \tag{1}$$

$$K_n = (\mu_n C_{OX})\left(\frac{W}{L}\right) \tag{2}$$

where V_T is the threshold voltage, K_n is the transconductance parameter, μ_n is the effective carrier mobility, C_{OX} is the gate oxide capacitance per unit area, W is the channel width and L is the channel length. It is also assumed that all body terminals are connected to the proper supply voltages and that the channel length modulation effect is neglected.

Consider the complete circuit of the transconductor shown in figure 2. Transistors M1a,M1b and M2a,M2b are assumed to be matched as well as M4,M5a,M5b and M6,M7. A floating current source I_B is used in the circuit, which can be realized as shown in figure 3. The current mirrors M4,M5a,M5b and M6,M7 are used to feed a current to the source of the differential pair which is equal to double the current flowing in M4. Using this current feedback technique, the current I_B will always flow in M3 without the need for amplifier stages (Wilson and Chan 1991). In this case, the output current I_{OUT} is given by

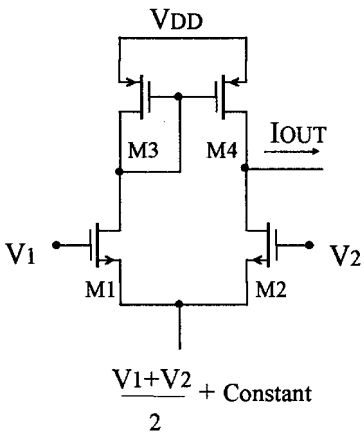

Figure 1. The simplified circuit for the antiphase common source transconductance amplifier.

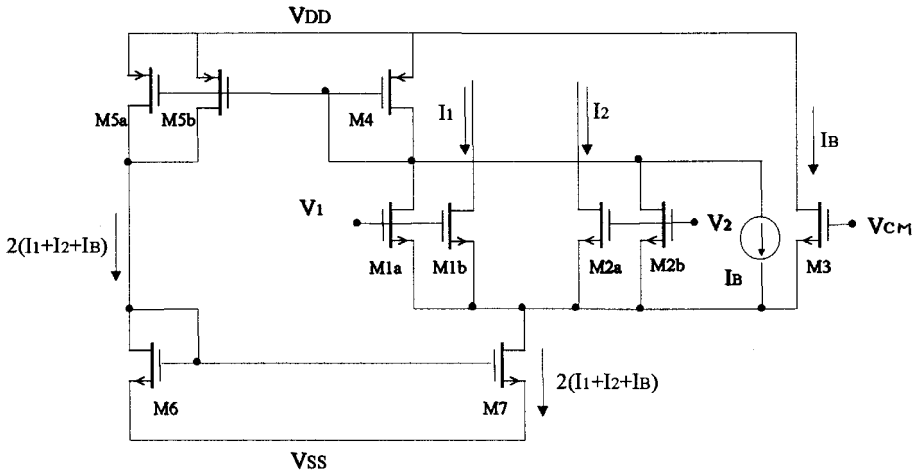

Figure 2. The complete circuit of the proposed transconductance amplifier.

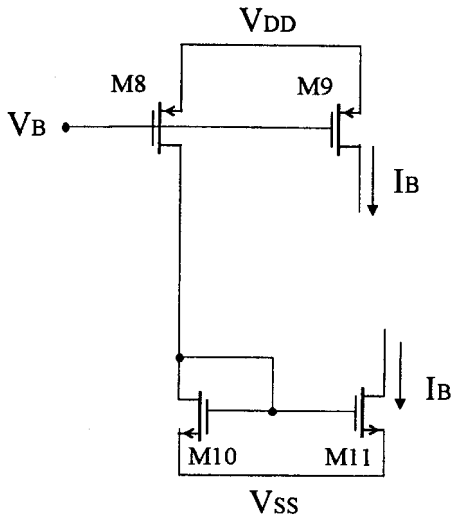

Figure 3. The circuit configuration of the floating current source I_B.

$$I_{OUT} = I_1 - I_2 = \frac{K_n}{2}(V_1 - V_S - V_T)^2 - \frac{K_n}{2}(V_2 - V_S - V_T)^2 \tag{3}$$

where K_n is the transconductance parameters of M1a–M2b. In addition, the current I_B flowing in the transistor M3 is given by

$$I_B = \frac{K_{n1}}{2}(V_{CM} - V_S - V_T)^2 \tag{4}$$

where K_{n1} is the transconductance parameter of the transistor M3. Substituting for V_S in (3) and using square law identity, one obtains

$$I_{OUT} = K_n(V_1 - V_2)\left[\frac{V_1 + V_2}{2} - \left(V_{CM} - V_T - \sqrt{\frac{2I_B}{K_{n1}}}\right) - V_T\right] \tag{5}$$

In order to obtain a linear transconductance circuit, the voltage V_{CM} should be adjusted to

$$V_{CM} = \frac{V_1 + V_2}{2} \tag{6}$$

For a fully differential input voltage, V_{CM} is simply a constant voltage that can be applied directly to the gate of M3. Otherwise, another circuit will be needed to estimate the value of V_{CM}. The circuit shown in figure 4 (Ismail *et al.* 1999) is used to estimate the value of V_{CM}. Assuming that the differential pairs M12,M13 and M14,M15 are matched, they carry the same differential voltage since they have the same current tail I_C as well as the same currents in differential pair branches. Therefore, one obtains

$$V_1 - V_{CM} = V_{CM} - V_2 \tag{7}$$

which results in (6). This relation is valid as long as the difference between V_1 and V_2 follows the relation

$$-2\sqrt{\frac{2I_C}{K_{n2}}} < (V_1 - V_2) < 2\sqrt{\frac{2I_C}{K_{n2}}} \tag{8}$$

where K_{n2} is the transconductance parameter of M12,M13,M14 and M15. It is noted that other techniques can be used to estimate the common mode signal. By substituting for V_{CM} in (5), the output current is finally given by

$$I_{OUT} = K_n\sqrt{\frac{2I_B}{K_{n1}}}(V_1 - V_2) \tag{9}$$

It is noted that for M1 and M2 to be on, the linearity range is limited to the value

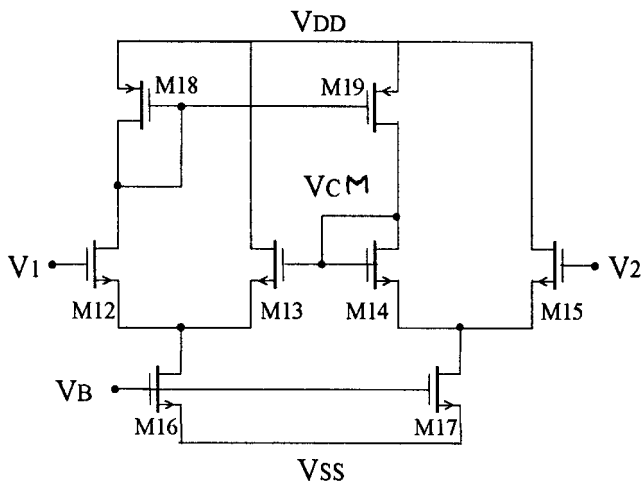

Figure 4. The proposed common-mode estimator circuit.

$$-2\sqrt{\frac{2I_B}{K_{n1}}} < (V_1 - V_2) < 2\sqrt{\frac{2I_B}{K_{n1}}} \tag{10}$$

Therefore, one can set the common mode estimator circuit input range given by equation (8) to equal the linearity range of the transconductor circuit by choosing appropriate values for I_C and K_{n2}. It is noted that the linearity range does not depend on the value of K_n. Therefore, unlike the ordinary long tail differential pair, the linearity range can be kept considerably wide, independent of the chosen value for the transconductance value.

3. Second order effects

The non-idealities represent the basic source of linearity error of the transconductor. The influence of these non-idealities is now investigated.

3.1. *Channel-length modulation*

By multiplying the square law term in equation (1) by the factor $(1 + \lambda V_{DS})$, a second order harmonic distortion is obtained as

$$HD_2 \cong \frac{\lambda}{16}(V_1 - V_2) \tag{11}$$

where λ is the channel length modulation parameter. This effect can be kept small by choosing transistors with long channels.

3.2. *Mobility reduction*

Owing to the vertical surface electric field, the μ factor in equation (2) is given by $\mu_n = \mu_o/[1 + \theta(V_{GS} - V_T)]$ where μ_o is the zero field mobility of carriers and θ is a constant. Seevinck and Wassenaar (1987) have shown that this effect can be modelled as a source series resistance with value $R_S = \theta/K_n$. Accordingly, the result is a third order harmonic distortion of value

$$HD_3 = \frac{\theta(V_1 - V_2)^2}{32\sqrt{(2I_B/K_{n1})}} \tag{12}$$

Compared with the values reported in Babanezhad and Temes (1985), Seevinck and Wassenaar (1987) and Wang and Guggenbuhl (1990) it is clear from equation (12) that the effect of mobility reduction on the linearity is very small. This verifies the analysis in Wilson and Chan (1990, 1991), proving that antiphase common-source pair topologies result in higher linearity ranges and much lower distortion levels when compared with cross coupled pair ones. In addition, there is no contribution for the body effect in distortion. Therefore, the proposed transconductor, as will be shown by simulations, is expected to have a very low distortion level.

4. PSpice simulations

PSpice simulation results for the proposed transconductor were carried out using transistors with aspect ratios as given in table 1 and with ± 2.5 V supply voltages, I_B

Transistor	Aspect ratio $W(\mu m)/L(\mu m)$
M1a,M1b,M2a,M2b	1/2
M3	1/2
M4,M5a,M5b	15/4
M6,M7	5/2
M8,M9	15/4
M10,M11	5/2
M12–M15	1/2
M16,M17	5/2
M18,M19	15/4

Table 1. The W/L of the transistors of the circuits shown in figures 2, 3 and 4.

of 30 μA and a 0.5 μm MIETEC CMOS process. The model parameter set of 0.5 μm CMOS Technology is given in table 2.

Figure 5 represents the I–V characteristics of the proposed transconductor. The balanced-input (V_1-V_2) is scanned from −1 V to +1 V for different values of I_B. Figure 6 represents the simulated linearity error of the transconductance value with respect to the input voltage. It is clear that the linearity error is less than 0.5% over a considerable operating range. Figure 7 shows the THD of the output current of the proposed transconductor and the ordinary LTP transconductor versus input voltage magnitude at 100 kHz. The ordinary LTP transconductor has been chosen such that its linearity range was approximately the same as the proposed circuit. This is realized by adjusting its I_{SS}/K ratio to 16 times the value of the I_B/K_n ratio chosen for the proposed circuit, where I_{SS} is the current tail of the ordinary LTP and K is the transconductance parameter of the differential pair transistors. This choice, of course, is done only for simulation purposes since the common mode operating range for LTP transconductor will be then limited. Simulation results show that the distortion level in the proposed transconductor when compared with the LTP transconductor is very low, which verifies the analysis in the previous

.MODEL NMNMOS LEVEL = 3
+UO = 460.5 TOX = 1.0E-8TPG = 1 VTO = 0.62 JS = 1.08E-6
+XJ = 0.15URS = 417 RSH = 2.73LD = 0.04U VMAX = 130E3
+NSUB = 1.71E17 PB = 0.761 ETA = 0.00 THETA = 0.129 PHI = 0.905
+GAMMA = 0.69 KAPPA = 0.10 CJ = 76.4E-5 MJ = 0.357 CJSW = 5.68E-10
+MJSW = 0.302 CGSO = 1.38E-10 CGDO = 1.38E-10 CGBO = 3.45E-10
+KF = 3.07E-28 AF = 1WD = +0.11U DELTA = +0.42 NFS = 1.2E11
+DELL = 0U LIS = 2ISTMP = 10
.MODEL PM PMOS LEVEL = 3
+UO = 100 TOX = 1.0E-8 TPG = 1VTO = −0.58JS = 0.38E-6XJ = 0.10U
+RS = 886 RSH = 1.81 LD = 0.03U VMAX = 113E3 NSUB = 2.08E17 + PB
= 0.911 ETA = 0.00 THETA = 0.120 PHI = 0.905 GAMMA = 0.76
+KAPPA = 2 CJ = 85E-5 MJ = 0.429 CJSW = 4.67E-10 MJSW = 0.631
+CGSO = 1.38E-10 CGDO – 1.38E-10 CGDO = 3.45E-10KF = 1.08E-29
+AF = 1 WD = +0.14U DELTA = 0.81 NFS = 0.52E11
+DELL = 0U LIS = 2 ISTMP = 10

Table 2. The model parameters set of 0.5 μm CMOS technology (obtained through MIETEC).

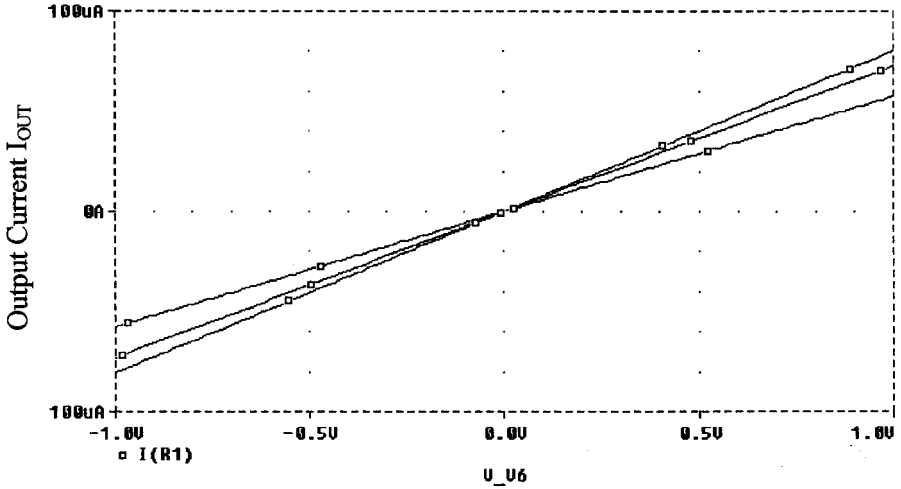

Figure 5. The *I–V* characteristics of the proposed transconductance amplifier for different values of the control current.

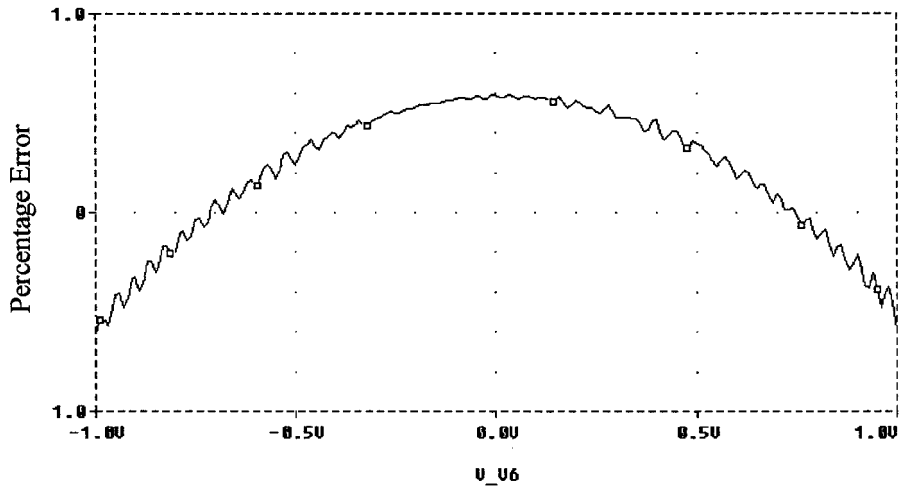

Figure 6. The linearity error in the transconductance value vs. the input voltage.

section. Simulation results also show that mismatches between basic transistors M1 and M2 in the current-controlled transconductor produce harmonic distortion and offset of the transfer characteristics. When mismatch increases to 5%, 10% and 25% the THD increases to 0.16%, 0.2% and 0.28% respectively at 100 kHz for a balanced input of 1 V_{p-p}.

5. Conclusions

A new low-distortion transconductor circuit has been proposed. The advantages of this new transconductor have been discussed. The simulated performances have also been presented. It has been shown that this multiplier gives a great linearity range and an excellent performance that makes it very suitable for analogue signal processing.

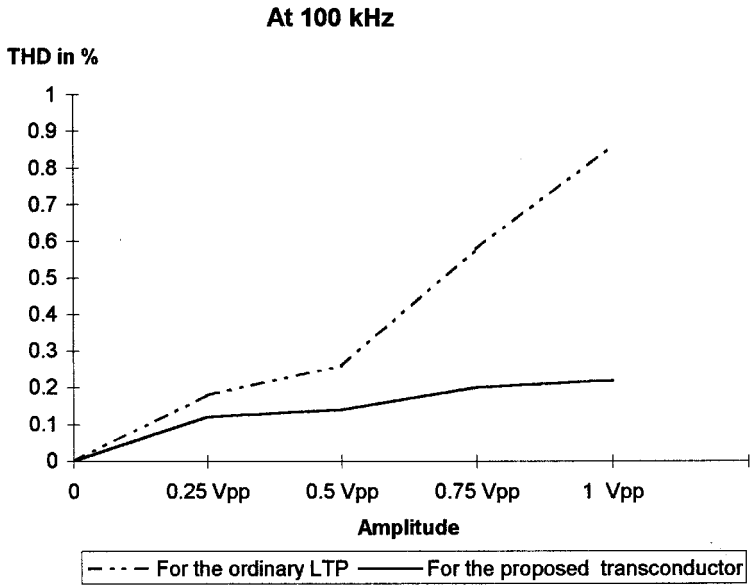

Figure 7. THD of the output current of the proposed transconductor and the ordinary LTP transconductor vs. input voltage magnitude at 100 kHz.

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