REFERENCES

[1] A. Lepschy, G. Mian, and U. Viaro, "Model reduction for control systems with restricted complexity controllers," *J. Franklin Inst.*, vol. 319, pp. 559–567, 1985.

[2] D. Xue and D. Atherton, "An optimal model reduction method for closed loop systems," in *Proc. 30th Conf. Decision Contr.*, Brighton, England, 1991, pp. 2729–2730.

[3] O. Perron, *Die Lehre von den Kettenbrüchen.* Stuttgart, Germany: Teubner, 1913, 3rd ed., 1957 (in German).

[4] K. Glover, J. Lam, and J. Partington, "Balanced realizations and Hankel-norm approximation of systems involving delays," in *Proc. 25th Conf. Decision Contr.*, Athens, Greece, 1986.

[5] K. Glover, J. Lam, and J. Partington, "Rational approximation of a class of infinite-dimensional systems," Tech. Rep. CUED/F-INFENG/TR.20, Eng. Dept., Cambridge Univ., 1988.

[6] C. Glader, G. Högnäs, P. M. Mäkilä, and H. T. Toivonen, "Approximation of delay systems—a case study," *Int. J. Contr.*, vol. 53, pp. 369–390, 1991.

[7] J. Lam, "Balanced realization of Padé approximants of e^{-sT}," *IEEE Trans. Automat. Contr.*, vol. 36, pp. 1096–1100, 1991.

[8] L. T. Pillage and R. A. Rohrer, "Asymptotic waveform evaluation for timing analysis," *IEEE Trans. Computer-Aided Design*, vol. 9, pp. 357–366, 1991.

Low-Voltage Low-Power CMOS Current Conveyors

Hassan O. Elwan and Ahmed M. Soliman

***Abstract*—New CMOS rail to rail second generation current conveyor circuits are proposed. First a class A current conveyor circuit which operates from a single supply of 1.5 V with a rail to rail voltage swing capability is given. The circuit is then modified to work as a class AB while maintaining the rail to rail swing capability. The class AB circuit works from supply voltages down to +1.1 V with standby current of 56 μA. These new current conveyor realizations are insensitive to the threshold voltage variation caused by the body effect, which minimizes the layout area and makes both circuits a valuable addition to the analog VLSI libraries. PSpice simulation confirms the attractive properties of the proposed circuits.**

***Index Terms*—Current conveyors.**

I. INTRODUCTION

Recently the demand for ever smaller and cheaper electronic systems has led manufacturers to integrate entire systems on a single chip, therefore systems employing digital and analog circuits on the same chip are common [1]. Analog cells used with digital systems must operate from low voltage and dissipate as little power as possible. The main reason behind this requirement is the large number of digital gates employed in most of today's integrated circuits applications. The more gates integrated, the more important it is to reduce the power consumption. Therefore a low supply voltage is required to decrease the power consumption of the digital portion of the chip enabling more functions to be integrated. Op amps operating from low supply voltages have been proposed [2]. These op amps require complicated input stages to guarantee a rail to rail input common mode operation while maintaining a constant transconductance, this is important to allow optimal frequency compensation. The use of compensating capacitors results in a finite gain bandwidth product for the op amp hence the bandwidth is not utilized effectively for higher gain values. Recently, current mode circuits have been receiving significant attention in analog signal processing [3], [4]. A useful block for high frequency current mode applications is the second generation current conveyor (CCII) proposed by Sedra and Smith [5]. Although CMOS realizations of the CCII are available, they usually operate in a class A mode with a limited voltage swing capability [6], [7].

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TABLE I

```
.MODEL NENH NMOS LEVEL=2 LD=0.250000U TOX=408.000001E-10
+ NSUB=6.264661E+15 VTO=0.77527 KP=5.518000E-05 GAMMA=0.5388
+ PHI=0.6 UO=652 UEXP=0.100942 UCRIT=93790.5 DELTA=1.000000E-06
+ VMAX=100000 XJ=0.250000U LAMBDA=2.752568E-03 NFS=2.06E+11 NEFF=1
+ NSS=1.000000E+10 TPG=1.000000 + RSH=31.020000 CGDO=3.173845E-10
+ CGSO=3.173845E-10 CGBO=4.260832E-10 CJ=1.038500E-04 MJ=0.649379
+ CJSW=4.743300E-10 MJSW=0.326991 PB=0.800000

.MODEL PENH PMOS LEVEL=2 LD=0.213695U TOX=408.000001E-10
+ NSUB=5.574486E+15 VTO=-0.77048 KP=2.226000E-05 GAMMA=0.5083
+ PHI=0.6 UO=263.253 UEXP=0.169026 UCRIT=23491.2 DELTA=7.31456
+ VMAX=17079.4 XJ=0.250000U LAMBDA=1.41E-02 NFS=2.77E+11 NEFF=1.001
+ NSS=1.000000E+10 TPG=-1.000000 + RSH=88.940000 CGDO=2.712940E-10
+ CGSO=2.712940E-10 CGBO=3.651103E-10 + CJ=2.375000E-04 MJ=0.532556
+ CJSW=2.707600E-10 MJSW=0.252466 PB=0.800000
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In this brief new CMOS CCII circuits operating from low supply voltages with a rail to rail swing capability are proposed. The first CCII circuit operates from a single supply voltage of 1.5 V in a class A mode. The second proposed CCII circuit operates in a class AB mode with a rail to rail voltage swing and a low standby current. PSpice simulations based on the SCN 2 level-2 parameters obtained through MOSIS are presented. The SPICE model parameters are listed in Table I.

II. THE CLASS A CCII CIRCUIT

The proposed class A current conveyor circuit is shown in Fig. 1, where two differential pairs are used to provide a rail to rail operation at the Y and the X terminals. Transistors M1 and M4 conduct till the positive supply rail, while transistors M2 and M3 conduct for signal swing down to the negative supply rail. By the current mirroring action of transistors M5, M6 and M7, M8 the currents are summed at the drains of transistors M1 and M4 as shown in Fig. 1. Transistors M9 and M10 force these currents to be equal and hence $V_x = V_y$. To provide a low impedance at the X terminal a suitable buffer circuit should be used. It is worth noting that the traditional source follower which has been used in [7] is not suitable since it will not provide a rail to rail swing capability. In the proposed circuit transistors M11 and M14 provide the necessary buffering action with a rail to rail swing capability. The X terminal current is then mirrored to the Z terminal by the action of transistors M12 and M15.

It is worth noting that the circuit operation is insensitive to the threshold voltage variation due to the body effect, since transistors M1, M4 and M2, M3 have the same source voltages, their threshold voltages cancel out. On the other hand, since transistors M5 to M16 have their sources connected to one of the two supply rails, they exhibt no body effect. This independence of the body effect allows the circuit to be implemented effectively on any standard CMOS process.

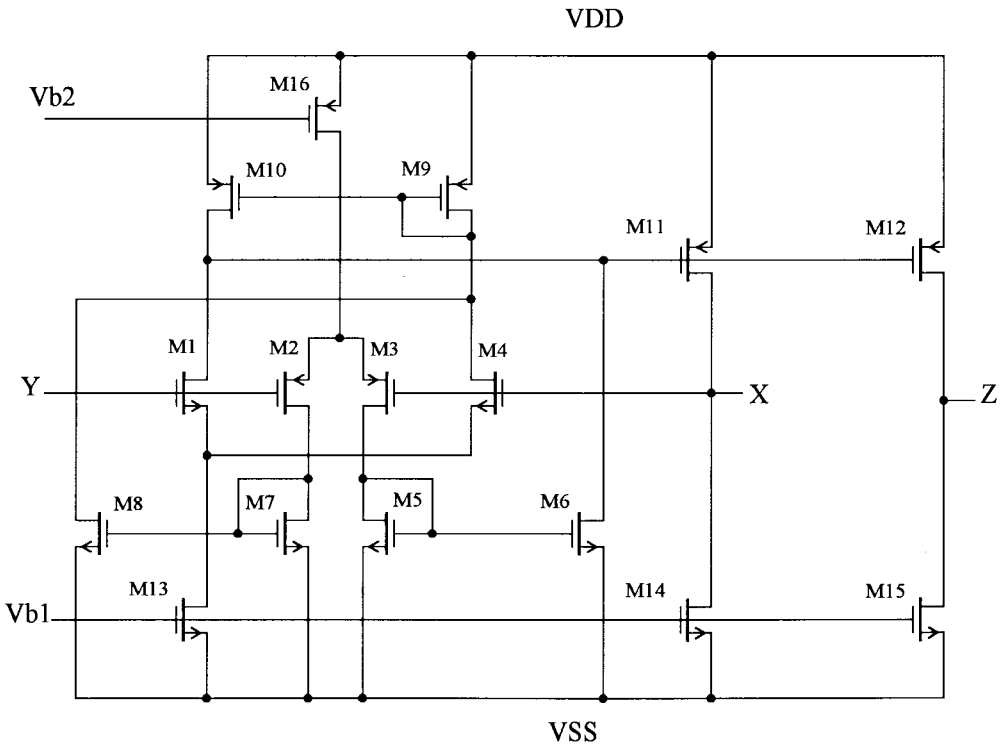


Fig. 1. The class A current conveyor circuit.

TABLE II

Transistor	Aspect ratio (W/L)
M1,M4	20/4
M2,M3	30/4
M5,M6,M7,M8	20/4
M9,M10	40/4
M11,M12	220/4
M14,M15	80/4

PSpice simulations of the class A CCII circuit with the transistors aspect ratios as given in Table II and a single supply voltage of 1.5 V have been carried out. Fig. 2(a) shows the voltage swing at the X and the Z terminal of the CCII cell of Fig. 1 when used to realize a voltage amplifier of gain two. The values of the grounded resistors used at the X terminal and the Z terminal are 10 KΩ and 20 KΩ respectively. The frequency response of the amplifier is shown in Fig. 2(b). Small signal simulation results indicate an output resistance of 27 Ω at the X terminal and a voltage gain of 0.996 between the Y and the X terminals indicating an error of 0.4%.

III. The Class AB CCII Circuit

Although the circuit of Fig. 1 operates from a low supply voltage, it withdraws large standby currents. This is due to the class A mode of operation where the constant current sources formed from transistors M14 and M15 result in unnecessary power dissipation in the standby mode. Applications demanding low power dissipation makes it essential to use class AB stages at the X and the Z terminals. Fig. 3 represents the proposed class AB CCII circuit where transistors M15 and M16 form the push pull X terminal output stage. Transistors M13 and M14 are level shifting transistors, providing proper biasing for transistor M15. If current is withdrawn from the X terminal then the gate voltages of transistors M15 and M16 are lowered. Thus the current through transistor M16 increases while that through transistor M15 decreases. Similarly if the X terminal is required to sink current, then the gate voltages of M15 and M16 increase causing the current through transistor M16 to decrease and that through transistor M15 to increase. This push pull action of transistors M15 and M16 help in reducing the power dissipation. To prevent cross-over distortion both transistors M15 and M16 must remain ON when no current is withdrawn from the X terminal (standby), yet this current should be small to decrease the standby power dissipation. This is achieved by using a suitable gate voltage for transistor M13 which sets the voltage level shift between the gates of M15 and M16. In the standby mode, no current is withdrawn from the X terminal, hence M15 and M16 have equal currents. Assuming that both transistors are operating in the saturation region, therefore

$$\sqrt{\frac{2I_{SB}}{K_{16}}} = (V_{DD} - V_{G16} - |V_{TP}|) \tag{1}$$

and

$$\sqrt{\frac{2I_{SB}}{K_{15}}} = (V_{G15} - V_{SS} - V_{Tn}). \tag{2}$$

Adding the above two equations, thus

$$I_{SB} = \tfrac{1}{2} K_{\text{eff}1}[(V_{DD} - V_{SS}) - (V_{G16} - V_{G15}) - V_{Tn} - |V_{TP}|]^2 \tag{3}$$

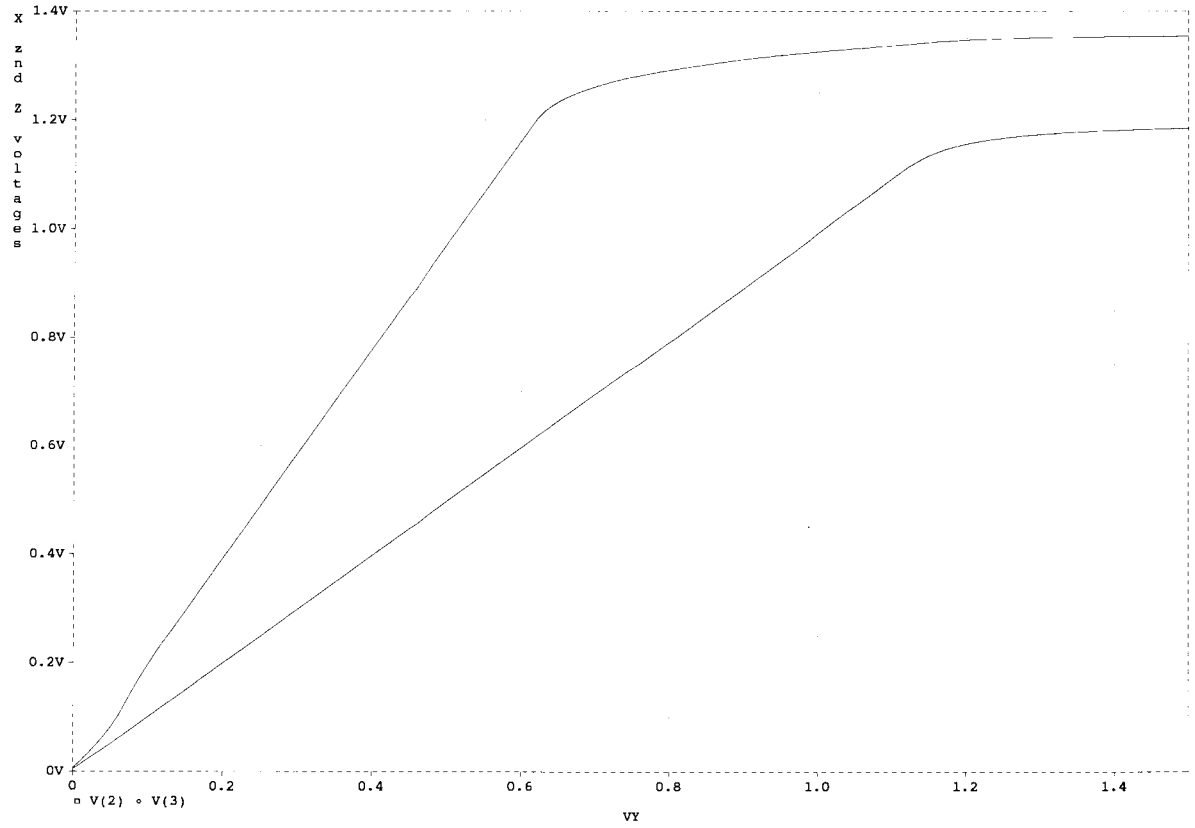
where

$$K_{\text{eff}1} = \frac{K_{15}K_{16}}{(\sqrt{K_{15}} + \sqrt{K_{16}})^2}. \tag{4}$$

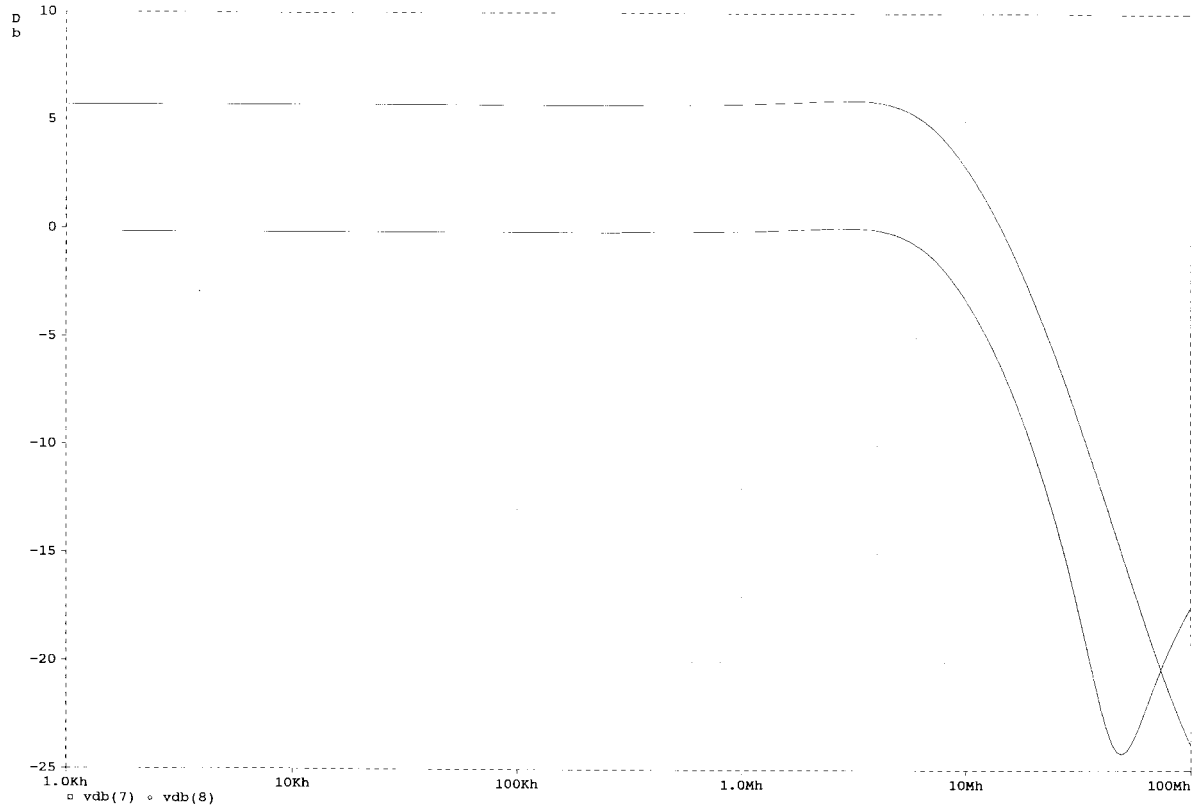
Since the two matched transistors M13 and M14 have equal currents the voltage level shift between the gates of M15 and M16 is given by

$$V_{G16} - V_{G15} = V_B - V_{SS} \tag{5}$$

where VB is the biasing voltage applied to the gate of M13.



(a)



(b)

Fig. 2. (a) The X terminal and the Z terminal voltages when the CCII circuit of Fig. 1 is used to realize an amplifier with gain 2. (b) The frequency response of the CCII based amplifier.

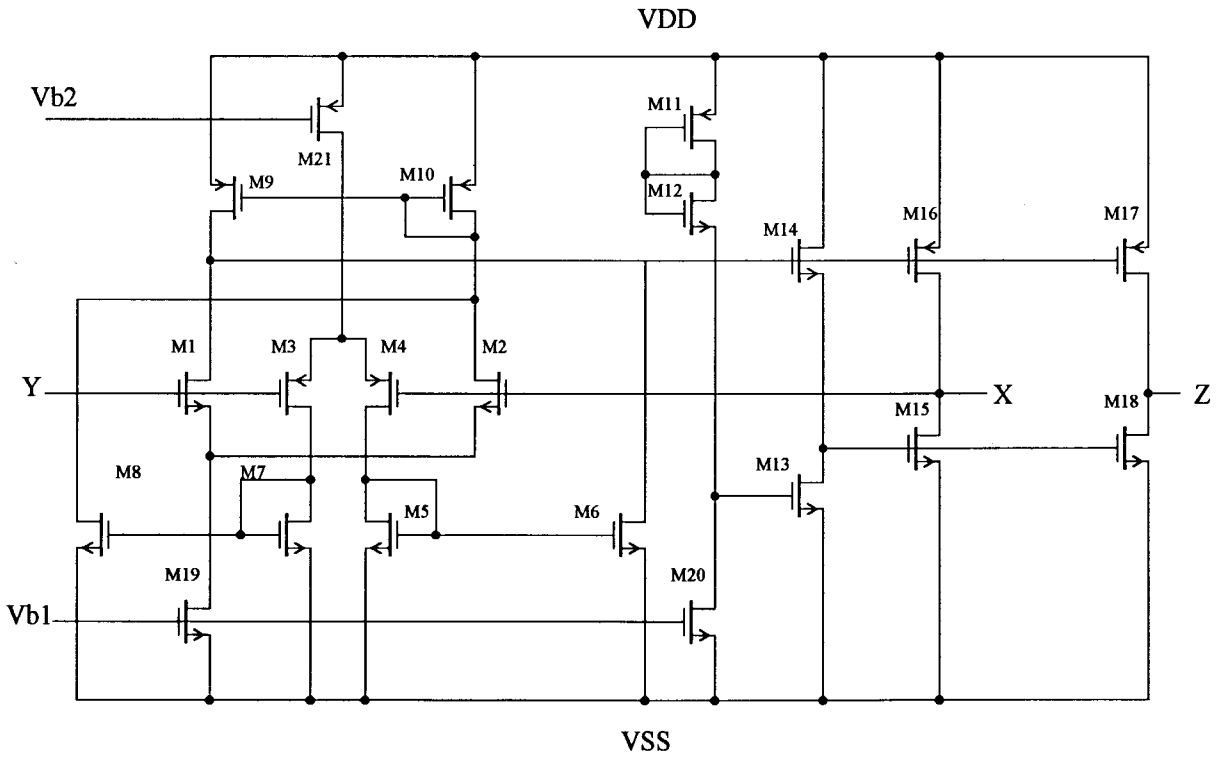


Fig. 3. The class AB current conveyor circuit.

TABLE III

Transistor	Aspect ratio (W/L)
M1,M2	20/4
M3,M4	30/4
M5,M6,M7,M8	20/4
M9,M10	40/4
M11,M16,M17	200/4
M12,M15,M18	90/4
M13,M14	4/4

From (3) and (5), the standby current is given by

$$I_{SB} = \tfrac{1}{2} K_{\text{eff}1}(V_{DD} - V_B - V_{T_n} - |V_{T_P}|)^2. \tag{6}$$

The biasing voltage VB obtained from the biasing circuit formed from M11, M12 and the current source I_b formed from M20 is given by

$$V_B = V_{DD} - V_{T_n} - |V_{T_P}| - \sqrt{\frac{2I_b}{K_{\text{eff}2}}} \tag{7}$$

and

$$K_{\text{eff}2} = \frac{K_{11}K_{12}}{(\sqrt{K_{11}} + \sqrt{K_{12}})^2}. \tag{8}$$

From (6) and (7), therefore

$$I_{SB} = \frac{K_{\text{eff}1}}{K_{\text{eff}2}} I_b. \tag{9}$$

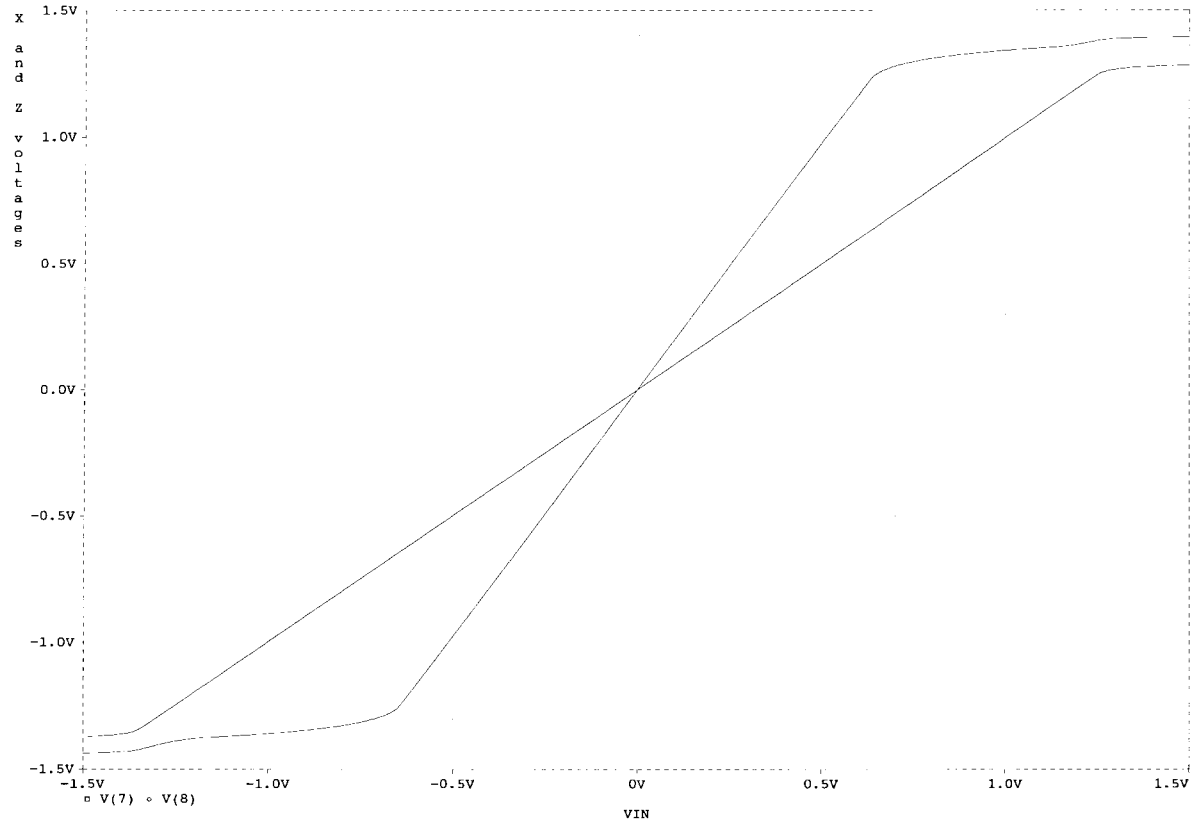
It is seen that the standby current can be controlled by the biasing current source and the aspect ratios of the appropriate transistors. Transistors M17 and M18 convey the current from the X terminal to the Z terminal.

PSpice simulations of the class AB circuit with the transistors aspect ratios as given in Table III and supply voltages of ± 1.5 V have been carried out.

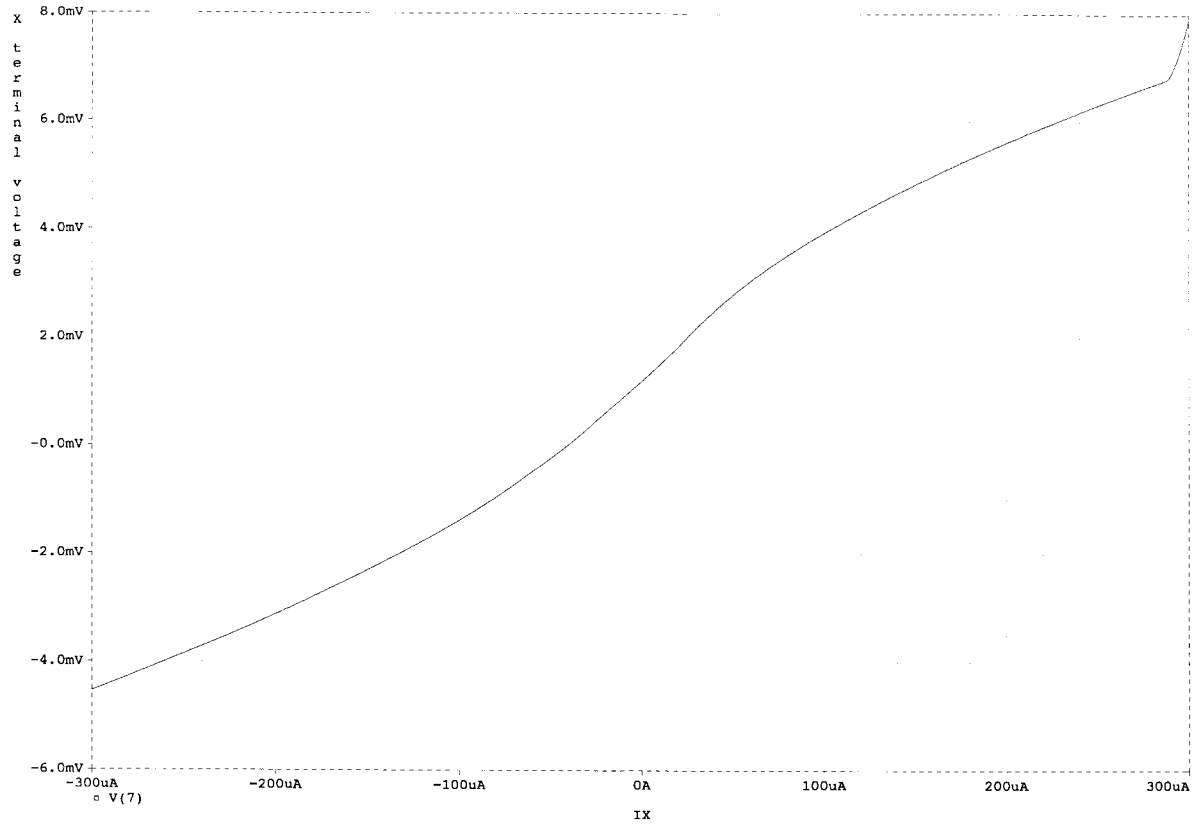
Fig. 4(a) shows the voltage swing at the X and the Z terminals of the class AB CCII circuit, when used to realize a voltage amplifier of gain two. The values of the grounded resistors used at the X terminal and the Z terminal are 10 and 20 KΩ, respectively. The biasing currents through transistors M19, M20, and M21 are adjusted to 6 μA.

Fig. 4(b) shows the X terminal voltage offset variation versus the current I_X, with the Y terminal being grounded. The variation of the X terminal offset voltage versus the biasing current I_b is shown in Fig. 4(c). Fig. 4(d) shows the currents through the output transistors M15 and M16 indicating the push pull action. The supply current is less than 56 μA and the X terminal output resistance is 29 Ω. PSpice simulations indicate that the circuit can function from supply voltages as low as ± 1.1 V with a reduced current driving capability. It is worth noting that all PSpice simulations have been carried out with the source of each transistor connected to the appropriate supply rail which reflects the fact that all transistors are in the same well. Although the body effect causes no distortion in the class AB circuit it results in a standby current which is dependent on the supply voltage. Equation (9) assumes that the threshold voltages of the NMOS transistors M13, M14 and M12, M15 are equal. The sources of the NMOS transistors M12 and M14 are not connected to the negative supply rail, hence the threshold voltages of transistors M12, M15 and M13, M14 are not equal. Since the mismatch in the threshold voltages is in the biasing circuit, it causes no distortion. However, this mismatch results in a standby current which is dependent on the supply voltage.

Fig. 5(a) shows the variation of the standby current versus the supply voltage for different values of I_b. This simulation has been carried out with the body of all transistors connected to the appropriate supply voltage.

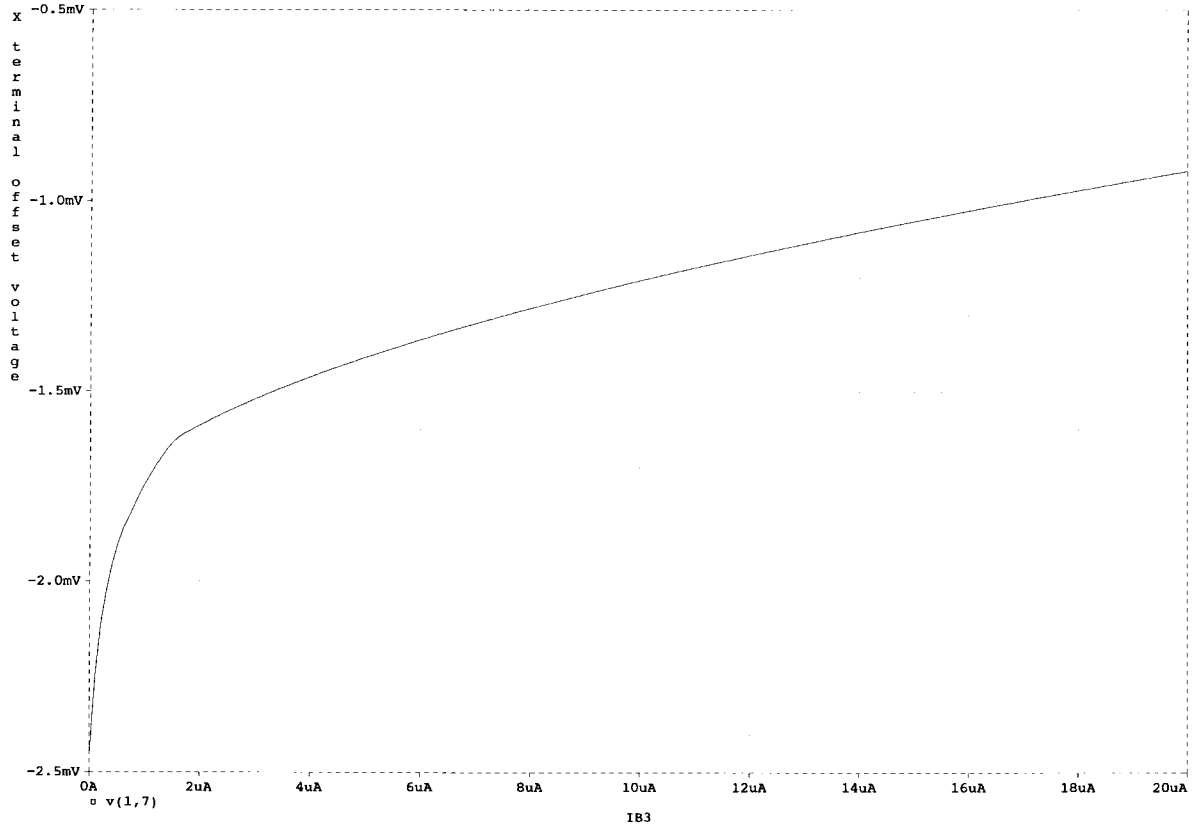


(a)

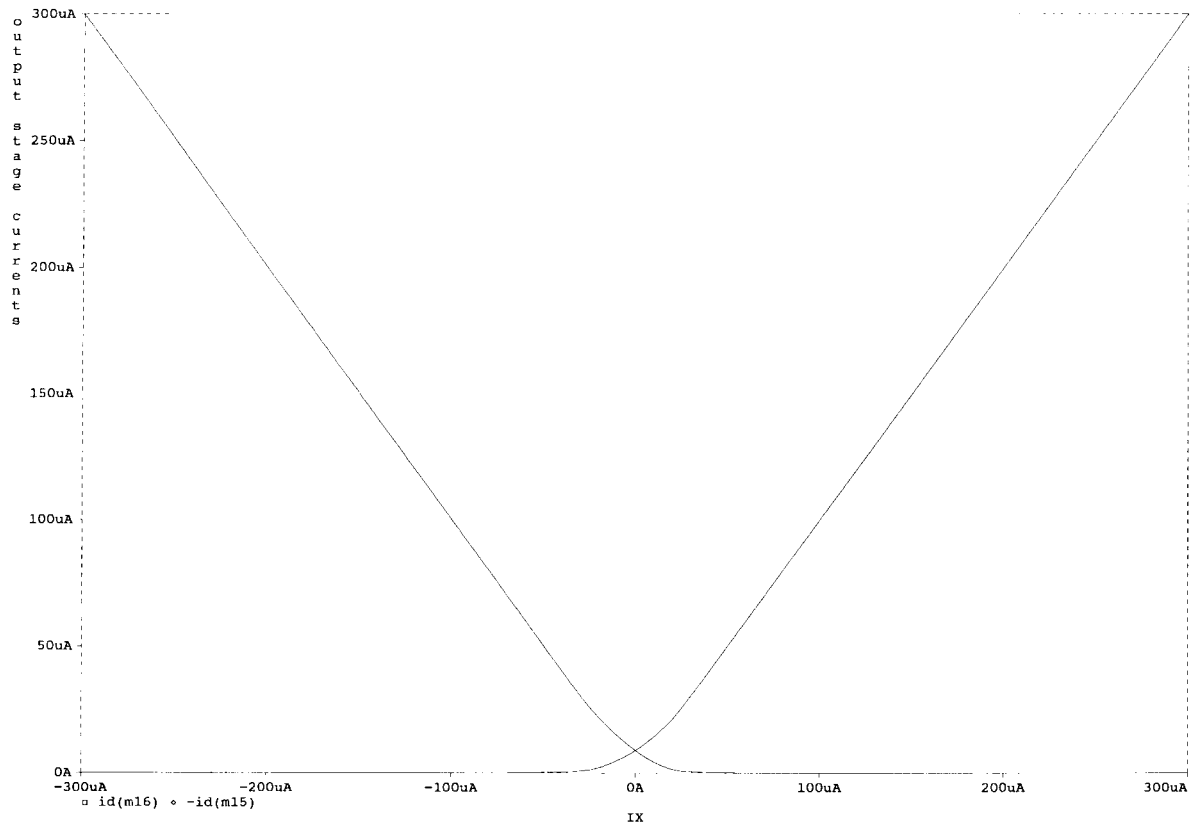


(b)

Fig. 4. (a) The X terminal and the Z terminal voltages when the CCII cell of Fig. 3 is used to realize an amplifier with gain 2. (b) The X terminal voltage offset variation versus the current I_X.

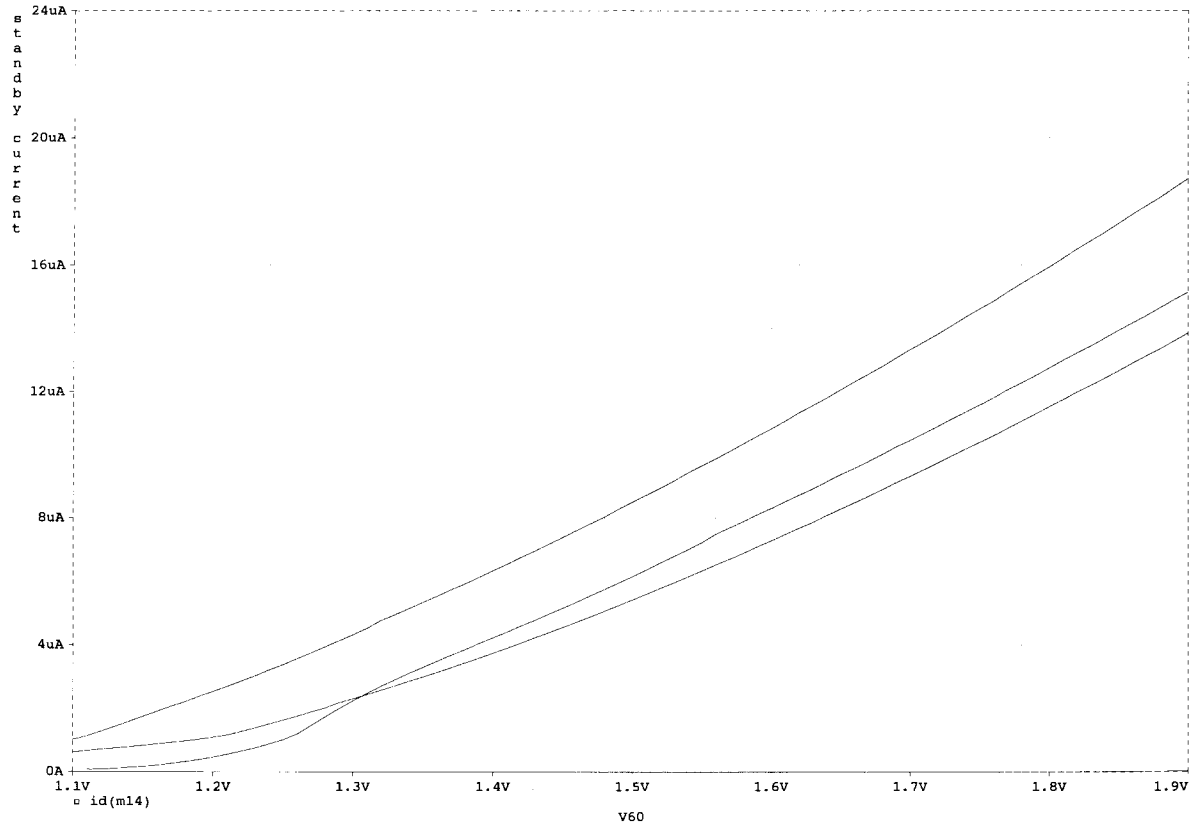


(c)

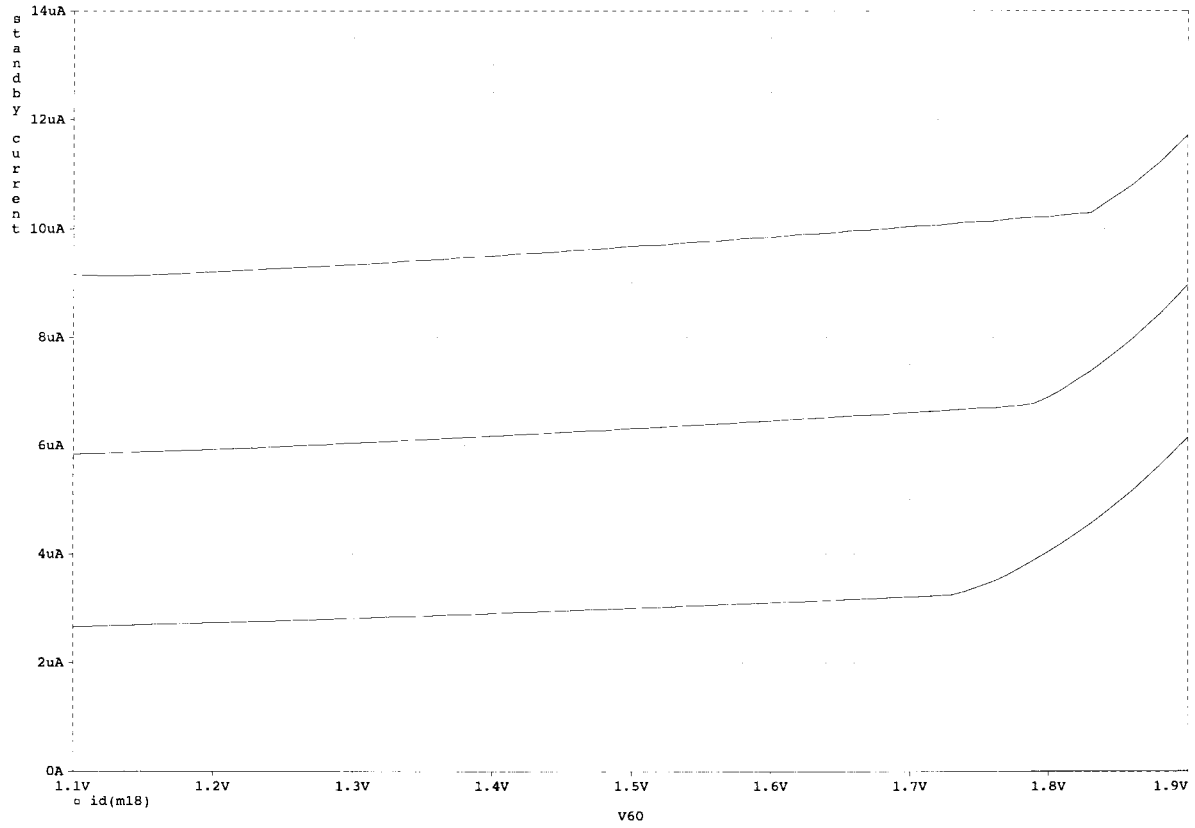


(d)

Fig. 4. *(Continued.)* (c) The variation of the X terminal offset voltage versus the biasing current I_b. (d) The currents through transistors M15 and M16 (push-pull action).



(a)



(b)

Fig. 5. (a) The standby current variation versus the supply voltages when all transistors are in the same well. (b) The standby current variation versus the supply voltages when transistors M12 and M14 are isolated in two P-wells.

Fig. 5(b) shows the variation of the standby current versus the supply voltage when the sources of transistors M12 and M14 are connected to the body. This can be easily achieved in any standard P-well CMOS process.

IV. Conclusion

New CMOS CCII realizations are given. The proposed circuits provide a rail to rail swinging capability with excellent linearity. The class A circuit operates from a single supply voltage of 1.5 V, while the class AB circuit operates from supply voltages as low as ± 1.1 V with small standby current. Since the proposed circuits require no compensating capacitors, they have a wide bandwidth which is independent of the gain. The operation of the given circuits is insensitive to the threshold voltage variation resulting from the body effect. PSpice simulations based on level-2 parameters obtained through MOSIS are in excellent agreement with the expected results.

References

[1] S. Kawada, Y. Hara, T. Isono, and T. Inuzuka, "1.5-μm CMOS gate arrays with analog/digital macros designed using common base arrays," *IEEE J. Solid-State Circuits*, vol. 24, pp. 985–990, Aug. 1989.

[2] R. HogerVost, R. J. Wiegerink, P. A. L. de Jong, J. Fonderie, R. F. Wassenaar, and J. H. Huijsing, "CMOS low-voltage operational amplifiers with constant gm rail-to-rail input stage," in *Proc. IEEE Int. Symp. Circuits Syst.*, May 1992, pp. 2876–2879.

[3] C. Toumazou, J. Lidgey, and A. Payne, "Emerging techniques for high frequency BJT amplifier design," in *The First Int. Conf. Electron. Circuits Syst.*, Cairo, Egypt, Dec. 1994.

[4] B. Wilson, "Recent developments in current conveyors and current-mode circuits," *Proc. Inst. Elect. Eng.*, vol. 137, pp. 63–77, Apr. 1990.

[5] A. Sedra and K. C. Smith, "A second generation current conveyor and its applications," *IEEE Trans. Circuit Theory*, vol. CT-17, pp. 132–134, Feb. 1970.

[6] M. C. H. Cheng and C. Toumazou, "3 V MOS current conveyor cell for VLSI technology," *Electron. Lett.*, vol. 29, pp. 317–319, Feb. 1993.

[7] W. Surakampontorn, V. Riewruja, K. Kumwachara, and K. Dejhan, "Accurate CMOS based current conveyors," *IEEE Trans. Instrum. Meas.*, vol. 40, pp. 699–702, Aug. 1991.

A New Approach to Design Cellular Neural Networks for Associative Memories

Giuseppe Grassi

***Abstract*— In this brief, a synthesis procedure of cellular neural networks for associative memories is presented. The proposed method, by assuring the global asymptotic stability of the equilibrium point, generates networks where the input data are fed via external inputs rather than initial conditions. This new approach enables to design both heteroassociative and autoassociative memories and reveals particularly suitable for VLSI implementation techniques.**

***Index Terms*— Associative memories, cellular neural networks, design methods, neural circuits.**

I. Introduction

Very recently, a new idea regarding an analogic array computer, called cellular neural network (CNN) universal machine, has been introduced [1]. The importance of the universal machine is related to its ability to implement any CNN application and has led to a hardware realization in the form of a CNN universal chip [2]. As a consequence, many researchers have focused their attention on VLSI-oriented design methods of CNN's for image processing, pattern recognition and associative memories [3]–[6].

When designing CNN's to perform any task, it is always of interest to study the stability properties of the network [7]. In particular, some studies have been devoted to find the conditions which assure the asymptotic stability of the equilibrium points as well as those which assure that each network trajectory converges to an equilibrium point. In these cases, the input data are fed via initial conditions and the outputs reach their steady state values at an equilibrium point which depends on the initial conditions. As regard with the design of CNN's for associative memories, all the methods developed until now follow the abovementioned theoretical approach. In particular, these methods are based on singular value decomposition techniques [5], on iterative algorithms [6] or on pseudo-inverse matrices [8] and enable to design autoassociative memories only.

Differently from the above mentioned approach, the idea underlying this brief is to design a CNN where the input data are fed via external inputs and each trajectory converges to a unique equilibrium point which depends only on the input and not on the initial state. These networks define a nonlinear mapping from the space of external inputs to the space of steady state outputs, which can be exploited for the design of both heteroassociative and autoassociative memories. This new approach reveals particularly suitable for CNN's running in real time [7] and, consequently, represents a tool which can be exploited for the CNN universal chip.

The brief is organized as follows. In Section II, a CNN model suitable for associative memories is presented, whereas in Section III, some results which assure the global asymptotic stability of the equilibrium point are reported. In Section IV, a synthesis procedure is developed, which assures the CNN stability properties via a suitable choice of the interconnection matrix. Finally, in Section V, some

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