Novel CMOS differential voltage current conveyor and its applications

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Abstract: Novel CMOS realisations of a differential voltage current conveyor (DVCC) are described. These circuits are powerful building blocks, especially for applications demanding differential or floating inputs like impedance converter circuits and current mode instrumentation amplifiers. Applications suitable for VLSI are then considered by using the DVCC to realise a MOS transconductor and a continuous-time current mode MOSFET-C filter. PSpice simulations indicate the excellent performance of the proposed DVCC and of its circuit applications.

1 Introduction

The differential voltage current conveyor (DVCC) is an extension of the second-generation current conveyor (CCII) introduced by Sedra and Smith [1]. Recently, the CCII has been realised using MOS transistors, with the intention to integrate the different CCII circuit applications on one chip [2, 3]. The CCII proves to be a versatile building block that can be used to implement a variety of high-performance circuits which are simple to construct. The CCII has a disadvantage that only one of the input terminals has a high input impedance (the Y terminal). This disadvantage becomes evident when the CCII is required to handle differential signals, as in the case of an instrumentation amplifier. The design of such an amplifier requires two or more CCIIs. A basic section used in realising floating input applications from CCIIs is given in [4]. Using such a circuit to realise an instrumentation amplifier results in an amplifier structure that has the advantage of a high CMRR (even at high frequencies) without the need for an accurately matched resistor network. The circuit given in [4] uses two CCIIs and a floating resistor to provide floating input handling capability. Moreover, the floating resistor is connected between the X terminals of the two CCIIs. As each X terminal has an output resistance R_x, the effective resistance between the two X terminals is $R + 2R_x$, that is the error caused by the nonzero X terminal resistance is doubled.

In this paper the differential voltage current conveyor (DVCC) building block is proposed. The DVCC is a novel building block specially defined to handle differential signals. The DVCC is a five-port building block which is defined by the following matrix equation:

$$\begin{bmatrix} V_X \\ I_{Y1} \\ I_{Y2} \\ I_{Z1} \\ I_{Z2} \end{bmatrix} = \begin{bmatrix} 0 & 1 & -1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 \\ -1 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_X \\ V_{Y1} \\ V_{Y2} \\ V_{Z1} \\ V_{Z2} \end{bmatrix} \quad (1)$$

The DVCC is a versatile building block for applications demanding floating inputs. Two CMOS realisations of this block are given. One of the proposed circuits is insensitive to the threshold voltage variation caused by the body effect. This minimises the layout area and makes the circuit compatible with standard CMOS processes. The proposed circuits are versatile blocks for implementing differential and floating input circuits. This versatility is demonstrated by realising a number of floating impedance converters and inverters. We use the DVCC to realise a MOS transconductor and a current mode MOSFET-C bandpass filter. It cancels the nonlinear terms of transistors operating in the ohmic region. PSpice simulations, which take the second-order effects like mobility degradation and channel length modulation into account, confirm the attractive properties of the proposed circuits.

2 Differential voltage current conveyor realisation

Our first CMOS realisation of the DVCC is shown in Fig. 1. All transistors operate in the saturation region and the sources are connected to the bulk/substrate. Transistors M17, M18 and M19, M20 shift the inputs Y1 and Y2 so that M1 remains on, therefore,

$$V_{G2} - V_{G1} = V_{Y1} - V_{Y2} \quad (2)$$

The current from transistor M1 is mirrored by M6 and M7 to transistor M2, thus,

$$V_{G1} - V_{S1} = V_{G2} - V_X \quad (3)$$

From eqn. 2 and because $V_{S1} = 0$, therefore,

$$V_X = V_{Y1} - V_{Y2} \quad (4)$$

The negative feedback action of transistors M3 and the bias current of M14 provides the desirable current from the X terminal, without altering the X terminal voltage. This current is mirrored to the Z1 terminal by transis-

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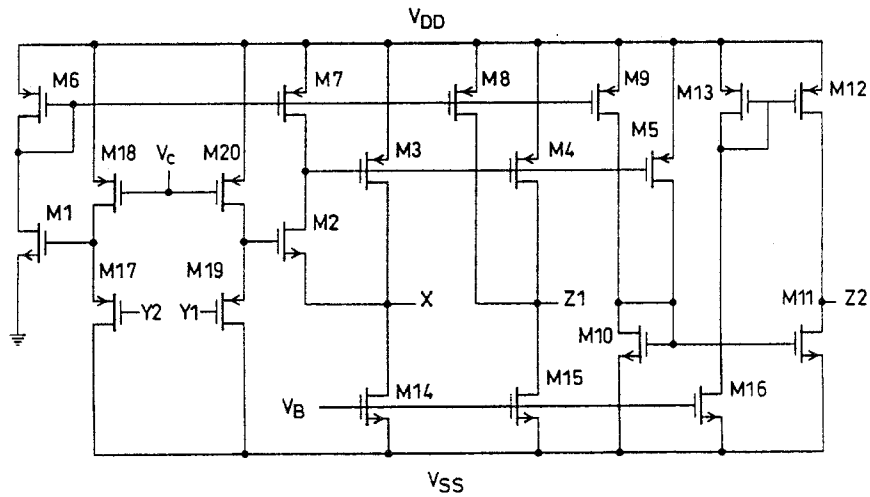

Fig. 1 *CMOS realisation of DVCC*

tors M8, M4 and M15. Current mirrors are used to mirror the current in an inverted form to the Z2 terminal and, hence, both the DVCC+ and DVCC– are realised simultaneously.

In the above analysis, we assumed that the body of the transistor is connected to the source, which is necessary to make the threshold voltage constant for all transistors. This requires a twin well process so that the nMOS and pMOS transistors can be separated in different wells. Although twin-well CMOS technology is available, it is not a standard VLSI technology. Another disadvantage is that the use of separable wells increases the layout area, because every time separable wells are used, guard rings have to surround each well to prevent latch-up.

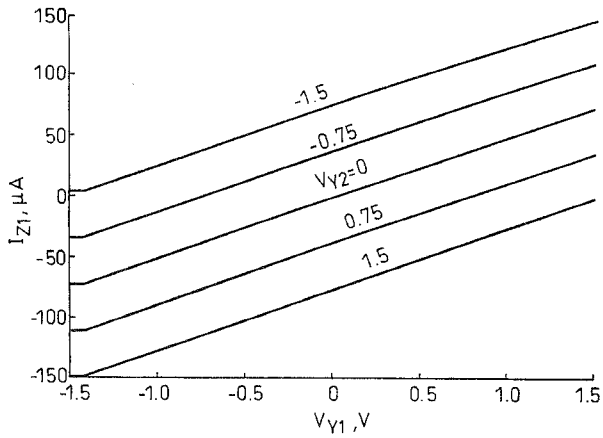

Fig. 2 *Output current against V_{Y1} with V_{Y2} as a parameter*

Fig. 2 shows the output current from the Z1 terminal of the DVCC against the voltage applied to Y1, when a grounded resistor of 20kΩ is connected to the X terminal. The family of curves are for different values of the voltage at Y2. The transistor aspect ratios used are given in Table 1. The supply voltages are ±5V, *Vc* is adjusted to 2.8V and the biasing current used is 380μA. The open-circuit X terminal voltage/frequency response is shown in Fig. 3 and the short-circuit current/frequency response is shown in Fig. 4. The total harmonic distortion is less than 0.25% for a 10kHz, 1V, peak-to-peak sinusoidal input and the terminal X input resistance is less than 10Ω. The SPICE model parameters used in these simulations are of a 2μm SCN process available through MOSIS.

Table 1: Transistor aspect ratios

Transistors	Aspect ratios (W/L)
M1, M2	2/4
M3, M4, M5	52/2
M6, M7, M8, M9	30/2
M10, M11	20/2
M12, M13	30/2
M17, M18, M19, M20	4/4

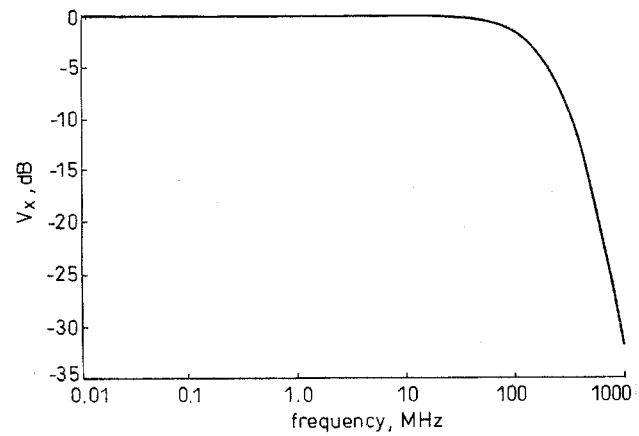

Fig. 3 *X-terminal open-circuit frequency response with $V_{Y1} = 1V$ and $V_{Y2} = 0V$*

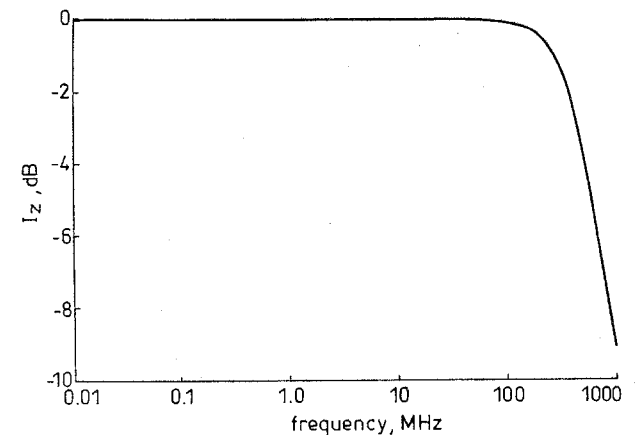

Fig. 4 *Z-terminal short-circuit frequency response where X terminal is driven by current source of 50μA*

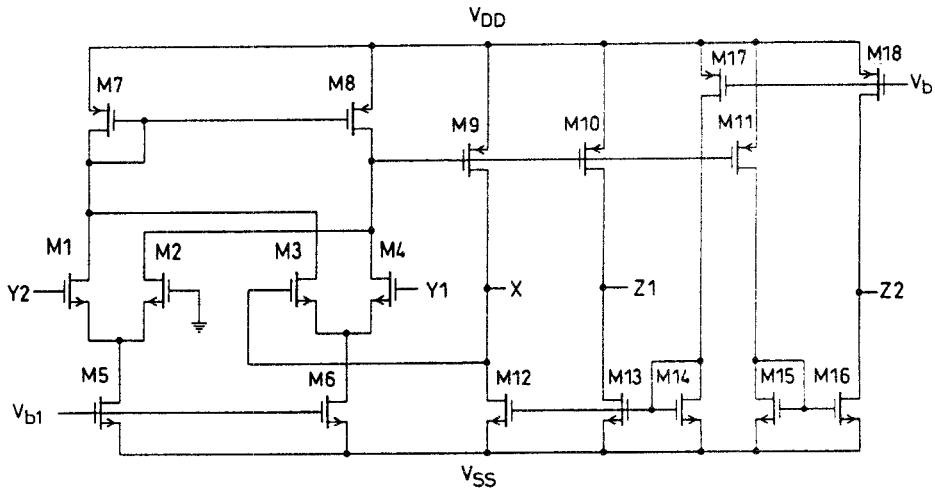

Fig. 5 *DVCC realisation independent of body effect*

3 Body effect independent realisation of CMOS DVCC

Our second DVCC realisation is shown in Fig. 5. The differential voltage conveying action of the circuit is based on the differential pairs M1, M2 and M3, M4. The current mirror formed by transistors M7 and M8 forces the sum of the drain currents of M1 and M3 to be equal to the sum of the drain currents of M2 and M4, hence,

$$I_1 - I_2 = I_4 - I_3 \tag{5}$$

therefore,

$$V_{G_1} - V_{G_2} = V_{G_4} - V_{G_3} \tag{6}$$

$$V_X = V_{Y1} - V_{Y2} \tag{7}$$

Transistors M9 and M12 provide the necessary feedback action to make the voltage V_X independent of the current drawn from the terminal X. It is worth noting that eqn. 7 is valid for large signals. The current through terminal X is conveyed to the Z1 terminal by the current mirrors consisting of transistors M9, M10 and M12, M13. By using extra current mirrors, the current is conveyed in an inverted manner to the Z2 terminal as described before.

The operation of this circuit is insensitive to the threshold voltage variation caused by the body effect. All the pMOS transistors have sources which are connected to the positive supply rail, while all nMOS transistors, except M1, M2, M3 and M4, have sources connected to the negative supply rail. This causes no variation in the threshold voltage because the source to body voltage is maintained equal to zero at all times. Although the sources of transistors M1 and M2 are not connected to the body, their operation is still unaffected by the body effect because they form a differential pair, and, hence, have the same source voltage. This causes equal variation in the threshold voltage of M1 and M2, and, hence, the two threshold voltages cancel out. The same is true for the differential pair transistors M3 and M4. Therefore, the circuit shown in Fig. 5 can be implemented effectively in either n-well or p-well CMOS process.

We performed PSpice simulations of the circuit (shown in Fig. 5) using 1.2μ level-3 model parameters obtained through MOSIS. The aspect ratios of the transistors used in the simulation are given in Table 2. The supply voltages are ±3.3V and the biasing currents through transistors M5, M6 and M17, M18 are adjusted to 60μA and 224μA, respectively. Fig. 6 shows the output currents from the Z1 and Z2 terminals of the DVCC against the voltage applied to Y1, when a grounded resistance of 10kΩ is connected to terminal X. The family of curves are for different values of the voltage at Y2. The frequency response of the output current from the Z1 terminal is shown in Fig. 7. The total harmonic distortion is less than 0.25% for a 1MHz, 1V, peak-to-peak sinusoidal input. It is worth noting that all simulations of the circuit, shown in Fig. 5, have been carried out with the body of each transistor connected to the appropriate supply rail, which reflects the fact that all transistors are in the same well.

Table 2: Transistor aspect ratios

Transistors	Aspect ratios (W/L)
M1, M2, M3, M4	7.2/4.8
M7, M8	39.6/4.8
M9, M10, M11, M17, M18	111.6/3.6
M5, M6, M12, M13, M14, M15, M16	144/4.8

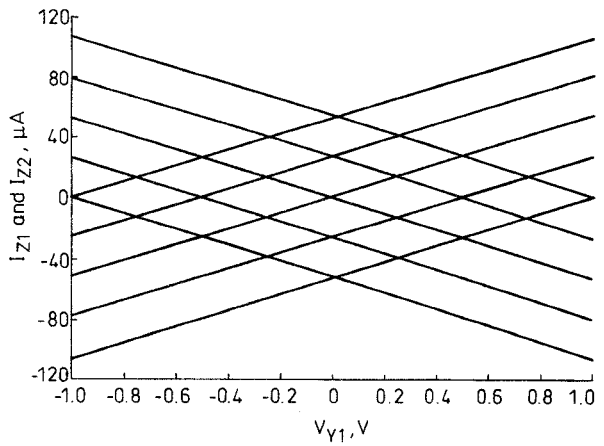

Fig. 6 *Z-terminal output currents of DVCC against Y1 terminal voltage*

3.1 Channel length modulation effect

In the analysis of the preceding Section, we neglected the second-order effects, which causes an offset voltage between the terminals Y1, Y2 and X. This offset

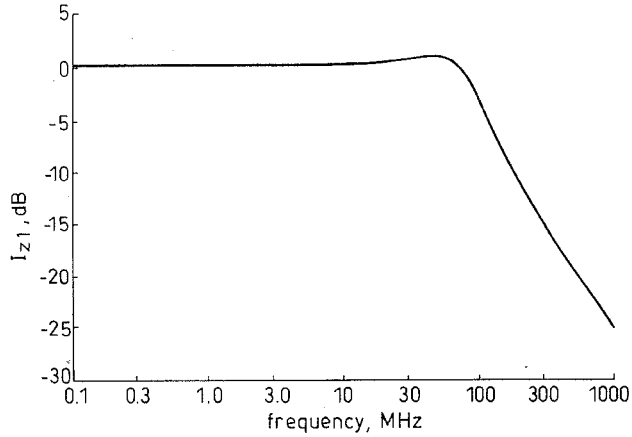

Fig. 7 *Frequency response of Z1 output current*

voltage is mainly due to the channel length modulation effect and can be compensated by an appropriate choice for the transistors' aspect ratios, as will be shown in the following.

The drain current of the pMOS transistor in the saturation region, taking into account the channel length modulation, is

$$I_d = \frac{K}{2}(V_{SG} - |V_{TP}|)^2(1 + \lambda V_{SD}) \tag{8}$$

where

$$K = \mu C_{ox}\frac{W}{L}$$

and λ is the channel length modulation parameter.

Although the current mirror transistors M7 and M8 have the same gate and source voltages, there will still be a current transfer error because the drain voltages are different. The current in M8 will be given by

$$I_8 \approx I_7[1 + \lambda(V_{D7} - V_{D8})] \tag{9}$$

This dependence of the current on the drain voltage causes an offset voltage to appear at the X terminal, even for equal Y terminal voltages. The offset voltage can be compensated, if the drain voltages of M8 and M7 are equal. This can be achieved if

$$V_{G7} = V_{G9} \tag{10}$$

which requires

$$\frac{K_7}{K_9} = \frac{I_{b1}}{I_b} \tag{11}$$

where I_{b1} is the biasing current through transistor M5 and I_b is the biasing current through transistor M12. The condition of eqn. 11 will maintain equal gate voltages for transistors M7 and M9, for equal Y terminal voltages. This makes V_X nearly independent of the common-mode Y-terminal voltage which reduces distortion.

Fig. 8 shows V_X against the common-mode input voltage applied at the Y terminals. It can be seen from Table 2 that the aspect ratios of transistors M7 and M9 satisfy the condition for compensation, as given by eqn. 11. The compensation condition of eqn. 11, however, will not hold if a current is withdrawn from the X terminal. The current withdrawn from the X terminal will cause the gate voltage of M9 to change and, hence, an offset voltage will appear at the X terminal. This offset voltage is dependent on the magnitude of the current drawn and is modelled by a small resistance r_x. The resistance r_x can be obtained by performing a small signal analysis which yields:

$$r_x = (g_{d_4} + g_{d_8})/g_{m_4}g_{m_9} \tag{12}$$

where g_d and g_m denote the drain conductance and the transconductance, respectively.

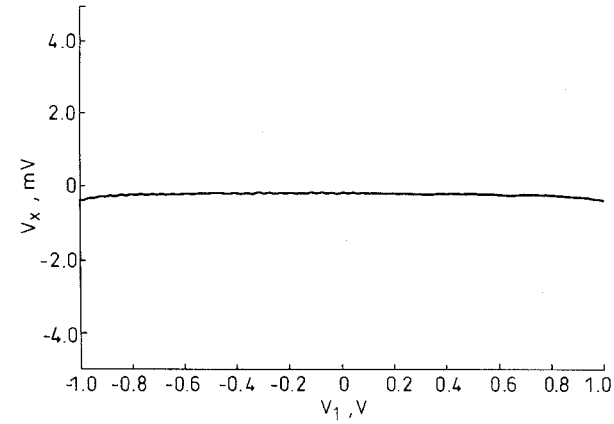

Fig. 8 *X-terminal voltage against common-mode input voltage applied at Y terminals*

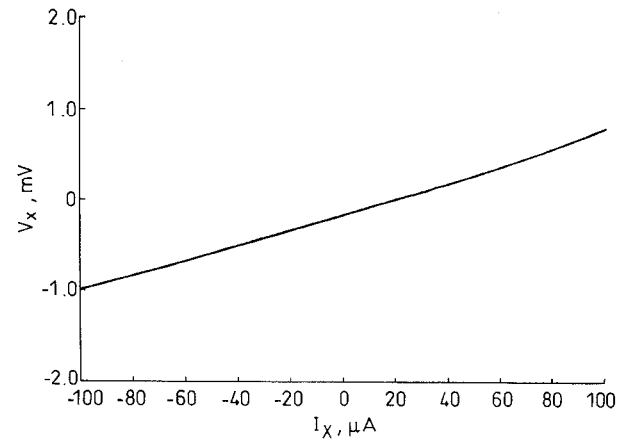

Fig. 9 *Variation of X-terminal voltage against current I_X*

Small-signal PSpice simulation indicates that the X terminal resistance is 10Ω. Fig. 9 shows the variation of the X-terminal voltage against the current I_x, from which the X terminal resistance is evaluated to be 12Ω. The variation of the X-terminal impedance with frequency is shown in Fig. 10.

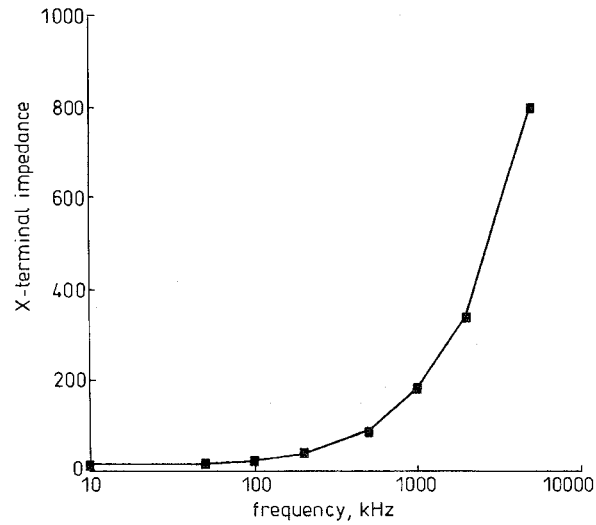

Fig. 10 *Variation of X-terminal impedance with frequency*

The small-signal output resistance of the Z terminal is given by

$$r_z = 1/(g_{d_{10}} + g_{d_{13}}) \quad (13)$$

Fig. 11 shows the variation of the Z-terminal current against the voltage V_Z. The output resistance is larger than 1 MΩ.

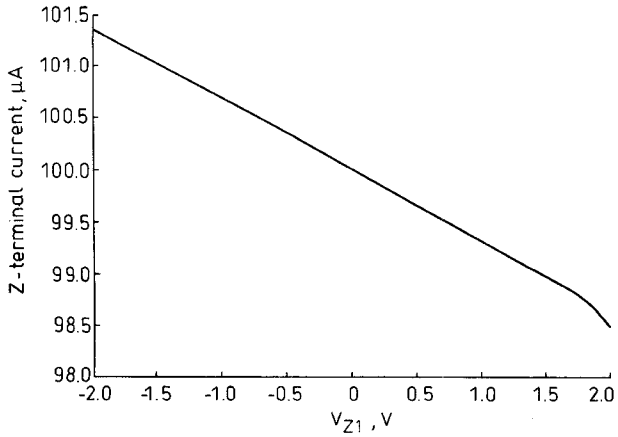

Fig. 11 *Variation of Z-terminal current against voltage V_Z*

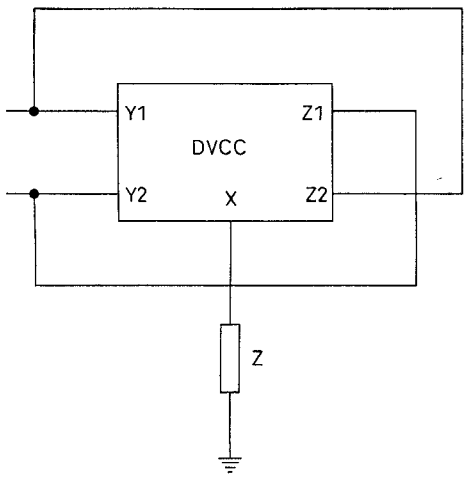

Fig. 12 *Grounded to floating positive impedance converter*

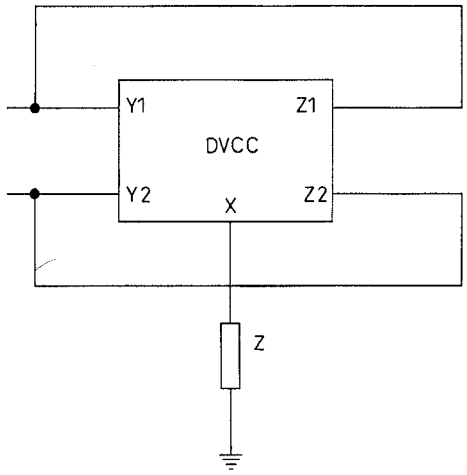

Fig. 13 *Grounded to floating negative impedence converter*

4 Applications based on DVCC

The DVCC is very flexible in implementing impedance conversion circuits, especially those which employ floating inputs. The advantage is that these circuits can be realised without the requirement of complicated circuitry and tight component matching. The realisation of a grounded to floating impedance converter and a grounded to floating negative impedance converter are shown in Figs. 12 and 13, respectively. Floating generalised impedance inverters and floating gyrators can be implemented using two DVCCs connected as shown in Figs. 14–16. A floating frequency-dependent negative resistance (FDNR) as well as a floating inductor can be realised from the circuits of Figs. 15 and 16, respectively. Although floating inductors and FDNR implementations based on two CCIIs only have been reported, these two current conveyor implementations generally require more external components, many of which have to be tightly matched, and, in some cases, they also suffer from high component sensitivities [4–7].

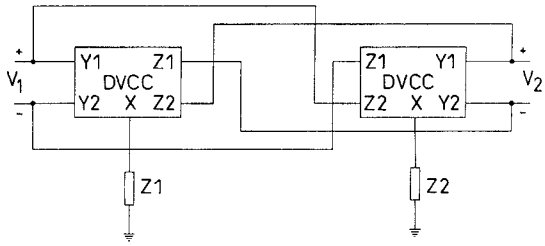

Fig. 14 *Floating generalised negative impedance inverter*

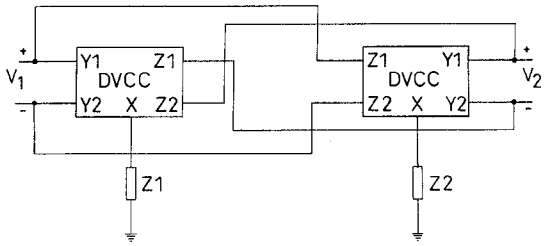

Fig. 15 *Floating generalised positive impedence inverter*

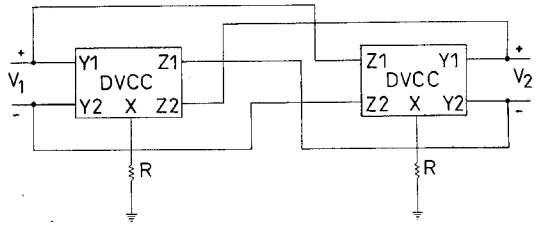

Fig. 16 *Floating gyrator*

4.1 MOSFET-C filter based on DVCC

The DVCC is a versatile building block for MOSFET-C continuous-time filters. Such filters are mainly used for analogue signal processing and are now widely accepted in industry [7–9]. The basic building block of these filters is the integrator realised by MOS transistors operating in the ohmic region, in an appropriate op-amp circuit structure that cancels the nonlinearities. MOSFET-C filters implemented with op-amps suffer from a limited frequency range due to the finite gain bandwidth product of the op-amp. This disadvantage is not present if the DVCC is used as a basic building block to implement current mode MOSFET-C filters. The DVCC can be used to cancel the nonlinearities of a MOS transistor connected between the Y2 and the X terminal, with the Y1 terminal grounded as shown in Fig. 17. In this case, the output current is given by

$$I_Z = 2K(V_G - V_T)V_i \quad (14)$$

Fig. 18 shows the output current of the transconductor of Fig. 17, where the input voltage is scanned for different values of gate voltage.

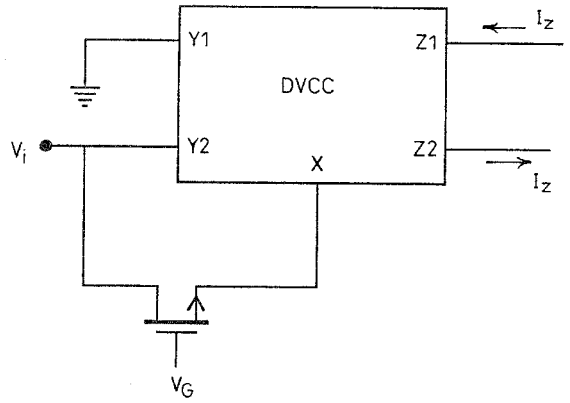

Fig. 17 *MOS transconductor based on DVCC*

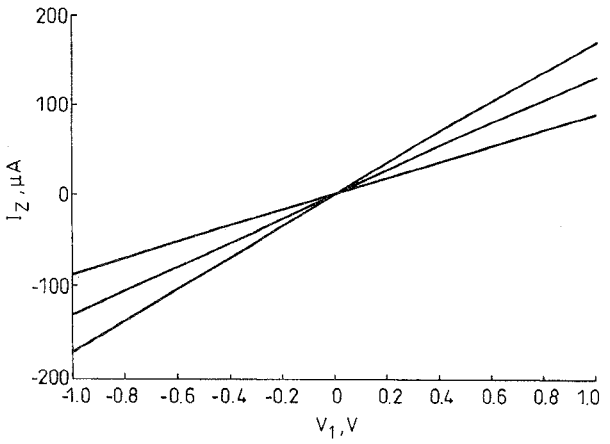

Fig. 18 *Output current of transconductor shown in Fig. 17*

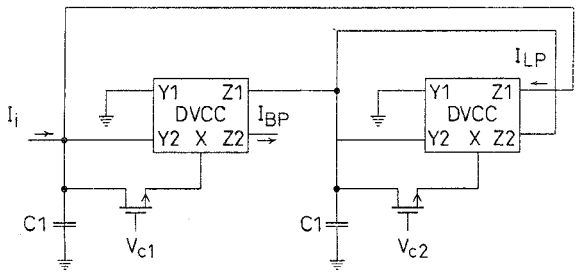

Fig. 19 *Current mode MOSFET-C bandpass filter*

A current mode electronically tunable bandpass filter based on this principle is shown in Fig. 19. The low-pass and bandpass current transfer functions are given by

$$\frac{I_{LP}}{I_i} = \frac{\frac{G_1G_2}{C_1C_2}}{S^2 + S\frac{G_1}{C_1} + \frac{G_1G_2}{C_1C_2}} \tag{15}$$

$$\frac{I_{BP}}{I_i} = \frac{S\frac{G_1}{C_1}}{S^2 + S\frac{G_1}{C_1} + \frac{G_1G_2}{C_1C_2}} \tag{16}$$

where

$$G_1 = 2K_1(V_{C1} - V_T) \tag{17}$$

$$G_2 = 2K_2(V_{C2} - V_T) \tag{18}$$

hence,

$$\omega_o = \sqrt{\frac{G_1G_2}{C_1C_2}} \quad \text{and} \quad Q = \sqrt{\frac{C_1G_2}{C_2G_1}} \tag{19}$$

The bandpass response shown in Fig. 20 is obtained by choosing $C_1 = 0.5\text{nF}$ $C_2 = 0.05\text{nF}$, $V_{C1} = V_{C2} = 3\text{V}$, $K_1 = K_2 = 45\mu\text{A/V}^2$ and $V_T = 0.78\text{V}$.

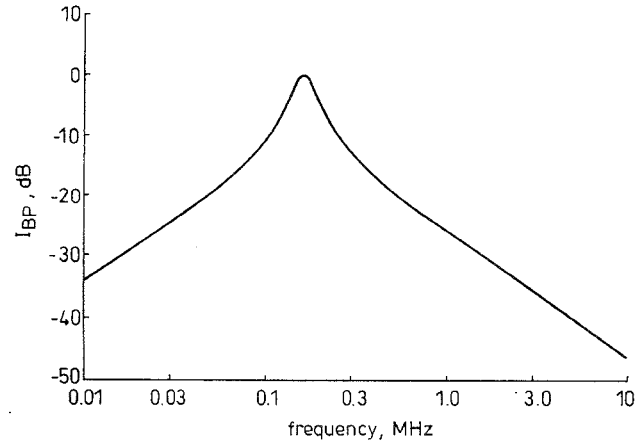

Fig. 20 *Bandpass current response of filter shown in Fig. 19*

5 Conclusion

In this paper, a novel DVCC building block is introduced. Two CMOS realisations of this block are given, the differential nature of this block is seen to be suitable for implementing floating and differential circuit structures. We used our DVCC to realise a current mode electronically tunable MOSFET-C filter. Pspice simulations taking into account the second-order effects, like mobility degradation and channel length modulation, confirm the excellent results as expected.

6 Acknowledgment

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