Journal of Circuits, Systems, and Computers
Vol. 22, No. 7 (2013) 1350060 (13 pages)

DOI: 10.1142/S0218126613500606

GENERATION OF THIRD-ORDER QUADRATURE OSCILLATOR CIRCUITS USING NAM EXPANSION*

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Received 28 March 2013
Accepted 16 May 2013
Published 16 July 2013

A systematic synthesis procedure for generating third-order grounded passive element quadrature oscillators is given. The synthesis procedure is based on using nodal admittance matrix (NAM) expansion applied to the Y matrix of a recently reported three Op Amp third-order oscillator circuit. Four new circuits using current conveyors (CCII) are reported. In addition four more new circuits using inverting current conveyors (ICCII) are also given. Many more quadrature third-order oscillator circuits using combinations of CCII and ICCII can be obtained. Simulation results demonstrating the practicality of one of the generated circuits are included.

Keywords: Third-order oscillators; current conveyors.

1. Introduction

The symbolic framework for systematic synthesis of linear active circuits based on nodal admittance matrix (NAM) expansion was introduced and presented in Refs. 1−4. The NAM expansion in Refs. 1−4 was limited to the use of nullators and norators as the two pathological elements.[5]

The systematic synthesis method based on NAM expansion using nullor elements has been extended to accommodate pathological mirror elements introduced in Refs. 6−8. This results in a generalized framework encompassing all pathological elements for ideal description of active elements.[9−12] Accordingly, more alternative realizations are possible and a wide range of active devices can be used in the synthesis.

In this paper, the conventional systematic synthesis framework using NAM expansion is used to synthesize grounded passive element third-order quadrature oscillator circuits. The active building blocks that are considered are the current conveyors (CCII)[13] or the inverting current conveyors (ICCII).[6]

*This paper was recommended by Regional Editor Piero Malcovati.

First a brief review of the second-order quadrature oscillators using three Op Amps is given.

2. Second-Order Quadrature Oscillators

The two integrator loop quadrature oscillator using three Op Amps is shown in Fig. 1(a) and can be described by the following state equation[14]:

$$\begin{bmatrix} C_1 \dfrac{dv_1}{dt} \\ C_2 \dfrac{dv_2}{dt} \end{bmatrix} = \begin{bmatrix} 0 & G_1 \\ -G_2 & 0 \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \end{bmatrix}. \tag{1}$$

This circuit has the disadvantage that there is no condition for oscillation. The radian frequency of oscillation is given by:

$$\omega_0 = \sqrt{\frac{G_1 G_2}{C_1 C_2}}. \tag{2}$$

A modified circuit using two additional resistors was given in Ref. 14 and is shown in Fig. 1(b) and the state equation is given by:

$$\begin{bmatrix} C_1 \dfrac{dv_1}{dt} \\ C_2 \dfrac{dv_2}{dt} \end{bmatrix} = \begin{bmatrix} \dfrac{G_1 G_4}{G} & G_1 \\ -G_2 & -G_3 \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \end{bmatrix}. \tag{3}$$

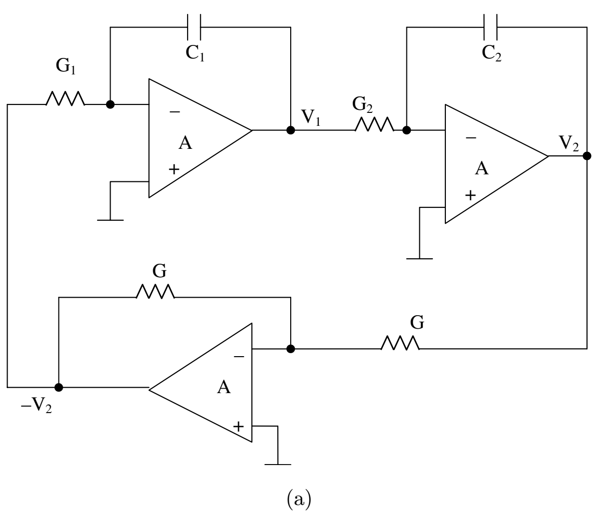
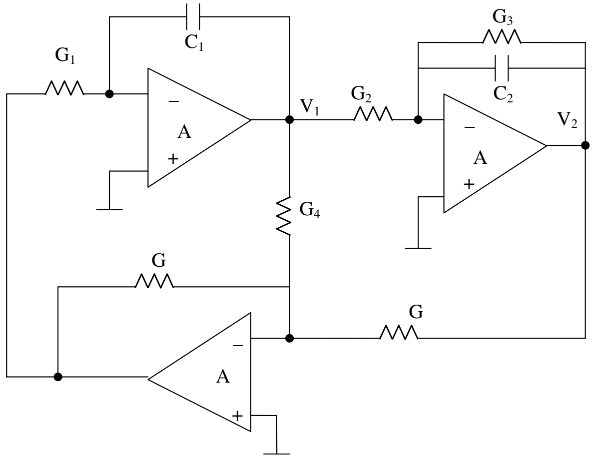
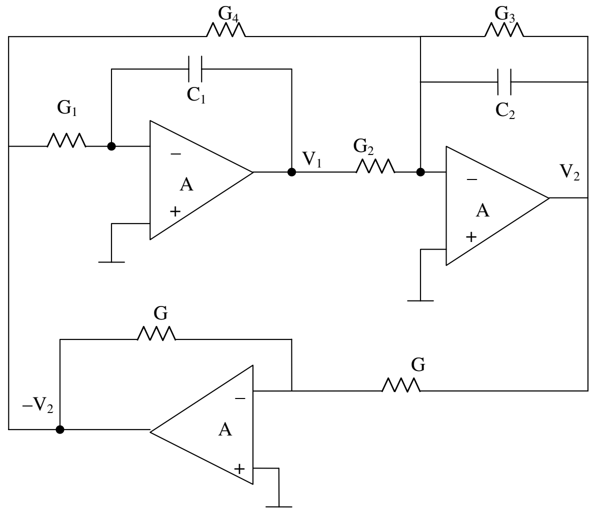


Fig. 1. (a) Three Op Amp second-order oscillator circuit.[14] (b) The three single input Op Amp oscillator proposed in Ref. 14. (c) A modified three single input Op Amps quadrature oscillator.



(b)



(c)

Fig. 1. (*Continued*)

The condition of oscillation is given by:

$$\frac{G_1 G_4}{G G_3} = \frac{C_1}{C_2} \,. \tag{4}$$

Although there is now a control on the condition of oscillation, the circuit of Fig. 1(b) does not provide quadrature outputs after this modification. A modified quadrature output oscillator circuit is shown in Fig. 1(c) which is obtained from

Fig. 1(b) by changing the position of G_4. The state equation in this case is given by:

$$\begin{bmatrix} C_1 \dfrac{dv_1}{dt} \\ C_2 \dfrac{dv_2}{dt} \end{bmatrix} = \begin{bmatrix} 0 & G_1 \\ -G_2 & G_4 - G_3 \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \end{bmatrix}. \tag{5}$$

The condition of oscillation is given by:

$$G_4 = G_3 \,. \tag{6}$$

This quadrature oscillator is similar to the circuit of Fig. 2(c) reported in Ref. 12.

3. Third-Order Quadrature Oscillators

A third-order quadrature oscillator using three Op Amps was recently given in Ref. 15 and is shown in Fig. 2; using same notations as in Ref. 15. The state equation in this case is given by:

$$\begin{bmatrix} C_2 \dfrac{dv_1}{dt} \\ C_3 \dfrac{dv_2}{dt} \\ C_1 \dfrac{dv_3}{dt} \end{bmatrix} = \begin{bmatrix} -G_2 & 0 & -G_3 \\ -G_4 & 0 & 0 \\ 0 & -G_5 & -G_1 \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ v_3 \end{bmatrix}. \tag{7}$$

The voltages V_1 and V_2 are the two quadrature outputs and the condition of oscillation is given by:

$$\frac{G_3 G_4 G_5}{G_1 G_2 C_3} = \frac{G_1}{C_1} + \frac{G_2}{C_2} \,. \tag{8}$$

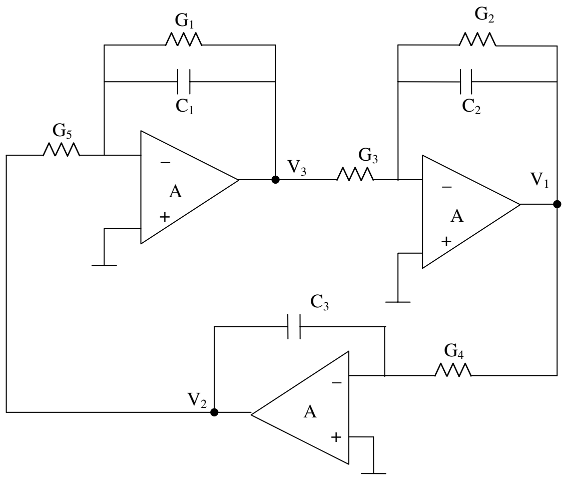


Fig. 2. Three Op Amp third-order oscillator circuit.[15]

The condition of oscillation can be controlled by G_3 or G_4 or G_5 without affecting the radian frequency of oscillation which is given by (2).

The circuit of Fig. 2 employs three floating capacitors and three floating resistors. Grounded capacitors quadrature oscillators using the current feedback operational amplifiers (CFOA)[16] are discussed in the following section.

4. Quadrature Oscillators Using CFOA or CCII (ICCII)

A second-order quadrature oscillator using three CFOA was reported in Ref. 12 and is shown in Fig. 3(a). The state equation in this case is given by:

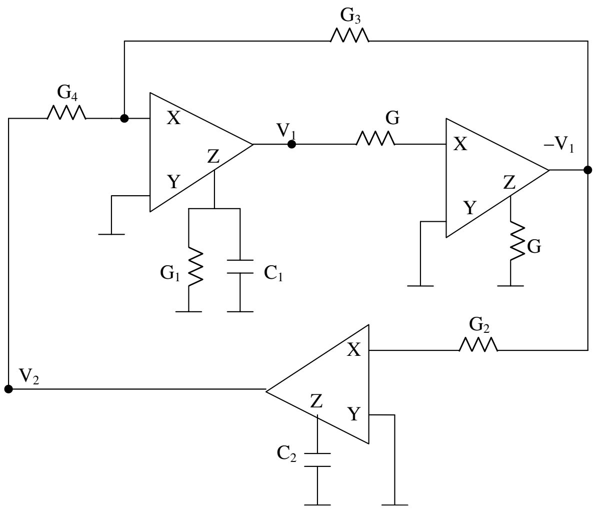
$$\begin{bmatrix} C_1 \dfrac{dv_1}{dt} \\ C_2 \dfrac{dv_2}{dt} \end{bmatrix} = \begin{bmatrix} G_3 - G_1 & -G_4 \\ G_2 & 0 \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \end{bmatrix}. \tag{9}$$

The condition of oscillation can be controlled by G_3 or G_1 and is given by:

$$G_3 = G_1 \,. \tag{10}$$

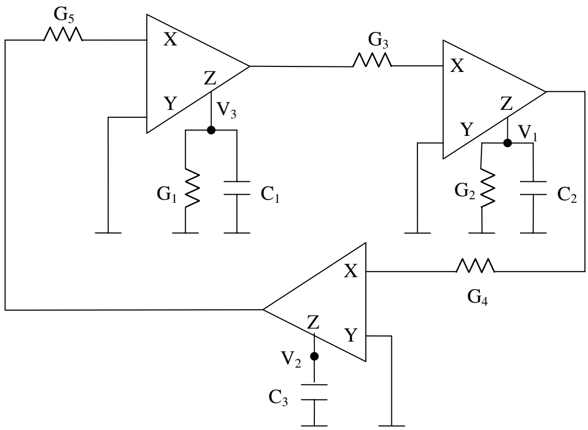
This circuit can absorb the effects of R_{X2} and R_{X3} as well as the effects of C_{Z1} and C_{Z3}. On the other hand it is affected by the stray resistance R_{X1} and the stray capacitance C_{Z2}.

A grounded capacitor version of the circuit of Fig. 2 and using three CFOA can be easily synthesized from (7) and is shown in Fig. 3(b).



(a)

Fig. 3. (a) Three CFOA grounded capacitors second-order oscillator circuit.[12] (b) Three CFOA grounded capacitors third-order oscillator circuit.



(b)

Fig. 3. (*Continued*)

The advantage of this circuit is that it can absorb the three parasitic resistances R_X and the three parasitic capacitances C_Z.

Grounded capacitors and grounded resistors second-order quadrature oscillators and using different active building blocks were reviewed in Ref. 17.

Generation of grounded capacitors and grounded resistors third-order oscillators and using CCII or ICCII and using NAM expansion are given next.

The NAM of the Op Amp circuit of Fig. 2 is given by:

$$Y = \begin{bmatrix} sC_2 + G_2 & 0 & G_3 \\ G_4 & sC_3 & 0 \\ 0 & G_5 & sC_1 + G_1 \end{bmatrix}. \tag{11}$$

The three capacitors are at diagonal positions hence will be realized as grounded capacitors. In order to have grounded resistors, it is desirable to move G_3, G_4 and G_5 to diagonal positions.

Adding a blank row and column to (11), connecting a nullator between node 3 and node 4 and a norator between nodes 1 and 4 to move G_3 to the diagonal position 4, 4 as follows:

$$Y = \left[\begin{bmatrix} sC_2 + G_2 & 0 & 0 & 0 \\ G_4 & sC_3 & 0 & 0 \\ 0 & 0 & sC_1 + G_1 & 0 \\ 0 & G_5 & 0 & G_3 \end{bmatrix}\right]. \tag{12}$$

Adding a blank row and column to (12), connecting a nullator between node 1 and node 5 and a norator between nodes 2 and 5 to move G_4 to the diagonal position 5, 5 as follows:

$$Y = \left[\left[\begin{bmatrix} sC_2 + G_2 & 0 & 0 & 0 & 0 \\ 0 & sC_3 & 0 & 0 & 0 \\ 0 & G_5 & sC_1 + G_1 & 0 & 0 \\ 0 & 0 & 0 & G_3 & 0 \\ 0 & 0 & 0 & 0 & G_4 \end{bmatrix}\right]\right]. \tag{13}$$

Finally it is desirable to move G_5 to the diagonal position 6, 6 as follows:

$$Y = \left[\left[\left[\begin{bmatrix} sC_2 + G_2 & 0 & 0 & 0 & 0 & 0 \\ 0 & sC_3 & 0 & 0 & 0 & 0 \\ 0 & 0 & sC_1 + G_1 & 0 & 0 & 0 \\ 0 & 0 & 0 & G_3 & 0 & 0 \\ 0 & 0 & 0 & 0 & G_4 & 0 \\ 0 & 0 & 0 & 0 & 0 & G_5 \end{bmatrix}\right]\right]\right]. \tag{14}$$

Figure 4 represents the realization of (14) using three CCII−. This circuit is equivalent to the circuit of Fig. 2 and uses grounded passive elements. It has the advantage that it can absorb the three parasitic resistances R_{X1} in R_5 and R_{X2} in R_3 and R_{X3} in R_4. The three parasitic capacitances can be absorbed in the three circuit capacitors as follows; C_{Z1} in C_1 and C_{Z2} in C_2 and C_{Z3} in C_3.

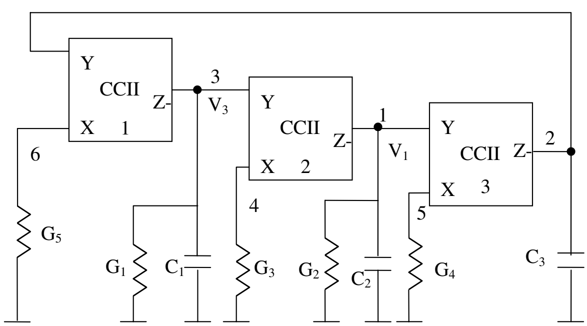


Fig. 4. Three CCII-grounded passive elements third-order oscillator circuit.

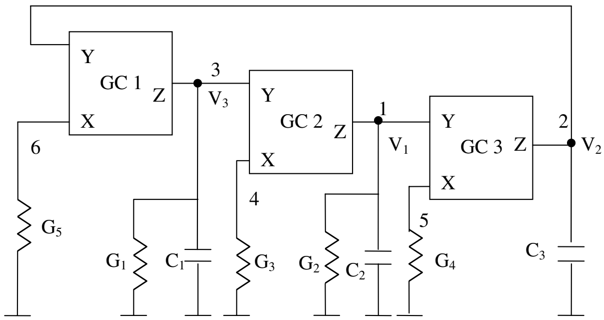


Fig. 5. Three GC grounded passive elements third-order oscillator circuit.

The circuit of Fig. 4 belongs to a family of oscillators that can be obtained by generalizing the three CCII− circuit using generalized conveyors (GC) defined by:

$$I_Y = 0\,, \quad V_X = aV_Y \quad \text{and} \quad I_Z = KI_X\,, \tag{15}$$

where $a = 1$ for CCII and $a = -1$ for ICCII. $K = 1$ for CCII+ and ICCII+ and $K = -1$ for CCII− and ICCII−.

The generalized circuit topology is shown in Fig. 5. The oscillator family members can be obtained from the following generalized characteristic equation:

$$s^3C_1C_2C_3 + s^2C_3[C_1G_2 + C_2G_1] + sC_3G_1G_2 - a_1a_2a_3K_1K_2K_3G_3G_4G_5 = 0\,. \tag{16}$$

The necessary coefficient condition of oscillation is given by:

$$a_1a_2a_3K_1K_2K_3 = -1\,. \tag{17}$$

For the CCII family, the coefficients a_1, a_2 and a_3 must be 1 and four circuits are obtained and given in Table 1.

For the ICCII family the coefficients a_1, a_2 and a_3 must be −1 and four circuits are obtained and given in Table 2.

Several circuits can be generated using combinations of CCII and ICCII and satisfying (17) and are not included here to limit the paper length.

Table 1. Four alternative CCII realizations derived from Fig. 5.

Circuit	a_1	K_1	a_2	K_2	a_3	K_3	GC_1	GC_2	GC_3
1	+	−	+	−	+	−	CCII−	CCII−	CCII−
2	+	−	+	+	+	+	CCII−	CCII+	CCII+
3	+	+	+	−	+	+	CCII+	CCII−	CCII+
4	+	+	+	+	+	−	CCII+	CCII−	CCII−

Table 2. Four alternative ICCII realizations derived from Fig. 5.

Circuit	a_1	K_1	a_2	K_2	a_3	K_3	GC_1	GC_2	GC_3
1	−	+	−	+	−	+	ICCII+	ICCII+	ICCII+
2	−	−	−	−	−	+	ICCII−	ICCII−	ICCII+
3	−	−	−	+	−	−	ICCII−	ICCII+	ICCII−
4	−	+	−	−	−	−	ICCII+	ICCII−	ICCII−

5. Adjoint of Third-Order Quadrature Oscillators

Although the adjoint network theorem is used to transform voltage mode circuits to current mode equivalent circuits,[20,21] it can also be used to transform oscillator circuits to obtain new equivalent circuits.

Figure 6 represents the third-order oscillator circuit adjoint to Fig. 2. The adjoint of the single input Op Amp is also a single input Op Amp.[16] The NAM obtained by writing KCL at nodes 1, 2 and 3 is given by:

$$Y = \begin{bmatrix} sC_2 + G_2 & G_4 & 0 \\ 0 & sC_3 & G_5 \\ G_3 & 0 & sC_1 + G_1 \end{bmatrix}. \tag{18}$$

The two voltages in quadrature are now V_2 and V_3 and not V_1 and V_2 as in the circuit of Fig. 2.

Several CCII and ICCII third-order oscillator circuits can be generated from the family of oscillators given in the previous section. Here only one circuit is given in

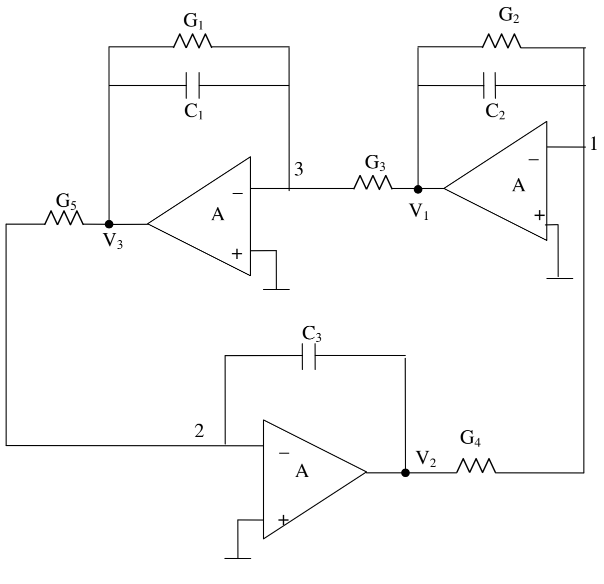


Fig. 6. Three Op Amp third-order oscillator circuit adjoint to the circuit of Fig. 2.

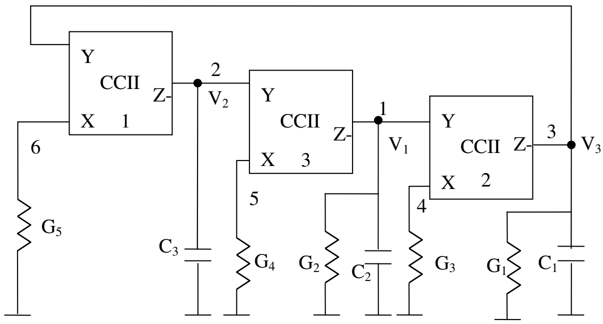


Fig. 7. Three CCII- third-order oscillator circuit adjoint to the circuit of Fig. 4.

Fig. 7 which is the adjoint of the three CCII−; circuit given in Fig. 3 and its NAM equation is given by (18).

6. Simulation Results

The active building block used in all simulations included in this paper is the DVCC.[18,19] The DVCC is defined as a five port building block with a describing matrix of the form:

$$\begin{bmatrix} V_X \\ I_{Y1} \\ I_{Y2} \\ I_{Z+} \\ I_{Z-} \end{bmatrix} = \begin{bmatrix} 0 & 1 & -1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 \\ -1 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_X \\ V_{Y1} \\ V_{Y2} \\ V_{Z+} \\ V_{Z-} \end{bmatrix}. \tag{19}$$

The DVCC is a very powerful building block as it realizes each of CCII+, CCII−, ICCII+ and ICCII− as special cases.

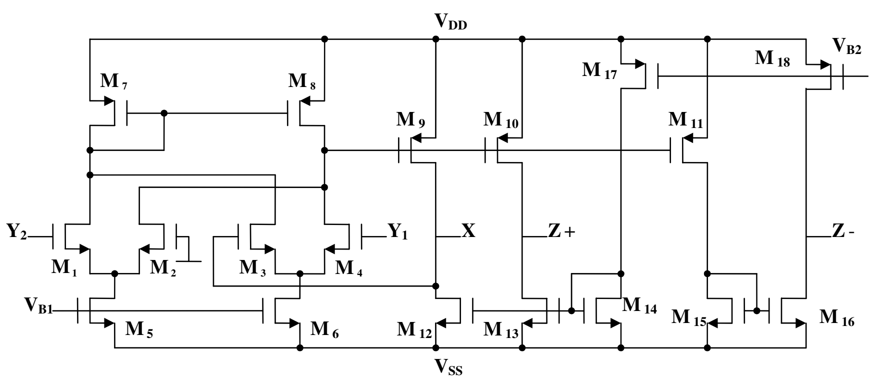


Fig. 8. CMOS circuit of the CCII or ICCII.[18]

Table 3. Dimensions of the MOS transistors of Fig. 8.

MOS transistors	$W(\mu\text{m})/L(\mu\text{m})$
M_1, M_2, M_3, and M_4	2.5/1
M_5 and M_6	8/1
M_{12}, M_{13}, M_{14}, M_{15}, and M_{16}	20/2.5
M_7 and M_8	10/1
M_9, M_{10}, M_{11}, M_{17}, and M_{18}	40/2

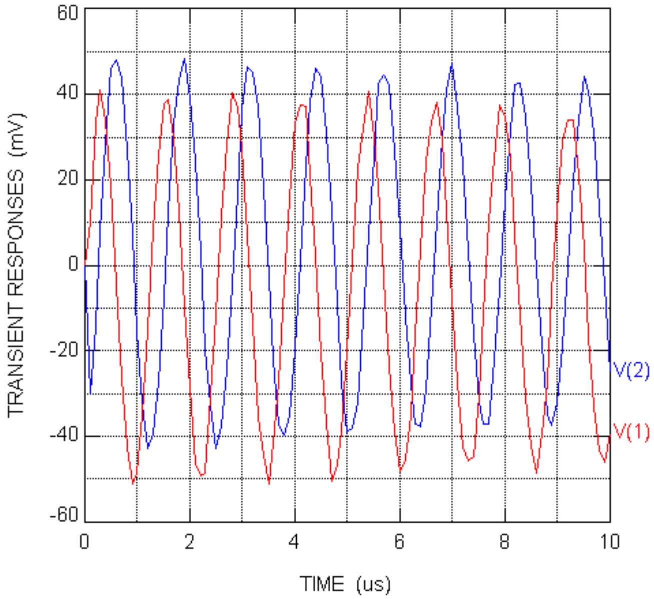


Fig. 9. The output waveforms of the circuit 2 in Table 1.

Figure 8 represents the CMOS DVCC circuit,[18] the transistor aspect ratios are given in Table 3 based on the 0.5 μm CMOS model from MOSIS. The supply voltages used are ± 1.5 V and $V_{B1} = -0.52$ V and $V_{B2} = 0.33$ V.

Figure 9 represents the output voltage waveform of the oscillator number 2 in Table 1 using CCII− and two; CCII+, designed for oscillation frequency equal to 0.8 MHz by taking $C_1 = C_2 = C_3 = 10$ pF, $R_1 = R_2 = R_3 = R_4 = 20\,\text{k}\Omega$ and $R_5 = 10\,\text{k}\Omega$. The total power dissipation is given by 2.96594 mW.

7. Conclusion

New family of third-order oscillator quadrature oscillator circuits are generated from the three Op Amp circuit[15] using NAM expansion.

It is found that there are four CCII circuits and four ICCII circuits. They have the advantages of having all passive elements being grounded. An additional advantage of the CCII and ICCII circuits is that all parasitic R_X and C_Z can be absorbed in the circuit components. Simulation results demonstrating the practicality of some of the generated circuits are included.

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