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Inverting second generation current conveyors: the missing building blocks, CMOS realizations and applications

INAS A. AWAD† and AHMED M. SOLIMAN†

The concept of voltage mirror is introduced and used, together with the current mirror, to ideally represent the current and voltage inverting properties of some analogue building blocks. The properties of the nullor and mirror elements are used to relate the different devices in the ideal case as well as to define the adjoint network for each building block. Two new types of second generation current conveyor (CCII) are introduced. One is the adjoint of the CCII+ and is named the inverting second generation current conveyor 'negative' (ICCII−); the other is the ICCII+. CMOS realizations of the ICCII− are presented and new ICCII− based current mode circuits are obtained by applying a voltage-to-current-mode transformation to the CCII+ based circuits.

1. Introduction

Several authors have investigated the possible theoretical existence of networks consisting of ideal elements, the behaviour of whose terminals cannot be described by any of the existing network descriptions such as Z, Y and H matrices. Such networks usually called pathological networks, are degenerate forms and are needed to complete the domain of network elements. The concept of nullors, i.e. combinations of nullators and norators, was first implicitly introduced by Tellegen (1954) under the name of ideal elements and given its present name by Carlin (1964) ten years later.

The main reasons for the popularity of these pathological elements are their capability of modelling active circuits independently of the particular realization of the active devices and the possibility of generating a number of equivalent idealized circuits from which the best practical ones can thereafter be selected.

It is well known that voltage mode circuits can be converted to current mode circuits using the adjoint network theorem (Roberts and Sedra 1989a), where the circuits are modelled in terms of passive networks and controlled sources. More generally, current mode circuits can be generated from their voltage mode counterparts simply by interchanging the nullators and norators (Carlosena and Moschytz 1993).

Despite the ability of nullators and norators to represent many active building blocks, they fail to represent the second generation current conveyor 'positive' (CCII+) which is one of the most important analogue building blocks (Sedra and Smith 1970). Other elements such as resistors are combined with the nullators and norators in order to obtain the nullor representation of the CCII+ (Svoboda 1989).

In order to avoid the use of resistors in the nullor representation of any building block, other pathological elements rather than nullators and norators need to be

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defined. One of these missing elements must represent the current mirroring action existing at the output port of the CCII+ and the other must represent a voltage mirroring action. The definition of these new mirror elements is given in § 2, and they are used to define the adjoint building block of the CCII+ which is introduced in § 3 and given the name 'Inverting second generation current conveyor "negative" (ICCII−)'. Another new building block, the ICCII+, is also defined and added to the second generation current conveyor family. In § 4, the nullor–mirror elements are used to define the relationships between the different building blocks. Two new ICCII− CMOS realizations are presented, and new applications are given.

2. The mirror elements

In this section the definition of the singular elements, the nullator and the norator, is reviewed; then the definition of the two proposed mirror elements, the current mirror and the voltage mirror, is presented.

The nullator is a one-port network element defined by $V = I = 0$. It presents an open-circuit and a short-circuit simultaneously. It is a bilateral and lossless one-port. On the other hand, the norator is a one-port network element defined by: V and I are arbitrary.

2.1. *The current mirror*

This is a two-port network element used to represent a current reversing action, and is defined by

$$\begin{matrix} V_1 \text{ and } V_2 \text{ are arbitrary} \\ I_1 = I_2, \text{ and they are also arbitrary} \end{matrix} \tag{1}$$

Although the proposed current mirror element has the same symbol as that defined by Wilson (1981) and shown in figure 1(*a*), it is a bidirectional element and has a theoretical existence. It can be represented using a nullator, two norators and two equal resistors as shown in figure 1(*b*). An alternative representation of the current mirror using the same number of elements is shown in figure 1(*c*) (Svoboda 1989).

2.2. *The voltage mirror*

This is a two-port network element used to represent a voltage reversing action, and is defined by

$$V_1 = -V_2 \tag{2a}$$

$$I_1 = I_2 = 0 \tag{2b}$$

Its symbolic representation is shown in figure 2(*a*). Two alternative realizations of the voltage mirror using a norator, two nullators and two equal resistors are shown in figures 2(*b*) and 2(*c*) respectively.

3. The CCII family

The second generation current conveyor CCII was proposed by Sedra and Smith (1970) as a versatile building block for analogue signal processing. Basically, the CCII is described as combined voltage-follower and current-follower. Only two

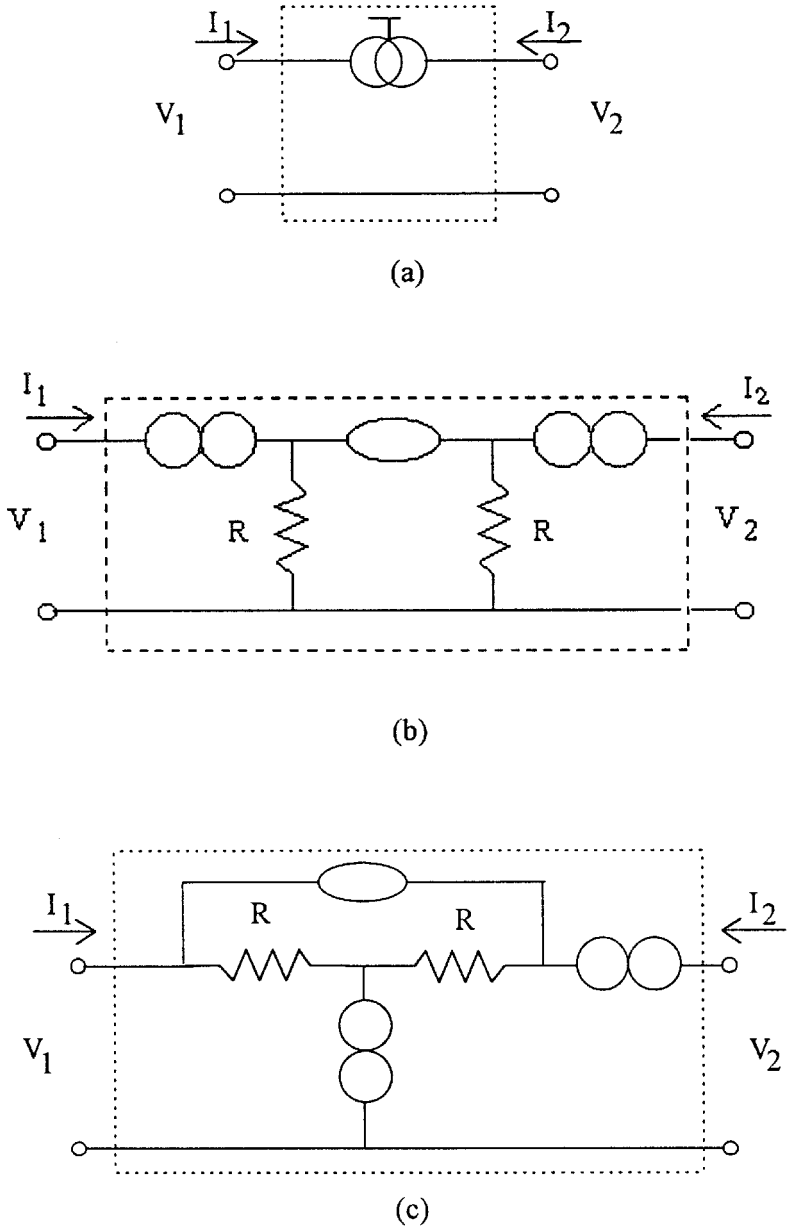


Figure 1. (*a*) The current mirror symbol. (*b*) A current mirror representation using one nullator, two norators and two equal resistors. (*c*) An equivalent current mirror representation using one nullator, two norators and two equal resistors.

types of CCII have been defined (the CCII+ and the CCII−) according to the polarity of the current-follower. However, there are two missing members of the family of the second generation current conveyor CCII and they need to be defined according to the polarity of the voltage-follower. In this section a generalized definition of the CCII family is presented and their nullor–mirror representations are illustrated.

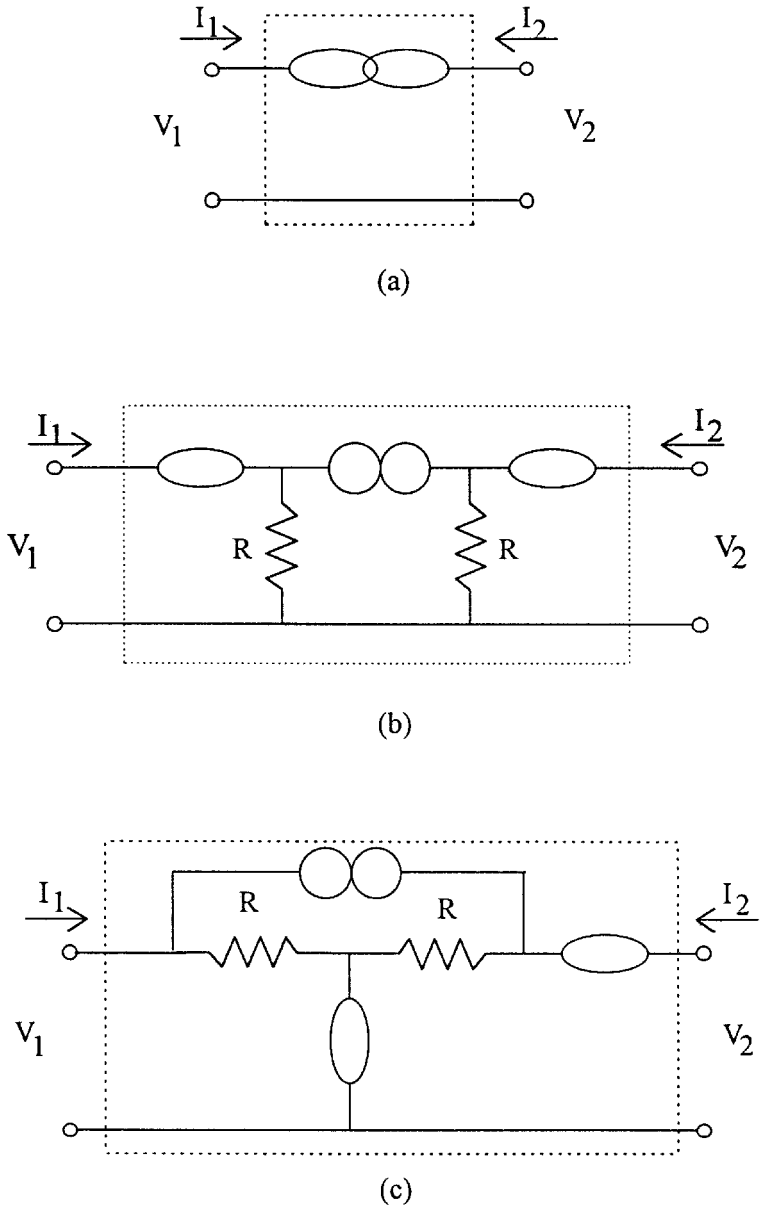


Figure 2. (*a*) The voltage mirror symbol. (*b*) A voltage mirror representation using one norator, two nullators and two equal resistors. (*c*) An equivalent voltage mirror representation using one norator, two nullators and two equal resistors.

Referring to figure 3(*a*), the generalized CCII is a three-terminal device which can be described using the following matrix equation

$$\begin{bmatrix} V_X \\ I_Y \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & \pm 1 & 0 \\ 0 & 0 & 0 \\ \pm 1 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_X \\ V_Y \\ V_Z \end{bmatrix} \tag{3}$$

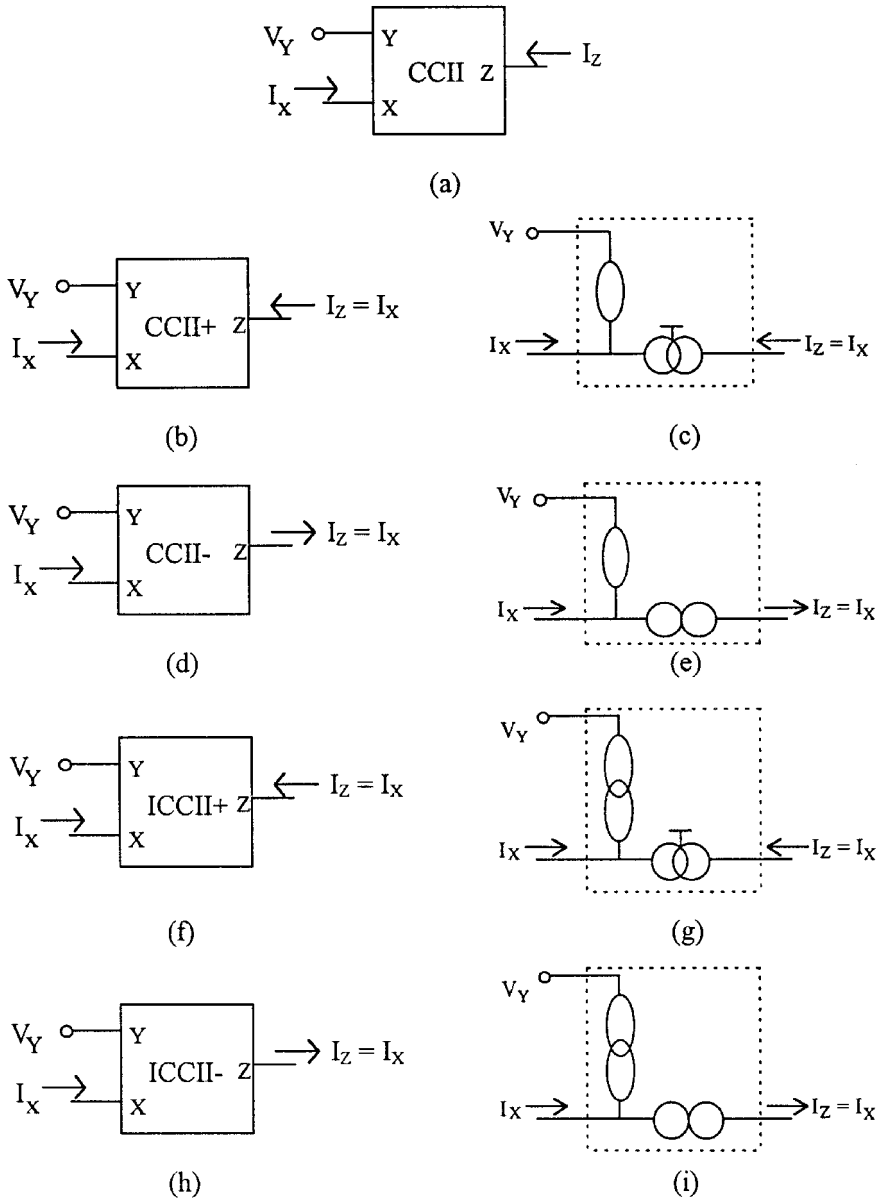


Figure 3. (*a*) The general CCII symbol. (*b*) The CCII+ symbol. (*c*) The CCII+ nullor–mirror representation. (*d*) The CCII− symbol. (*e*) The CCII− nullor representation. (*f*) The ICCII+ symbol. (*g*) The ICCII+ mirror representation. (*h*) The ICCII− symbol. (*i*) The ICCII− nullor–mirror representation.

Table 1 shows four different types of CCII, defined according to the signs of V_X and I_Z relative to V_Y and I_X. The first row of table 1 describes the CCII+, which has positive V_X and positive I_Z. Its symbol and nullor–mirror representation are given in figures 3(*b*) and 3(*c*) respectively. It is represented using a nullator connected to a current mirror. The second type described is the CCII−, which has positive V_X and negative I_Z. Its symbol and well known nullor representation are given in figures 3(*d*)

Sign of V_X	Sign of I_Z	CCII type	Adjoint of the CCII
+	+	CCII+	ICCII−
+	−	CCII−	CCII−
−	+	ICCII+	ICCII+
−	−	ICCII−	CCII+

Table 1. The four types of CCII.

and 3(e) respectively. It is represented using a nullator connected to a norator. Figure 3(f) shows a new CCII− type called the inverting second generation current conveyor 'positive' (ICCII+), It has negative V_X and positive I_Z. It is represented using a voltage mirror connected to a current mirror, as shown in figure 3(g). The last type to be described is the ICCII−, which is the same as the ICCII+ but with negative I_Z. Its symbol and nullor–mirror representation are given in figures 3(h) and 3(i) respectively.

The adjoint network theorem is very useful in the process of designing current-mode circuits which are obtained from their voltage-mode counterparts after replacing each building block with its adjoint and then interchanging the excitation and the response (Roberts and Sedra 1989b). Kaulberg (1993) reported that the adjoint of the CCII− is a CCII−. On the other hand, he described the adjoint of the CCII+ as a building block with a negative voltage-follower and a positive current-follower. This description is the same as that of the ICCII−.

Similarly, the adjoint of any building block can be obtained using the transformation method described by Carlosena and Moschytz (1993), which is based on interchanging the nullators and norators of a given network in order to obtain its adjoint network. On the basis of this transformation method, the current mirrors are replaced by voltage mirrors and vice versa.

Following the transformation method, the adjoint building blocks of the four CCII types can be obtained as given in table 1. The CCII− and ICCII+ are self-adjoint whereas the adjoint of the CCII+ is the ICCII−, and vice versa.

4. The relationships between different building blocks based on their nullor–mirror representations

Many building blocks are represented using the same nullor and mirror elements but with different connections. This property can be used to generate ideally equivalent circuits by simply replacing a building block in any circuit with another one after connecting it in a configuration that results in the same nullor–mirror representation. The ideally equivalent building block configurations are illustrated in table 2. The group of building blocks comprises the voltage op amp (VOA), the operational floating amplifier (OFA) (Huijsing 1993), the current op amp (COA) (Bruun 1995), the operational floating conveyor (OFC) (Toumazou *et al.* 1991), the operational mirrored amplifier (OMA) (Huijsing and Veelenturf 1981), the second generation current conveyor with its four types, the differential difference amplifier (DDA) (Sackinger and Guggenbuhl 1987) and the differential voltage current conveyor (DVCC) (Elwan and Soliman 1997).

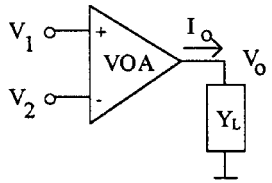
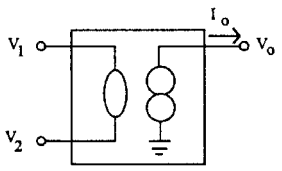
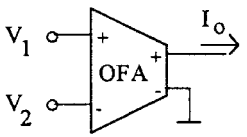
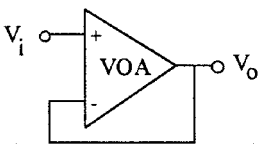
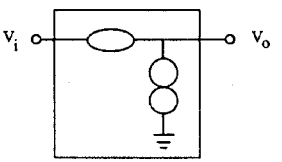
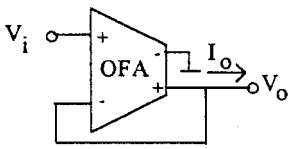
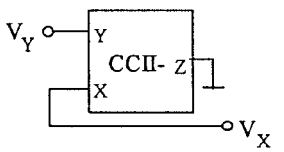
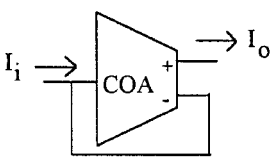
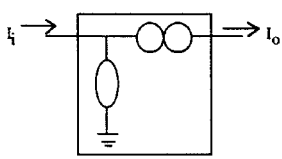
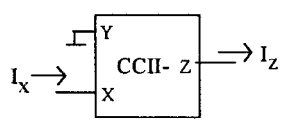
Basic configuration	Nullor-mirror representation	Equivalent configuration
 $I_1 = I_2 = 0$ $V_o = A(s)(V_1 - V_2)$ $I_o = V_o\ Y_L$	 $I_1 = I_2 = 0$ $V_1 = V_2$ V_o , I_o arbitrary	 $I_1 = I_2 = 0$ $I_o = G(s)(V_1 - V_2)$
 $I_i = 0$ $V_o = V_i \dfrac{A(s)}{1 + A(s)}$	 $I_i = 0$ $V_o = V_i$	 $I_i = 0$ $V_o = V_i - G(s)\ I_o$
		 $I_Y = 0$ $V_X = V_Y$
 $V_i = 0$ $I_o = I_i \dfrac{A(s)}{1 + A(s)}$	 $V_i = 0$ $I_o = I_i$	 $V_X = 0$ $I_Z = I_X$

Table 2. Ideally equivalent configurations and their corresponding nullor–mirror representations.

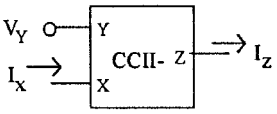
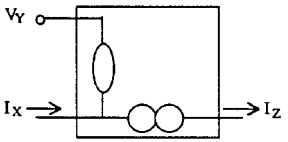
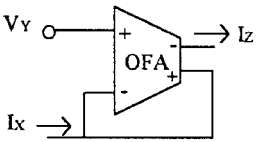
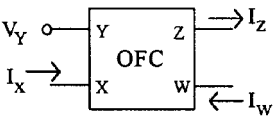
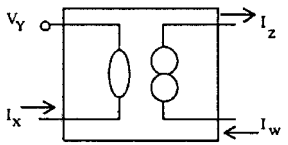
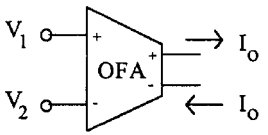
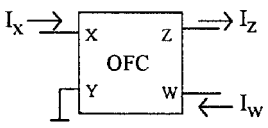
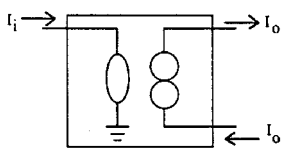
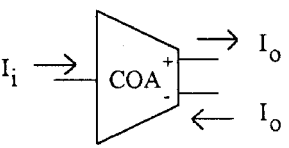
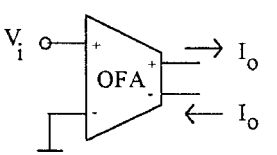
Basic configuration	Nullor-mirror representation	Equivalent configuration
 $I_Y = 0$ $V_X = V_Y$ $I_Z = I_X$	 $I_Y = 0$ $V_X = V_Y$ $I_Z = I_X$	 $I_Y = 0$ $V_X = V_Y + \frac{I_X}{G(s)}$ $I_Z = I_X$
 $I_Y = 0$ $V_X = V_Y$ $V_W = -Z_T I_X$ $I_Z = I_W$	 $I_Y = I_X = 0$ $V_X = V_Y$ V_W arbitrary $I_Z = I_W$	 $I_1 = I_2 = 0$ $I_o = G(s)(V_1 - V_2)$
 $V_X = 0$ $V_W = -Z_T I_X$ $I_Z = I_W$	 $V_i = 0$ $I_i = 0$ I_O arbitrary	 $V_i = 0$ $I_o = A(s) I_i$
		 $I_i = 0$ $I_o = G(s)\ V_i$

Table 2. (*Continued*)

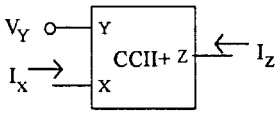
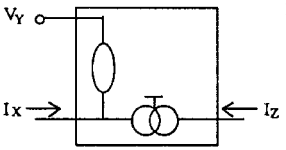
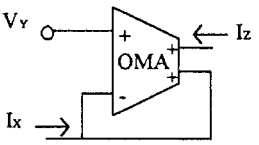
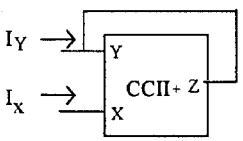
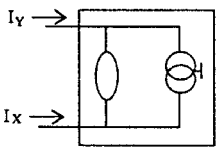
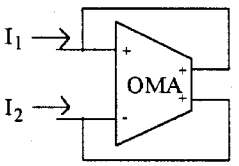
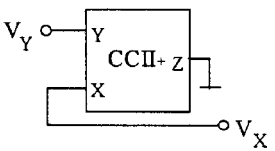
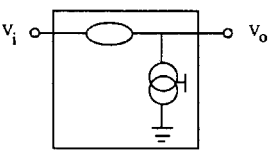
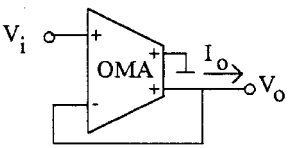
Basic configuration	Nullor-mirror representation	Equivalent configuration
		
$I_Y = 0$ $V_X = V_Y$ $I_Z = I_X$	$I_Y = 0$ $V_X = V_Y$ $I_Z = I_X$	$I_Y = 0$ $V_X = V_Y + \frac{I_X}{G(s)}$ $I_Z = I_X$
		
$V_X = V_Y$ $I_Y = I_X$	$V_X = V_Y$ $I_Y = I_X$	$V_2 = V_1 + \frac{I_2}{G(s)}$ $I_1 = I_2$
		
$I_Y = 0$ $V_X = V_Y$	$I_i = 0$ $V_o = V_i$	$I_i = 0$ $V_o = V_i + \frac{I_o}{G(s)}$

Table 2. (*Continued*)

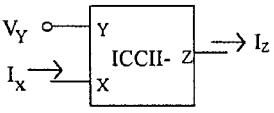
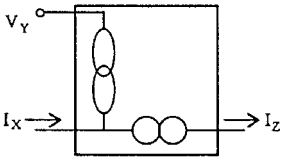
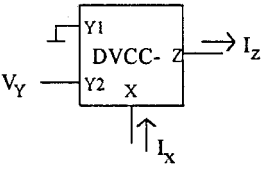
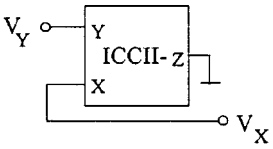
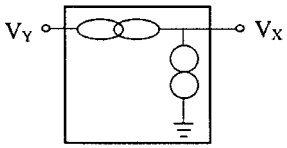
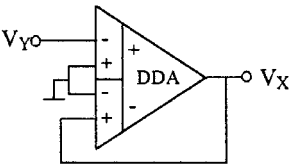
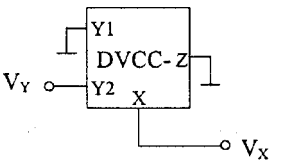
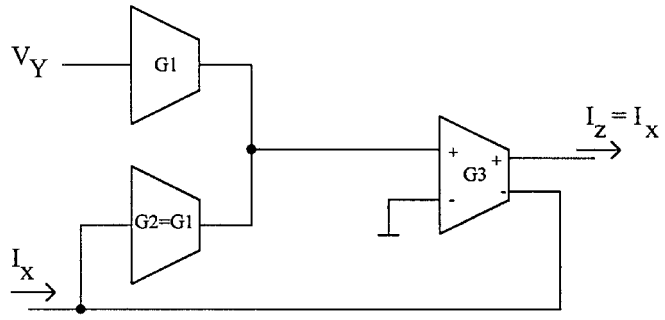
Basic configuration	Nullor-mirror representation	Equivalent configuration
 $I_Y = 0$ $V_X = -V_Y$ $I_Z = I_X$	 $I_Y = 0$ $V_X = -V_Y$ $I_Z = I_X$	 $I_Y = 0$ $V_X = -V_Y + \frac{I_X}{G(s)}$ $I_Z = I_X$
 $I_Y = 0$ $V_X = -V_Y$	 $I_Y = 0$ $V_X = -V_Y$	 $I_Y = 0$ $V_X = -V_Y \frac{A(s)}{1+A(s)}$
		 $I_Y = 0$ $V_X = -V_Y$

Table 2. (*Continued*)

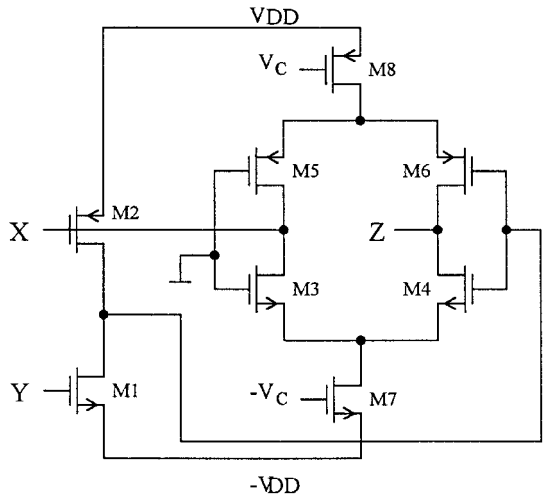
5. New CMOS realizations of the ICCII−

In this section two CMOS realizations of the ICCII− are presented. The two circuit implementations of the ICCII− are based on the block diagram shown in figure 4(*a*). The input stage is formed by blocks G1 and G2, which are single input single output transconductors, while the output stage is formed by block G3 which is a floating output transconductor. Negative feedback is used in order to minimize the input impedance at the X terminal.

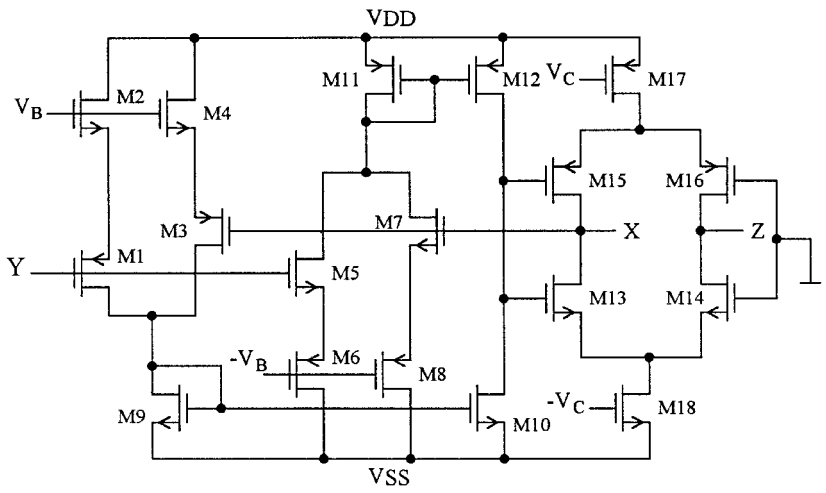
The gain between the Y and the X terminals depends on the transconductors G1 and G2 which must be equal in order to have an inverting property with unity gain between the two terminals.



(*a*)



(*b*)



(*c*)

Figure 4. (*a*) The block diagram of the ICCII− implementation. (*b*) The first proposed ICCII− CMOS realization. (*c*) The second proposed ICCII− CMOS realization.

Many ICCII− CMOS realizations with differing performance can be obtained according to the basic transconductor used. In order to obtain accurate current-following action between the X and the Z terminals, the floating output stage G3 is realized using the floating current source (FCS) introduced by Arbel and Goldminz (1992) whereas two alternative realizations are given for the input transconductors.

5.1. *The first proposed CMOS realization*

Figure 4(*b*) shows the first proposed ICCII− CMOS realization, which is the simplest realization since the input stage is formed by an NMOS transistor M1 and a PMOS transistor M2. For proper operation, the aspect ratios of M1 and M2 must be chosen according to the following relation:

$$\frac{(W/L)_1}{(W/L)_2} = \frac{\mu_p}{\mu_n} \tag{4}$$

where μ_n and μ_p are the electron and hole mobilities respectively.

Transistors M3 to M8 form the FCS output stage which provides two balanced output currents; one of them is fed back into the X terminal and the other is the Z terminal output current. The accuracy between I_X and I_Z is determined by the matching of the transistors M7 and M8. The input resistance seen at the X terminal, R_x, is equal to the inversion of the loop gain; hence, a low impedance level can be achieved by increasing the transconductance of the output stage.

5.2. *The second proposed CMOS realization*

Although the first ICCII− proposed realization uses a small number of transistors, mismatch between the input transistors can result in a large dc offset between the Y and the X terminals. Moreover, the positive and negative supplies and the threshold voltages of the NMOS and the PMOS transistors are assumed to be equal in magnitude. These limitations can be avoided by using a linear transconductor which depends on two matched CMOS pairs and whose gain is controlled by two extra control voltages and is independent of the supply voltages. Figure 4(*c*) shows the second proposed ICCII− realization. The input stage is formed by a double input transconductor stage which uses four matched CMOS pairs (M1–M2, M3–M4, M5–M6 and M7–M8) and two current mirrors (M9–M10 and M11–M12). For dc offset cancellation, the difference between the two control voltages must equal the difference between the NMOS and the PMOS threshold voltages. The output stage is formed by transistors M13 to M18 and is the same FCS stage as used in the first proposed realization.

5.3. *Simulation results*

The two proposed ICCII− realizations were simulated using PSpice with model parameters of the 1.2 μm CMOS process (vendor: AMI). The supply voltages used were equal to ±2.5 V. The aspect ratios of the two CMOS realizations are given in table 3 and the model parameters used are given in table 4. The simulation results of the first proposed ICCII− realization are shown in figure 5. The dc and ac characteristics between the Y and the X terminals voltages are shown in figures 5(*a*) and

Transistors	W (μm)/L (μm)
M1	30/4.8
M2	97.2/4.8
M3, M4	60/1.2
M5, M6	120/1.2
M7	94.8/3.6
M8	198/3.6

(a)

Transistors	W (μm)/L (μm)
M1, M2, M3, M4, M5, M6, M7, M8	120/3.6
M9, M10	30/3.6
M11, M12	90/3.6
M13, M14	60/1.2
M15, M16	120/1.2
M17	198/3.6
M18	94.8/3.6

(b)

Table 3. Aspect ratios of the two proposed ICCII− CMOS realizations.

```
.MODEL NENH NMOS LEVEL=3 PHI=0.700000 TOX=3.0500E-08 XJ=0.200000U
+TPG=1 VTO=0.95705 DELTA=1.2520E+00 LD=1.7770E-09 KP=7.9173E-05
+ UO=699.3 THETA=1.2260E-01 RSH=9.0910E-02 GAMMA=0.5623
+ NSUB=1.2210E+16 NFS=6.5000E+11 VMAX=2.0250E+05 ETA=1.0560E-01
+ KAPPA=1.9540E-01 CGDO=5.0000E-11 CGSO=5.0000E-11
+ CGBO=3.2665E-10 CJ=2.7366E-04 MJ=5.4287E-01 CJSW=1.7362E-10
+ MJSW=1.0000E-01 PB=9.9000E-01

.MODEL PENH PMOS LEVEL=3 PHI=0.700000 TOX=3.0500E-08 XJ=0.200000U
+TPG=-1 VTO=-0.8351 DELTA=2.1860E+00 LD=1.1000E-09 KP=1.9485E-05
+ UO=172.1 THETA=9.6900E-02 RSH=1.7270E-01 GAMMA=0.3423
+ NSUB=4.5250E+15 NFS=6.5000E+11 VMAX=2.0380E+05 ETA=1.4870E-01
+ KAPPA=9.9980E+00 CGDO=5.0000E-11 CGSO=5.0000E-11
+ CGBO=3.4117E-10 CJ=2.8838E-04 MJ=4.9284E-01 CJSW=2.0216E-10
+ MJSW=1.0000E-01 PB=9.9000E-01
```

Table 4. The 1.2-μm CMOS process parameters.

5(b) respectively. The dc transfer characteristic between the currents I_X and I_Z is shown in figure 5(c) with a dc offset smaller than 0.1 μA. The ac response of I_Z is shown in figure 5(d) with a bandwidth of 55 MHz. The simulation results of the second proposed realization are shown in figure 6. A capacitor of 15 pF with a series resistor of 500 Ω are added at the gate of M13 in order to ensure the stability of the proposed ICCII−.

Simulation results showing a comparison between the two realizations are shown in figure 7. Figure 7(a) shows the improvement in the dc offset between the X and the Y terminals, achieved by using the linear transconductor of the second realization.

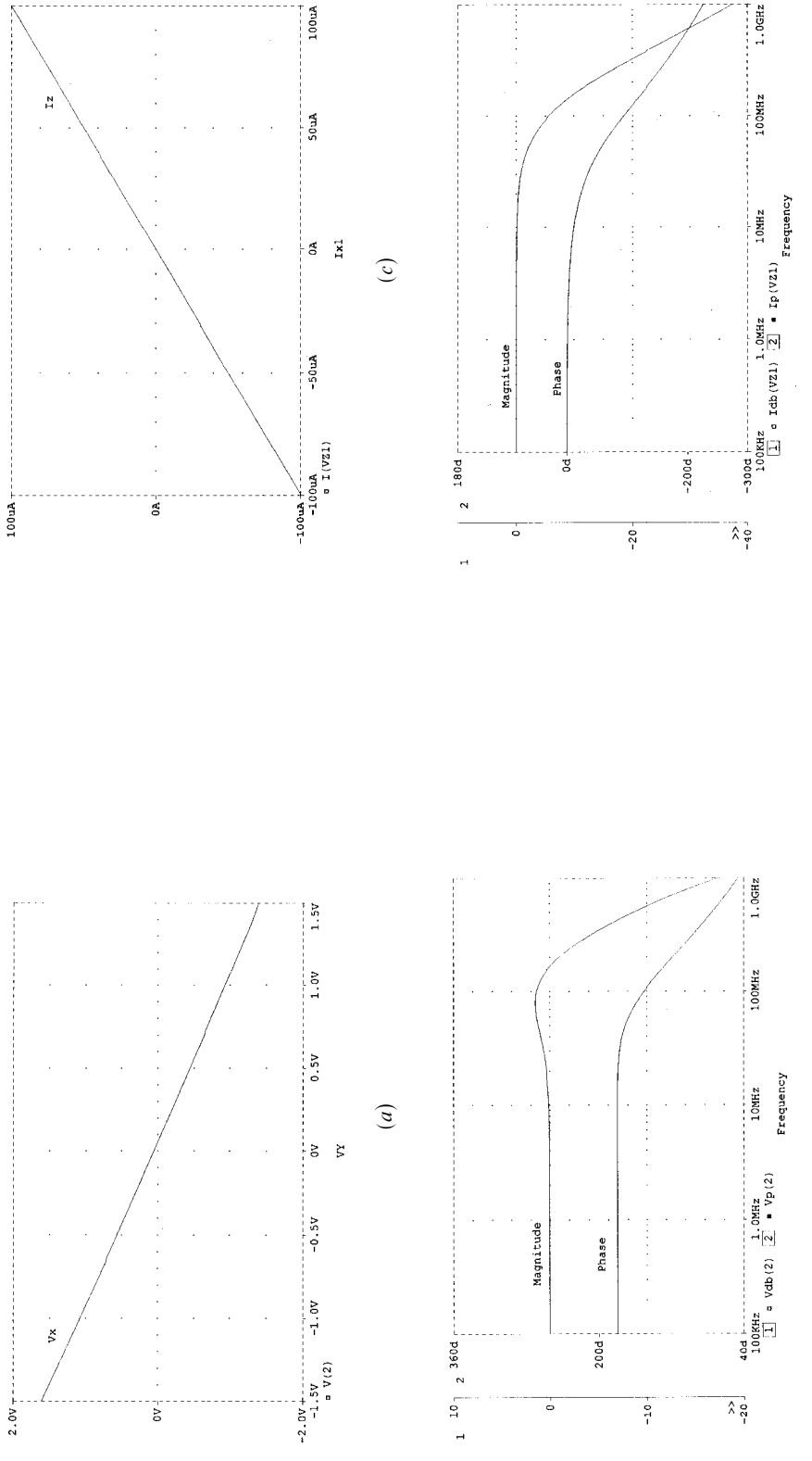


Figure 5. Simulation results of the first proposed ICCII− CMOS realization.

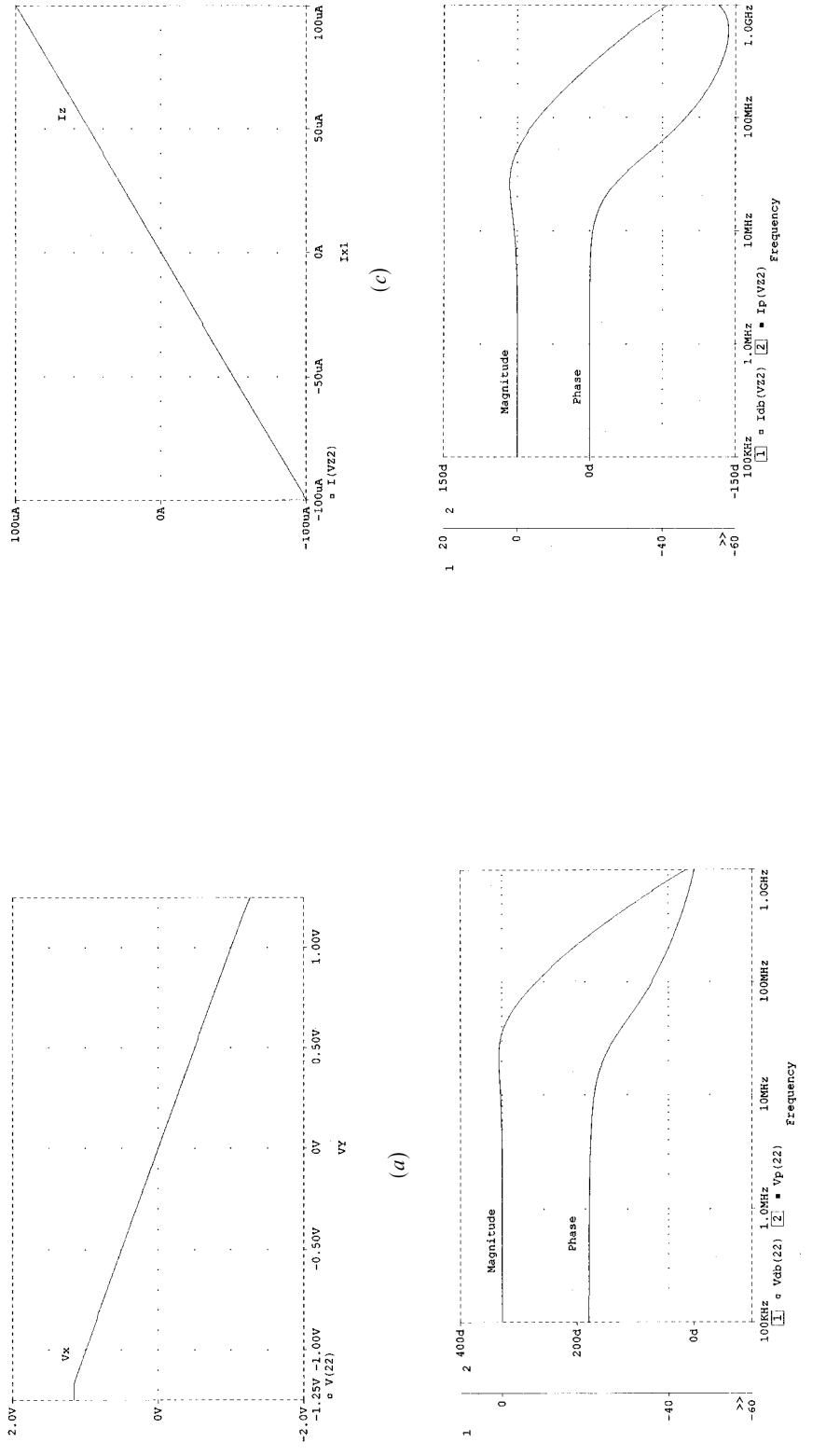
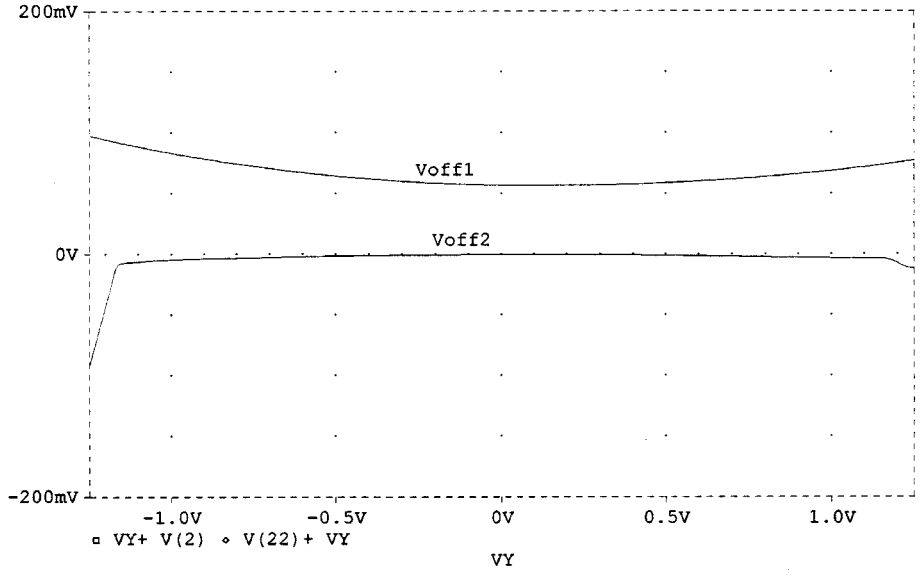
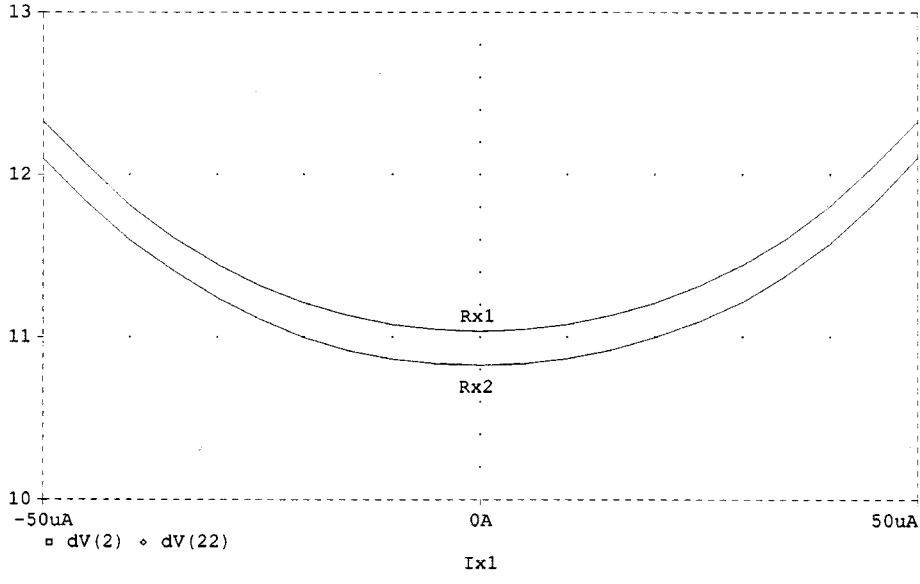


Figure 6. Simulation results of the second proposed ICCII− CMOS realization.



(*a*)



(*b*)

Figure 7. Comparison between the dc offset and R_X of the two proposed realizations.

Figure 7(*b*) shows the improvement in the input resistance seen at the X terminal, achieved by increasing the transconductance gain of the second realization.

6. Applications of the ICCII−

In this section, the ICCII− is used to realize current mode circuits by applying the adjoint transformation to the CCII+ based voltage mode circuits. Recently, new

realizations of the basic zero and pole sections using the CCII+ have been introduced by Soliman (1996). By applying the adjoint transformation to these sections, new ICCII− based sections are obtained. Figure 8(*a*) shows the basic zero section implemented using the CCII+ while figure 8(*b*) shows the new ICCII− basic zero section obtained by applying the adjoint transformation to the circuit of figure 8(*a*). Both sections have the same transfer admittance, given by

$$\frac{I_o}{V_i} = Y_1 - Y_2 \tag{5}$$

Similarly, a new ICCII− based basic pole section is obtained from its CCII+ based counterpart, as shown in figure 9. The transfer impedance is given by

$$\frac{V_o}{I_i} = \frac{1}{Y_A - Y_B} \tag{6}$$

Cascading the basic zero and the basic pole sections shown in figures 8(*a*) and 9(*a*) respectively realizes a voltage transfer function given by

$$\frac{V_o}{V_i} = \frac{Y_1 - Y_2}{Y_A - Y_B} \tag{7}$$

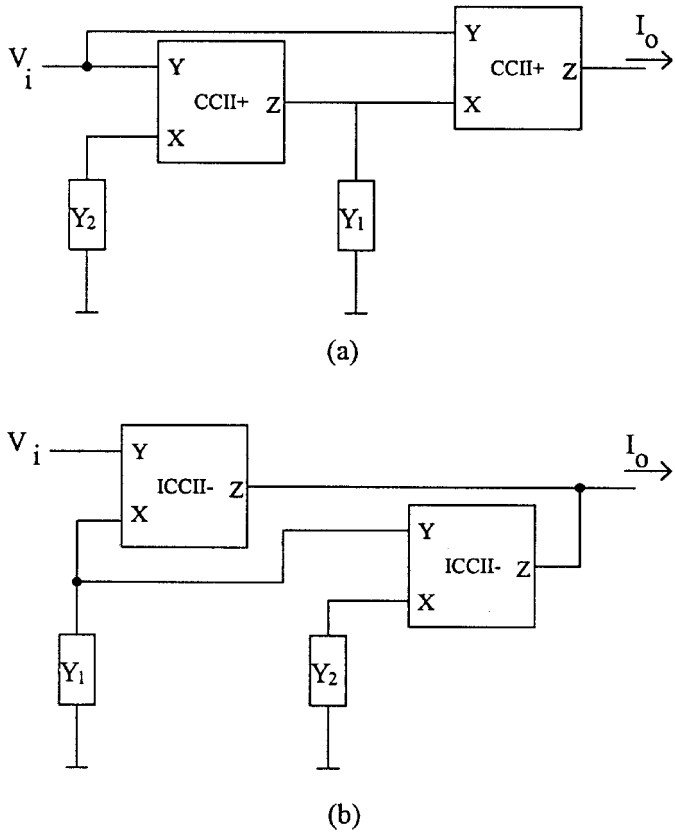


Figure 8. (*a*) The CCII+ based basic zero section. (*b*) The ICCII− based new basic zero section.

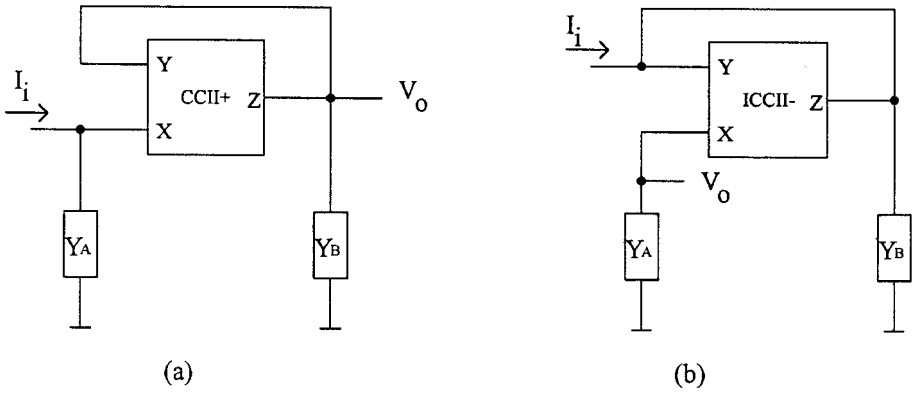
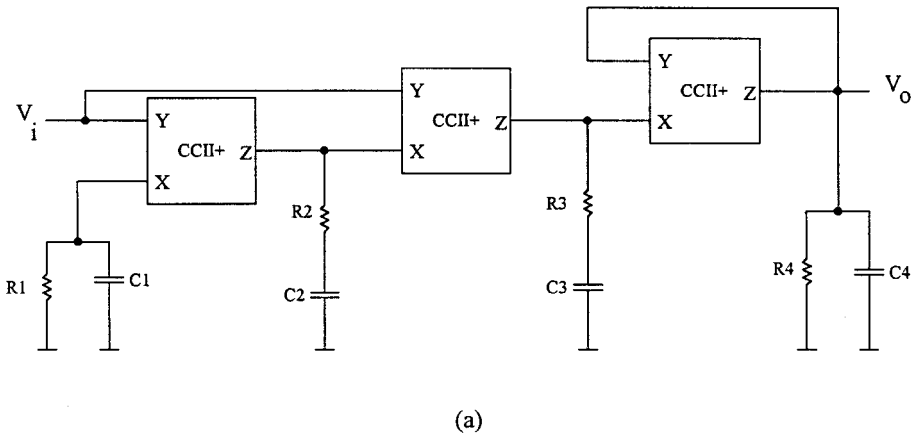


Figure 9. (*a*) The CCII+ based basic pole section. (*b*) The ICCII− based new basic pole section.



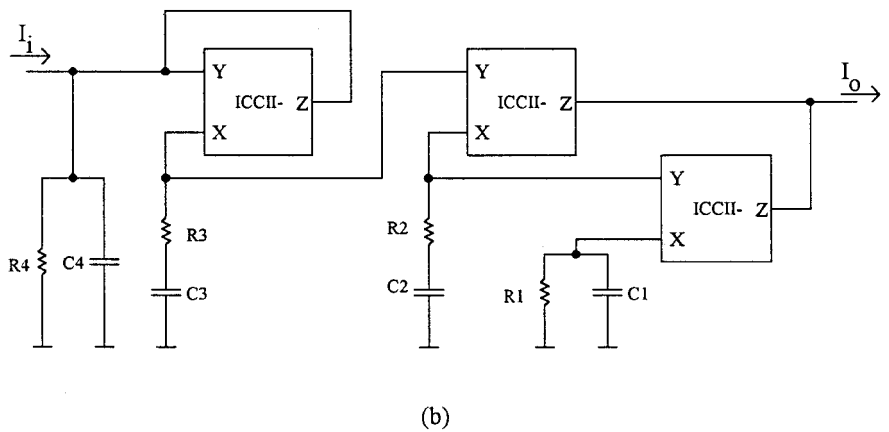


Figure 10. (*a*) The CCII+ based voltage mode allpass filter. (*b*) The ICCII− based new current mode allpass filter.

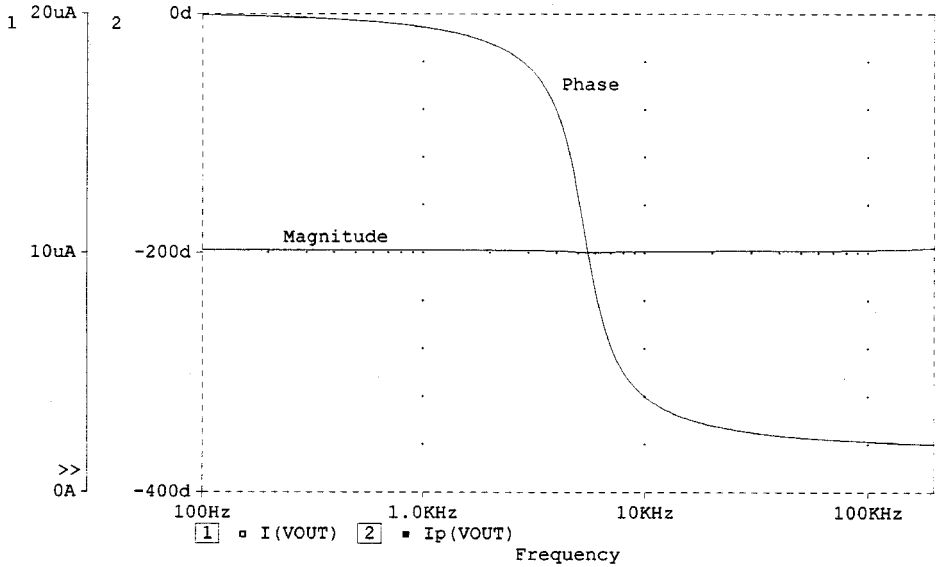


Figure 11. Simulation results of the allpass filter.

6.1. *Example*

In order to realize the current transfer function given by

$$T_i(s) = \frac{s^2 - s + 4}{s^2 + s + 4} \tag{8}$$

consider the voltage transfer function of the same form as given by (8), and divide the numerator and denominator by a polynomial $Q(s) = s + 1$. Apply the RC: CR decomposition and compare with (7); one gets the grounded capacitor circuit shown in figure 10(*a*). The resulting resistor and capacitor values are: $R_1 = R_4 = 1/4\ \Omega$, $R_2 = 1/6\ \Omega$, $R_3 = 1/4\ \Omega$, $C_1 = C_4 = 1$ F, $C_2 = 6$ F and $C_3 = 4$ F.

The new ICCII− based current mode allpass filter, shown in figure 10(*b*), is obtained by applying the adjoint network theorem to the above CCII+ based voltage mode filter. The same current mode filter can be obtained by cascading the basic pole and the basic zero sections of figures 9(*b*) and 8(*b*) respectively. PSpice simulations have been carried out for the circuit of figure 10(*b*), using the first proposed ICCII− realization, after scaling all resistors by 6×10^4 and all capacitors by 10^{-9} and taking $I_i = 10\ \mu$A. Figure 11 represents the magnitude and phase responses for the output current I_o.

7. Conclusions

The current mirror and the voltage mirror elements were defined and used together with the nullator and norator elements in order to simplify the representation of different building blocks in the ideal case. Two new building blocks (the ICCII− and the ICCII+) were added to the CCII family. Both current conveyors exhibit an inverting property between the X and the Y terminals. The ICCII− is the adjoint building block of the CCII+ while the ICCII+ is self adjoint. New CMOS realizations of the ICCII− were proposed. PSpice simulations using the 1.2 μm

CMOS process have been carried out. R_X smaller than 11 Ω, bandwidth of up to 55 MHz and low dc offset were obtained. New basic zero and basic pole sections using the ICCII− were realized by applying the adjoint network theorem to the CCII+ based sections. Finally, a new allpass filter implemented using the ICCII− was presented.

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