*Frequenz*
*57 (2003)*
*9–10*

# New CMOS Compound Current Conveyor

**Ein neuer CMOS-Compound-Current-Conveyor**

Abstract
A new Compound CMOS current conveyor based on the block diagram introduced by Barthelemy and Fabre is presented. The circuit provides very low input impedance, wide voltage transfer bandwidth as well as equal current transfer bandwidths for the CCII$^+$ and CCII$^-$ sections. As an application example, Elwan and Soliman electronically tunable current-mode filter is implemented. Simulation results are included.

Übersicht
Einer neuer „Compound-CMOS-Current-Conveyor" auf der Basis eines von Barthelemy und Fabre eingeführten Block-Diagramms wird vorgestellt. Die Schaltung bietet eine sehr kleine Eingangsimpedanz, eine breite Spannungsübertragungsbandbreite sowie gleiche Stromübertragungsbandbreiten für die CCII$^+$ als auch für die CCII$^-$ Sektionen. Als ein Anwendungsbeispiel wird ein elektronisch abstimmbares Filter vom Strom-Typ nach der Idee von Elwan und Soliman implementiert. Simulationsergebnisse werden mitgeteilt.

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Für die Dokumentation
CMOS-Technik / Compound Current Conveyor / abstimmbares Filter

## 1. Introduction

In 1968 Smith and Sedra introduced the first generation current conveyor (CCI) [1] and in 1970 the second generation current conveyor (CCII) was proposed by the same authors [2]. Since then CCII, which is essentially a combined voltage and current buffer, has proved to be functionally flexible and versatile, rapidly gaining acceptance as both a theoretical and practical building block [3, 4]. Current conveyors and related current-mode circuits have begun to emerge as an important class of circuits with properties that enable them to rival their voltage-mode counterparts in a wide range of applications. Current-mode circuits are suitable to operate under low voltage supplies since voltage swings are substituted by current swings in signal propagation. Key performance features of current-mode signal processing are wideband capability and a wide dynamic range under low power operation [5].

In some current-mode applications both CCII$^+$ and CCII$^-$ types are required [6, 7]. A balanced output CCII acts as CCII$^+$ and CCII$^-$ simultaneously. It can be straightforwardly implemented by inverting the output current of a given type of CCII by a current mirror to obtain the other type. However, this current mirror introduces an additional pole that causes degradation in the current transfer bandwidth of the additional CCII type [8].

Another problem in basic CMOS current conveyors is their large input resistance usually in the order of several kilo-ohms. CMOS realizations featuring low input resistance in the order of several ohms have been proposed in [9–12]. Also, the CCII proposed in [13] features very low input resistance in the order of a several milliohms. However, it sacrifices the voltage and current transfer bandwidths in return.

The objective of this paper is to present a new balanced output class-A CMOS CCII based on the block diagram introduced by Barthelemy and Fabre in [14]. The proposed circuit exhibits wide voltage transfer bandwidth, equal current transfer bandwidths for the CCII$^+$ and CCII$^-$ sections, as well as very low input resistance in the order of several milliohms.

A comparison between the proposed CCII and the CCII presented in [11] and shown in **Fig. 1** is held to show the benefits gained by the new architecture. Both circuits are designed following a fair comparison criterion that has the following constraints [15]. Firstly, both circuits operate under the same supply voltages. The supply voltages are equal to 1.5 V and –1.5 V. Secondly, aspect ratios of equivalent transistors are equal and equivalent current sources are identical. The reference DC current source $I_B$ is taken as 100 μA. Thirdly, simulations are carried out with the same model and under the same circumstances. TOP SPICE simulations were carried out with level 8 model parameters of 0.5 μm CMOS process provided by MOSIS (AGILENT).

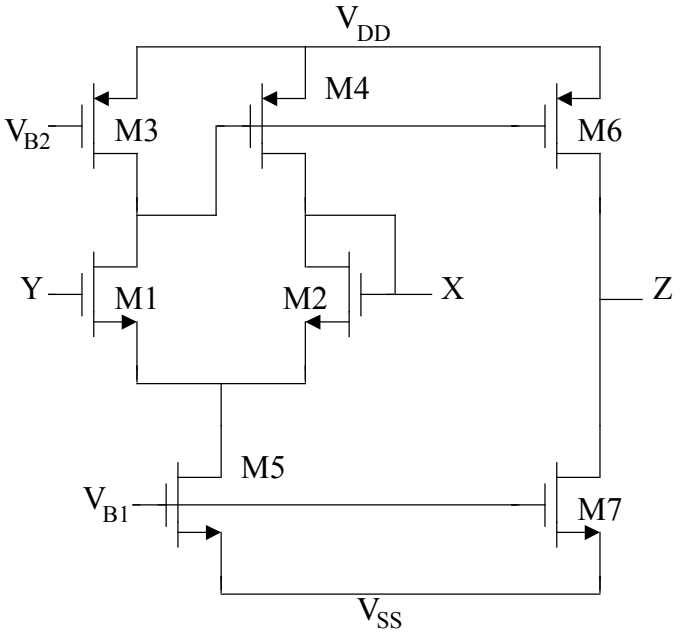


Fig. 1: The CCII realization proposed in [11]

Finally, as an application example, the electronically tunable current-mode filter which is proposed by Elwan and Soliman in [6] is implemented and simulated.

## 2. The Proposed CMOS-Compound CCII

### 2.1 Circuit Description

The CMOS realization of the proposed balanced output CCII is shown in **Fig. 2**. The groups of the transistors ($M_1$–$M_4$), ($M_5$–$M_9$), ($M_{10}$ and $M_{11}$), ($M_{12}$, $M_{14}$ and $M_{16}$), as well as ($M_{13}$ and $M_{15}$) are matched. Assuming that all the transistors operate in their saturation regions, the operation of the circuit can be explained as follows. Transistors from $M_{10}$ to $M_{16}$ serve as DC current sources. Each of the transistors $M_{10}$, $M_{11}$, $M_{12}$, $M_{14}$ and $M_{16}$ holds $I_B$. Each of the transistors $M_{13}$ and $M_{15}$ holds $2I_B$. The circuit consists of two long tail pairs ($M_1$ and $M_3$) and ($M_2$ and $M_4$). Consequently, the current flowing through M3 is forced to be equal to that flowing through $M_1$ and equals $I_B$ causing the gate-to-source voltages of $M_1$ and $M_3$ to be equal. The result is that the gate voltage of $M_3$ equals the input voltage at terminal *Y*. Similarly, the gate voltage of $M_3$ is transferred to terminal *X*. As a result the voltage at termi-

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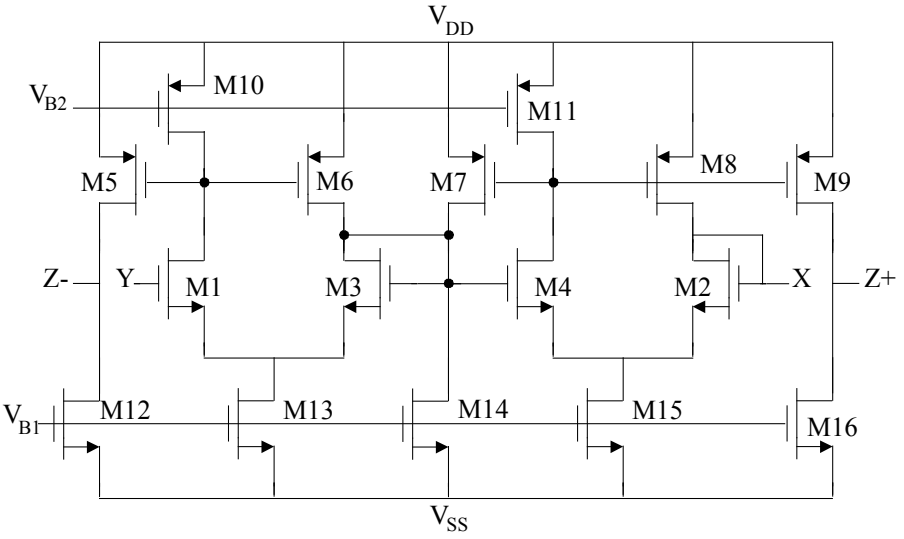


Fig. 2: The proposed CMOS Compound CCII

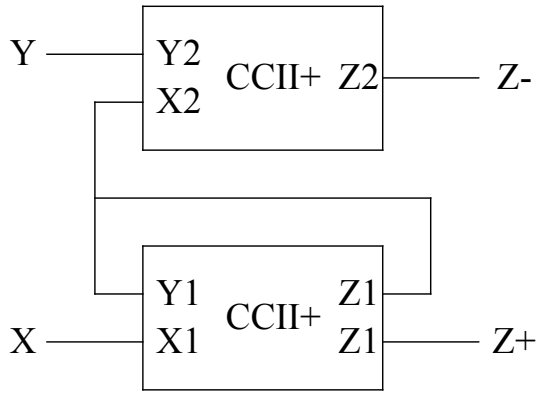


Fig. 3: Block diagram of the circuit shown in Fig. 2 [14]

nal *X* follows that at terminal *Y*. The common source transistors ($M_8$ and $M_9$) are responsible for conveying the *X* terminal current to terminal $Z^+$. It can be easily noted that the *X* and $Z^+$ terminals currents have the same direction. The common source transistors ($M_5$ and $M_6$) are responsible for conveying the *X* terminal current to terminal $Z^-$. However, the *X* and $Z^-$ terminals currents flow in opposite directions.

The block diagram of the proposed CCII is shown in **Fig. 3**. It includes two CCII circuits where the first CCII has two *Z* terminals. The *Y* and one of the *Z* terminals of the first CCII are connected together (forming a CCI), then connected to terminal *X* of the second CCII. This block diagram was first introduced by Barthelemy and Fabre in [14]. It was used without the $Z^-$ terminal to achieve a $CCII^+$ with reduced input resistance at terminal *X*. In this paper, by adding the $Z^-$ terminal, the block diagram is used to achieve a balanced output CMOS CCII (Compound CCII)with reduced input resistance at terminal *X*. If the two CCII blocks are ideal, i. e. having unity voltage and current transfer gains as well as infinite output resistances at the *Z* terminals, the input resistance of the proposed CCII can be given by

$$r_x = r_{x1} - r_{x2} \tag{1}$$

Not to add much complexity, the simplest $CCII^+$ proposed by Palmisano and Palumbo in [11] is used as a building block while realizing the block diagram shown in Fig. 3. The proposed circuit exhibits voltage transfer gain very close to unity due to the local negative feedback actions on the drains of $M_2$ and $M_3$. The equations of the voltage transfer gain and the input resistance at terminal *X* are approximately given by:

Table 1: Transistors aspect ratios of the circuit shown in Fig. 2

| Transistor | *W*(μm)/*L*(μm) |
|---|---|
| $M_1$–$M_4$ | 60/1 |
| $M_5$–$M_9$ | 100/2.5 |
| $M_{10}$, $M_{11}$ | 100/2.5 |
| $M_{12}$, $M_{14}$, $M_{16}$ | 50/2.5 |
| $M_{13}$, $M_{15}$ | 100/2.5 |

$$\frac{v_x}{v_y} = \frac{g_{m1}\left(g_{m6}+g_{d10}\right)}{g_{m1}\left(g_{m6}+g_{d10}\right)+\left(g_{d1}+2g_{d10}\right)\left(g_{d6}+g_{d14}+\dfrac{g_{d7}g_{d11}}{g_{m8}+g_{d11}}\right)} \tag{2}$$

$$r_x = \left(\frac{g_{d1}+2g_{d10}}{g_{m4}\left(g_{m8}+g_{d10}\right)}\right)\left(\frac{g_{m1}\left(g_{m6}+g_{d10}-g_{m7}\right)+g_d\left(g_{d1}+2g_{d10}\right)}{g_{m1}\left(g_{m6}+g_{d10}\right)+g_d\left(g_{d1}+2g_{d10}\right)}\right) \tag{3}$$

where $g_d + g_{d6} = g_{d7} + g_{d14}$, $g_{m1} = g_{m2} = g_{m3} = g_{m4}$, $g_{d1} = g_{d4}$, $g_{d7} = g_{d8}$ and $g_{d10} = g_{d11}$.

The output resistances at terminal $Z^+$ and $Z^-$ are given by:

$$r_{z^+} = \frac{1}{g_{d9}+g_{d16}} \tag{4}$$

$$r_{z^-} = \frac{1}{g_{d5}+g_{d12}} \tag{5}$$

### 2.2 Simulation Results

Transistors aspect ratios are reported in **Table 1**. Simulation results are tabulated in **Table 2** and shown in figures numbered from 3 to 6. These results can be described as follows. The input voltage range is from –0.32 V to 0.6 V. The average value of the open circuit voltage transfer gain equals 0.9997. The voltage offset varies from –0.65 mV to 0.9 mV within the input voltage range. The open circuit voltage transfer bandwidth exhibits a 3-dB frequency of 550 MHz (**Fig. 4**). The input current range equals 200 μA. For the $CCII^+$ section, the average value of the short circuit current transfer gain equals to 0.9947, the current offset varies from 0.025 μA to 2.32 μA within the input current

Table 2: Parameters of the circuits shown in Fig. 1 and Fig. 2

| Parameter | Unit | Palmisano CCI [8] | Proposed CCII |
|---|---|---|---|
| Input voltage range | V | –0.3 to 0.7 | –0.32 to 0.6 |
| $A_v$ (average value) | – | 1.00014 | 0.9997 |
| Maximum deviation from $A_v$ | – | 1.79 % | 2 % |
| Voltage offset variation | mV | –0.642 to 0.506 | –0.65 to 0.9 |
| $F_{3db}$ of voltage transfer gain | MHz | 1800 | 550 |
| Input current range | μA | –100 to 100 | –100 to 100 |
| $A_i$ (average value) for $CCII^+$ | – | 0.9946 | 0.9947 |
| Maximum deviation from $A_i$ for $CCII^+$ | – | 8.7 % | 8.7 % |
| Current Offset variation for $CCII^+$ | μA | 0.583 to 2.35 | 0.025 to 2.32 |
| $F_{3db}$ of current transfer gain for $CCII^+$ | MHz | 94.5 | 53.7 |
| $A_i$ (average value) for $CCII^-$ | – | – | 0.9894 |
| Maximum deviation from $A_i$ for $CCII^-$ | – | – | 8.7 % |
| Current Offset variation for $CCII^-$ | μA | – | –1.7 to 1.47 |
| $F_{3db}$ of current transfer gain for $CCII^-$ | MHz | – | 47 |
| $R_x$ | Ω | 14.63 | 0.2 |
| THD for a sinusoid of 100 kHz | – | 0.05539 % | 0.1055 % |

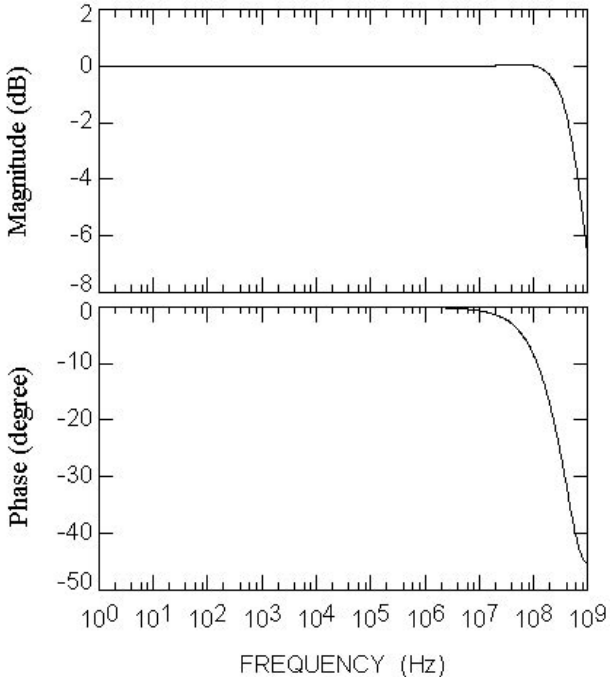


Fig. 4: Frequency characteristics of the open circuit voltage transfer gain between *Y* and *X* ($V_X/V_Y$) for the circuit shown in Fig. 2

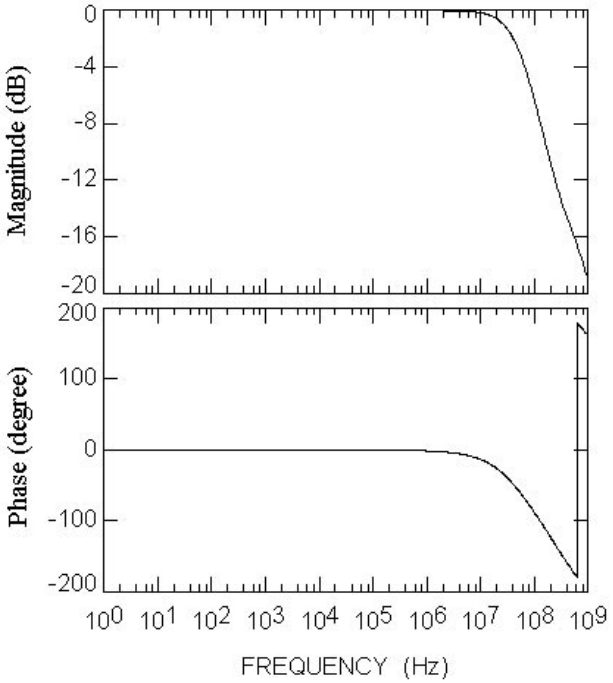


Fig. 5: Frequency characteristics of the short circuit current transfer gain between *X* and $Z^+$ ($I_{Z^+}/I_X$) for the circuit shown in Fig. 2

range and the short circuit current transfer bandwidth exhibits a 3-dB frequency of 53.7 MHz (**Fig. 5**). For the $CCII^-$ section, the average value of the short circuit current transfer gain equals to 0.9894, the current offset varies from –1.7 μA to 1.47 μA within the input current range and the short circuit current transfer bandwidth exhibits a 3-dB frequency of 47 MHz (**Fig. 6**). The input resistance at terminal X at D.C equals 0.2 Ω. Finally, the total harmonic distortion (THD) for an input sinusoid of frequency 100KHz and amplitude 0.5 V p-p is 0.1055 %.

To ensure the stability of the proposed architecture, the transient response of the circuit is simulated for an input square wave at terminal *X*. The input square wave has 0.9 V peak to peak amplitude, 1 MHz fundamental frequency and 1 ns rise/fall times. The output at terminal *Y* is shown in **Fig. 7**. It can be noticed that it represents a faithful replica of the input square wave with no overshoots or oscillations.

A fair comparison can be held between the $CCII^+$ section of the proposed CCII and Palmisano-Palumbo CCII. From Table 2, one can easily notice what follows. Both circuits exhibit almost the same results regarding input voltage and current ranges as well as transfer gains and offsets. Also, the proposed CCII has the advantage of a much lower input resistance than the case of Palmisano-Palumbo CCII. It drops from 14.63 Ω to 0.2 Ω paying some loss in bandwidths which is yet acceptable in many applications. Moreover, a $Z^-$ terminal with the same short circuit current transfer bandwidth as the $Z^+$ terminal is achieved.

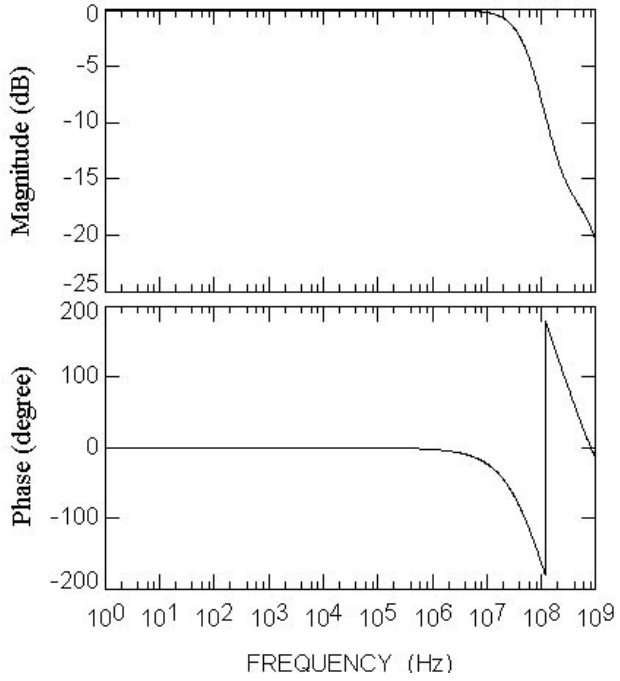


Fig. 6: Frequency characteristics of the short circuit current transfer gain between $X$ and $Z^-$ ($I_{Z^-}/I_X$) for the circuit shown in Fig. 2

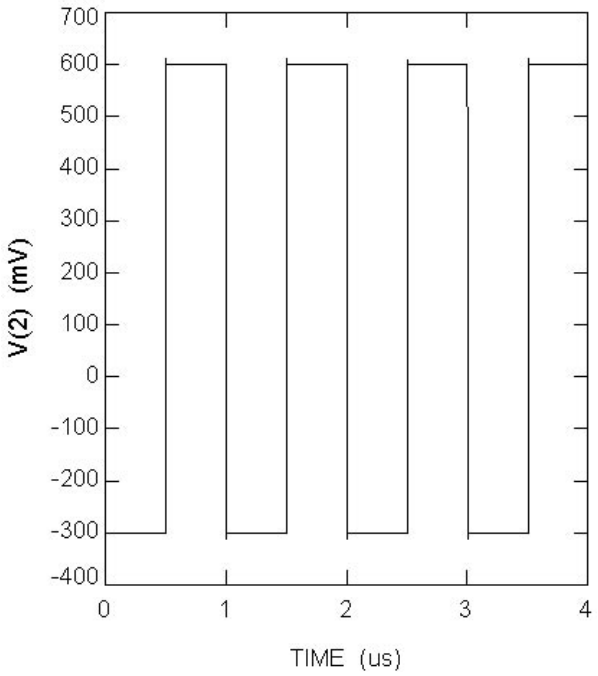


Fig. 7: The transient response of the circuit shown in Fig. 2

## 3. Elwan and Soliman Electronically Tunable Current Mode Filter

### 3.1 Circuit description

The electronically tunable current-mode second order low-pass band pass filter proposed in [6] is shown in **Fig. 8**.

Assuming ideal current conveyors, the low-pass and the band-pass current transfer functions of the filter are given by:

$$\frac{I_{LP}}{I_i} = \frac{\dfrac{1}{C_1C_2R_1R_2}}{s^2 + \dfrac{s}{C_1R} + \dfrac{1}{C_1C_2R_1R_2}} \tag{6}$$

$$\frac{I_{BP}}{I_i} = \frac{\dfrac{s}{C_1R_2}}{s^2 + \dfrac{s}{C_1R} + \dfrac{1}{C_1C_2R_1R_2}} \tag{7}$$

The center frequency and the quality factor of the filter are given by:

$$\omega_o = \frac{1}{\sqrt{C_1C_2R_1R_2}} \tag{8}$$

$$Q = R\sqrt{\frac{C_1}{C_2R_1R_2}} \tag{9}$$

The center frequency gain of the band-pass filter is given by:

$$T(j\omega_o) = \frac{R}{R_2} \tag{10}$$

Practically, this filter requires very low input impedance balanced output current conveyors because its center frequency and quality factor are sensitive to $r_{x1}$ and $r_{x2}$. Consequently, the new balanced output CCII proposed in this paper fits in such application in order to obtain minimized shifts in the center frequency and the quality factor.

### 3.2 Simulation results

**Fig. 9** shows the band-pass current response of the filter where the input current is 100 μA (peak to peak). The Capacitor values are $C_1$ = 1 nF and $C_2$ = 0.4 nF. The resistors are adjusted such that $R_1 = R_2 = R/4 = r$. The current gain at the center frequency equals to $R/R_2$ = 4. The center frequency is scanned by electronically tuning the value of $r$ from 2 KΩ to 3 KΩ.

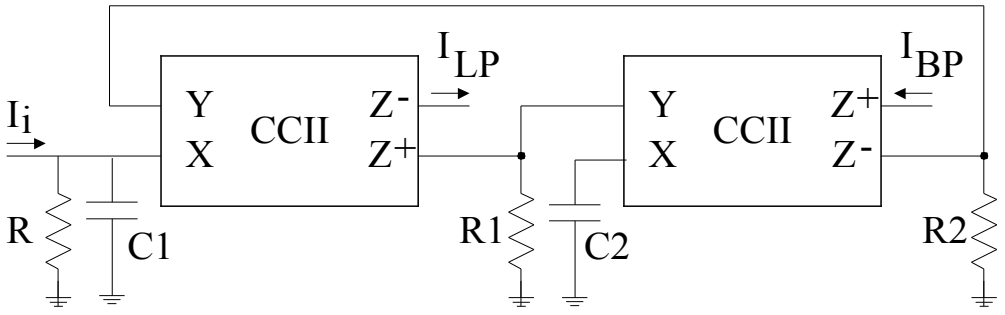


Fig. 8: The current mode low-pass band-pass filter proposed in [6]

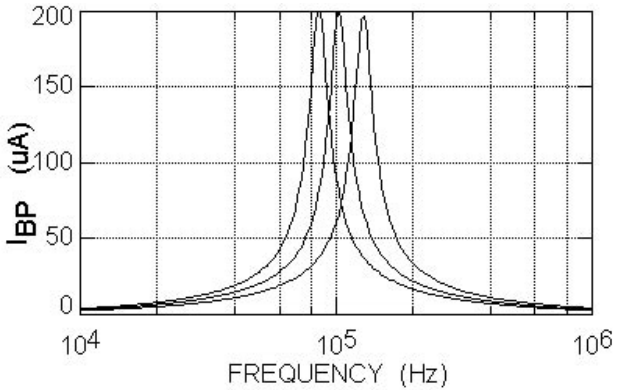


Fig. 9: The electronically tuned band-pass response of the current-mode filter

### 4. Conclusions

A new balanced output CMOS current conveyor was introduced in this paper. Simulation results showed that the circuit features very low input resistance, wide voltage transfer bandwidth as well as equal current transfer bandwidths for $CCII^+$ and $CCII^-$. To prove the strength of the proposed architecture, Elwan and Soliman electronically tunable current-mode filter was implemented using the new CCII.

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(Received on July 6, 2003)