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# PATHOLOGICAL REALIZATIONS OF BOTA AND FDDTA USING GROUNDED RESISTORS*

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Sixteen pathological realizations of the balanced output transconductance amplifier (BOTA) using four grounded G are generated. Each of these circuits is realizable using four current conveyors (CCII) or four inverting current conveyors (ICCII) or a combination of four CCII and ICCII. Six new pathological realizations of the BOTA using two grounded $G$ based on current subtraction are introduced. Four new pathological realizations of the BOTA using two grounded $G$ based on voltage subtraction are introduced. Several new pathological realizations of the FDDTA as a voltage subtraction stage and a BOTA stage are also given. Simulation results are included.

*Keywords*: Balanced output transconductor; nullator; norator; voltage mirror; current mirror.

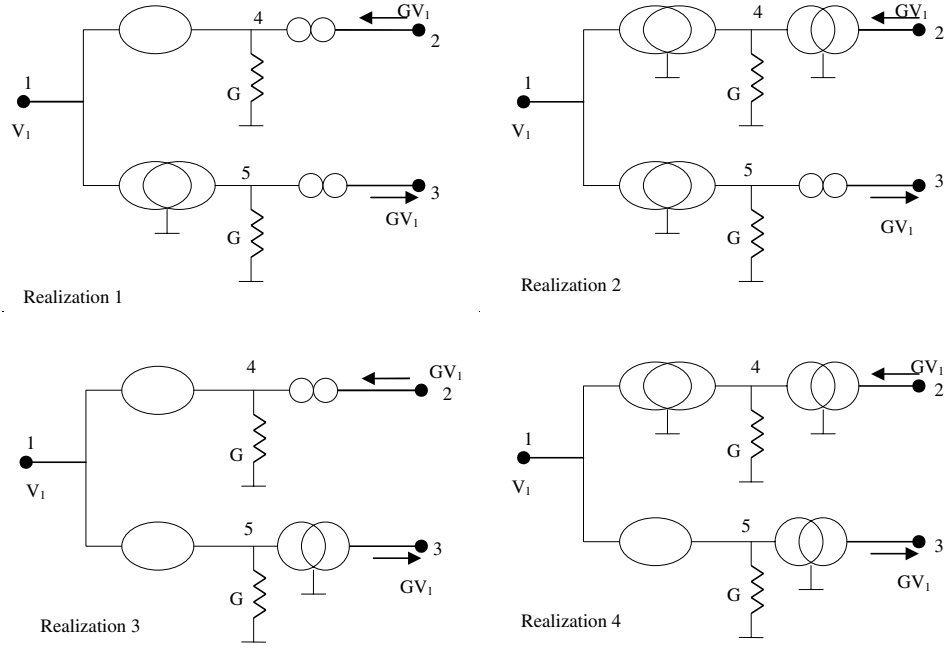
## 1. Introduction

Recently a systematic generation method of transconductance amplifiers (TA) based on using nullator, norator elements and pathological mirror elements was used to provide pathological realizations of different types of TA.[1] Four pathological realizations of the single input balanced output TA, each uses two grounded $G$, were given and are summarized in Table 1. Four pathological realizations of the differential input single output TA, each uses two grounded $G$, were given and are summarized in Tables 2 and 3 for the two polarities of the output current of the TA. Six pathological realizations of the differential input balanced output TA known as balanced output transconductance amplifier (BOTA) were given in Ref. 1, four of them employ a floating $G$ and each of the remaining two realizations employ two grounded $G$. Since long time there was an interest in using nullor elements[2] to represent the TA and this has been demonstrated in the literature by several authors.[3–7]

The realizations given in Ref. 1 however are based on using nullor elements together with the additional pathological elements called mirror elements that were introduced in Refs. 8–10 to describe the voltage and current reversing actions.

*This paper was recommended by Regional Editor Piero Malcovati.

Table 1. Pathological realizations of the single input balanced output TA.

| Four realizations of the single input balanced output TA[1] |
|---|
|  |



The voltage mirror (VM), shown in Fig. 1(a), is a lossless two-port network element used to represent an ideal voltage reversing action and it is described by:

$$V_1 = -V_2\,, \tag{1a}$$

$$I_1 = I_2 = 0\,. \tag{1b}$$

Table 2. Pathological realizations of the differential input single output TA$^-$.

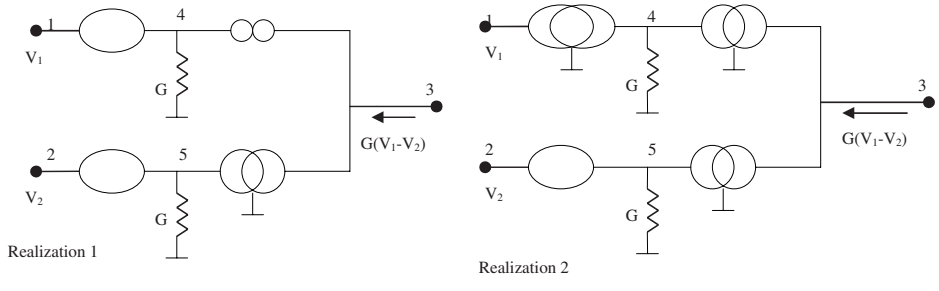
| Four realizations of the differential input single output TA$^{-1}$ |
|---|
|  |

Table 2. (*Continued*)

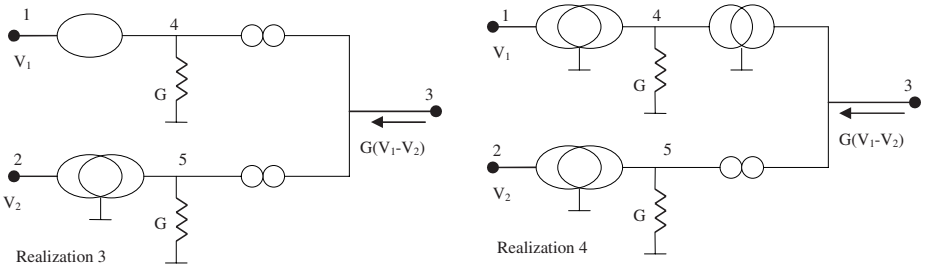
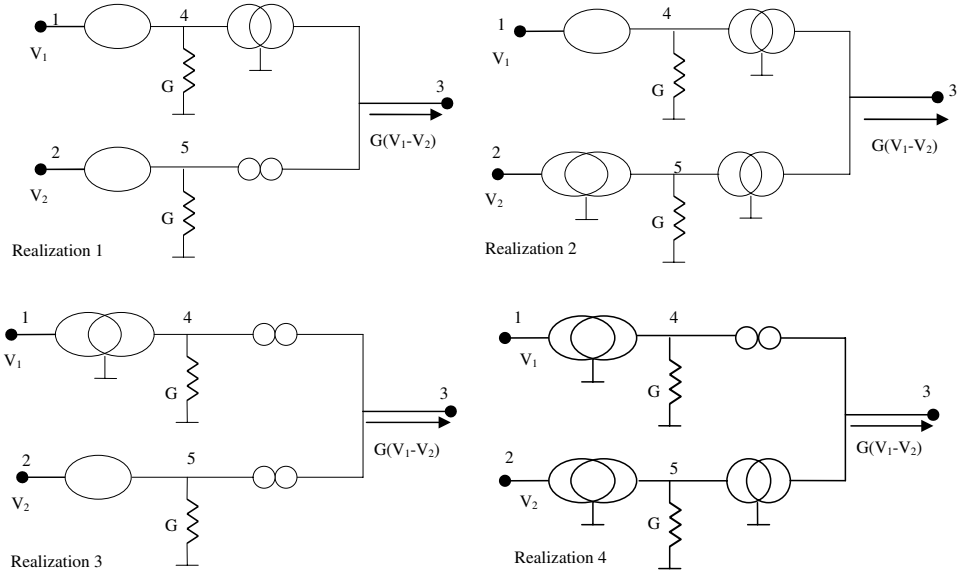
| Four realizations of the differential input single output $TA^{-1}$ |
|---|
|  |



Table 3. Pathological realizations of the differential input single output $TA^{+}$.

| Four realizations of the differential input single output $TA^{+}$ |
|---|
|  |



The current mirror (CM), shown in Fig. 1(b), is a two-port network element used to represent an ideal current reversing action and it is described by:

$$V_1 \text{ and } V_2 \text{ are arbitrary}, \tag{2a}$$

$$I_1 = I_2, \text{ and they are also arbitrary}. \tag{2b}$$

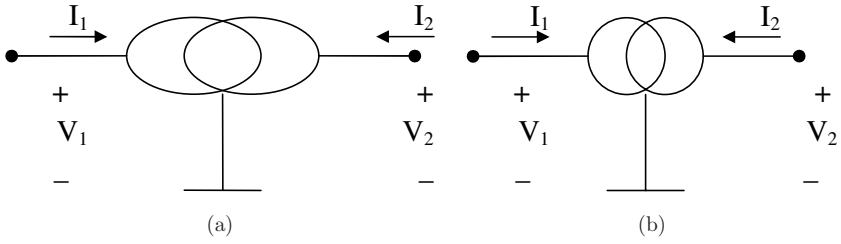



Fig. 1. (a) Voltage mirror and (b) Current mirror.

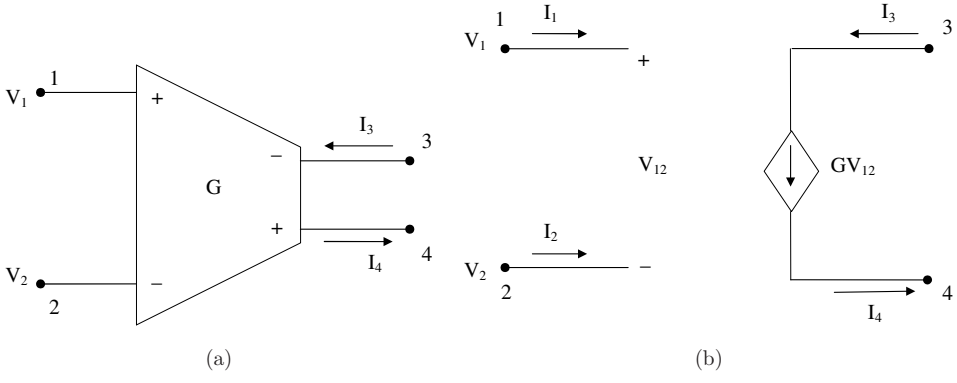



Fig. 2. (a) Symbolic representation of the BOTA and (b) equivalent VCCS model for the BOTA.

In this paper new pathological realizations of the BOTA and of the fully differential difference balanced output TA (FDDTA) using grounded $G$ are introduced.

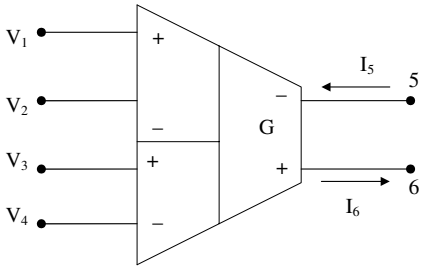
## 2. NAM of BOTA and of FDDTA

The BOTA is represented symbolically as shown in Fig. 2(a) and is represented by the voltage controlled current source model shown in Fig. 2(b). The nodal admittance matrix (NAM) of the BOTA is given by:

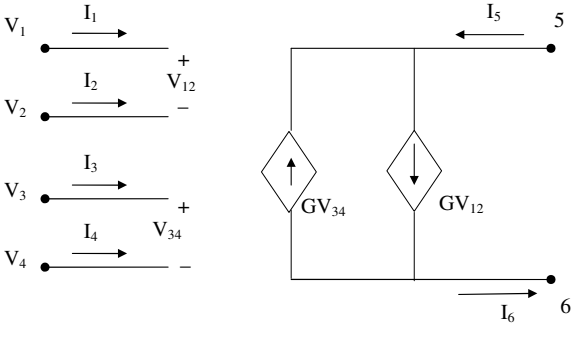
$$Y = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ G & -G & 0 & 0 \\ -G & G & 0 & 0 \end{bmatrix}. \tag{3}$$

From Fig. 2(b) it is seen that the BOTA is a floating active building block.

The FDDTA is represented symbolically as shown in Fig. 3(a)[11,12] and is represented by the voltage controlled current source model shown in Fig. 3(b).




(a)




(b)

Fig. 3. (a) Symbolic representation of the DDTA and (b) equivalent VCCS model for the DDTA.

The admittance matrix of the FDDTA is given by:

$$Y = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ G & -G & -G & G & 0 & 0 \\ -G & G & G & -G & 0 & 0 \end{bmatrix}. \tag{4}$$

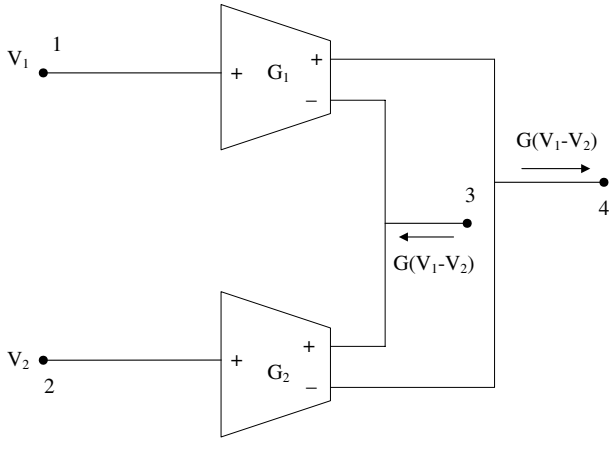
From Fig. 3(b) it is seen that the FDDTA is a floating active building block.

## 3. Realization of BOTA from other TA Using Four Grounded G

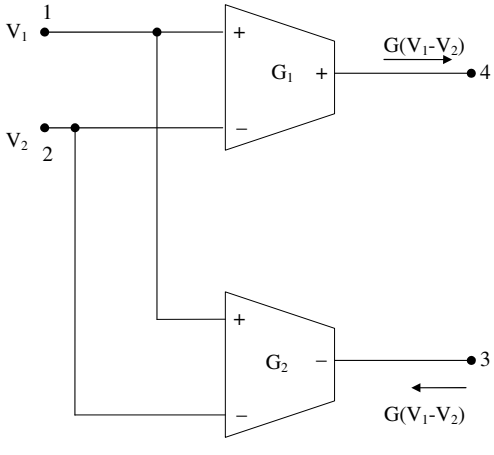
In this section new realizations of the BOTA using grounded $G$ derived from other types of TA as well as from current conveyors (CCII)[13] or inverting current conveyors (ICCII)[8] are introduced.

The BOTA can be realized from two matched single input balanced output TA as shown in Fig. 4(a). Two differential input single-output TA having equal $G_1$ and $G_2$ can also be used to realize the BOTA as given in Figs. 4(b)–4(d).[14]

Four new pathological realizations of the BOTA using four grounded $G$ can be generated from the circuit of Fig. 4(a) using the realizations given in Table 1. Figure 5(a) represents a new pathological realization of the BOTA based on realization 1 in Table 1 and it employs two nullators, two VM and four norators. Figure 5(b) is based on using realization 3 in Table 1 to realize Fig. 4(a) and it represents another new pathological realization of the BOTA using four nullators, two CM and two norators. This realization is the adjoint[15,16] of the BOTA circuit of

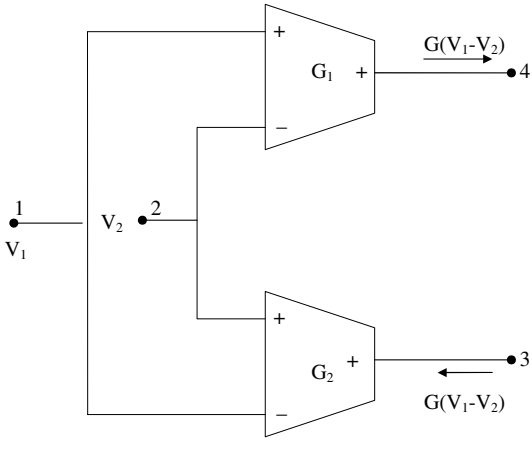



(a)

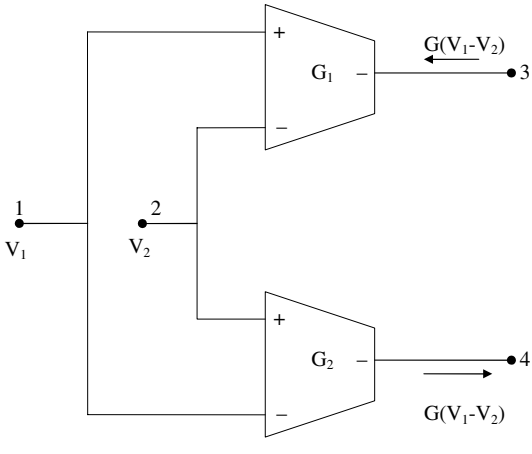



(b)

Fig. 4. (a) Realization of BOTA from two matched single input balanced output TA. (b) Realization of BOTA from two matched differential input single output TA. (c) Realization of BOTA from two matched differential input single output TA. (d) Realization of BOTA from two matched differential input single output TA.




(c)




(d)

Fig. 4. (*Continued*)

Fig. 5(a) after interchanging the two input and two output ports. Figure 5(c) is based on using realization 2 in Table 1 to realize Fig. 4(a) and Fig. 5(d) is based on using realization 4 in Table 1 to realize Fig. 4(a).

The same circuits of Fig. 5 can be generated from Fig. 4(b) using the pathological realizations of the differential input single output TA given in Tables 2 and 3. For example Fig. 5(a) is obtainable from realization 3 in Table 3 to realize $G_1$ and realization 3 in Table 2 to realize $G_2$.

There are twelve more pathological realizations of the BOTA that can be generated using two alternative circuits from Table 1 to realize Fig. 4(a) as will be explained next.

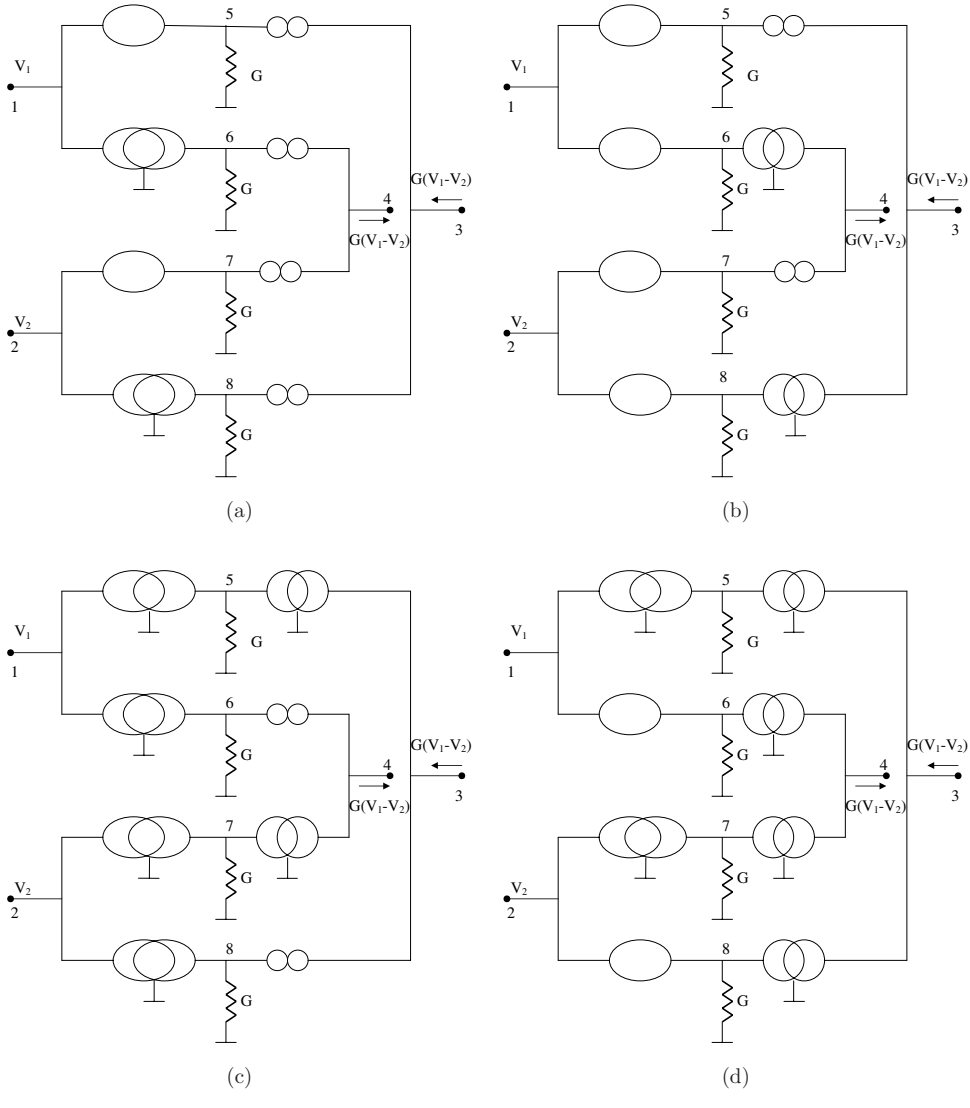



Fig. 5. (a) Realization 1 of BOTA using four grounded $G$. (b) Realization 2 of BOTA using four grounded $G$. (c) Realization 3 of BOTA using four grounded $G$. (d) Realization 4 of BOTA using four grounded $G$.

## 4. CCII and ICCII Realizations of BOTA

The pathological realization given in Fig. 5(a) can be realized using two CCII− and two ICCII−. It is desirable to obtain all other CCII and ICCII realizations of the BOTA using four grounded $G$. Since the BOTA circuit topology is known it can be generalized as shown in Fig. 6 where the generalized conveyor (GC) is

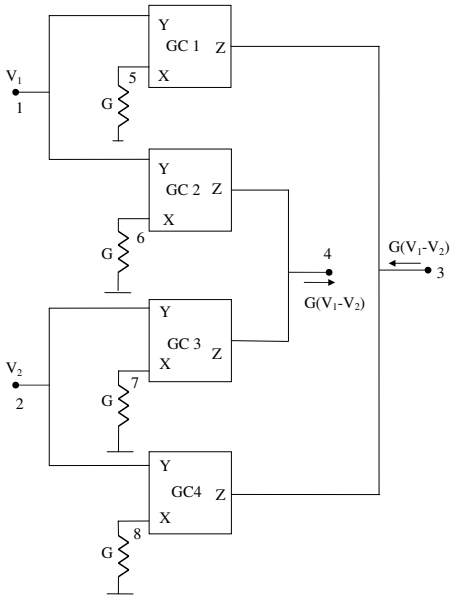



Fig. 6. Generalized realization of BOTA using four grounded $G$.

defined by:

$$I_Y = 0, \quad V_X = aV_Y \quad \text{and} \quad I_Z = KI_X\,, \tag{5}$$

where $a = 1$ for CCII and $a = -1$ for ICCII.

$K = 1$ for CCII+ and ICCII+ and $K = -1$ for CCII− and ICCII−.

By direct analysis of the circuit of Fig. 6 the two output currents of the BOTA circuit are given by:

$$I_3 = -a_1K_1GV_1 - a_4K_4GV_2 \quad \text{and} \quad I_4 = a_2K_2GV_1 + a_3K_3GV_2\,. \tag{6}$$

From the above equation the necessary conditions to realize the BOTA realizing Fig. 2(a) are given by:

$$a_1K_1 = -1\,, \quad a_2K_2 = +1\,, \quad a_3K_3 = -1\,, \quad a_4K_4 = +1\,. \tag{7}$$

Sixteen alternative circuits that satisfy the above equations are given in Table 4. Among the reported circuits there is only one circuit that uses only CCII members namely circuit number 5 in Table 4. Among the reported circuits there is only one circuit that uses only ICCII members namely circuit number 12 in Table 4.

Although all the 16 circuits described in Table 4 are floating, the grounded current $I_G$ is not zero in all of them. Of course circuit number 15 in Table 4 has $I_G = 0$ as it employs two CCII− and two ICCII− with $I_G = 0$ in each of the four conveyors. There are however three more circuits in Table 4 that enjoy the property of having $I_G = 0$. The necessary conditions for $I_G = 0$ in the GC circuit of Fig. 6 are

Table 4. Alternative GC realizations of BOTA of Fig. 6.

| Circuit | $a_1$ | $K_1$ | $a_2$ | $K_2$ | $a_3$ | $K_3$ | $a_4$ | $K_4$ | GC1 | GC2 | GC3 | GC4 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | + | − | + | + | − | + | + | + | CCII− | CCII+ | ICCII+ | CCII+ |
| 2 | − | + | + | + | − | + | + | + | ICCII+ | CCII+ | ICCII+ | CCII+ |
| 3 | + | − | − | − | − | + | + | + | CCII− | ICCII− | ICCII+ | CCII+ |
| 4 | − | + | − | − | − | + | + | + | ICCII+ | ICCII− | ICCII+ | CCII+ |
| 5 | + | − | + | + | + | − | + | + | CCII− | CCII+ | CCII− | CCII+ |
| 6 | − | + | + | + | + | − | + | + | ICCII+ | CCII+ | CCII− | CCII+ |
| 7 | + | − | − | − | + | − | + | + | CCII− | ICCII− | CCII− | CCII+ |
| 8 | − | + | − | − | + | − | + | + | ICCII+ | ICCII− | CCII− | CCII+ |
| 9 | + | − | + | + | − | + | − | − | CCII− | CCII+ | ICCII+ | ICCII− |
| 10 | − | + | + | + | − | + | − | − | ICCII+ | CCII+ | ICCII+ | ICCII− |
| 11 | + | − | − | − | − | + | − | − | CCII− | ICCII− | ICCII+ | ICCII− |
| 12 | − | + | − | − | − | + | − | − | ICCII+ | ICCII− | ICCII+ | ICCII− |
| 13 | + | − | + | + | + | − | − | − | CCII− | CCII+ | CCII− | ICCII− |
| 14 | − | + | + | + | + | − | − | − | ICCII+ | CCII+ | CCII− | ICCII− |
| 15 | + | − | − | − | + | − | − | − | CCII− | ICCII− | CCII− | ICCII− |
| 16 | − | + | − | − | + | − | − | − | ICCII+ | ICCII− | CCII− | ICCII− |

given by:

$$a_2 = -a_1 \quad \text{and} \quad a_4 = -a_3\,. \tag{8}$$

It can be easily seen that circuit numbers 2, 3, 14 and 15 in Table 4 satisfy the above conditions.

Similarly in the four GC three port gyrator published recently in Ref. 17, it was mentioned that $I_G = 0$ in circuit number 16 in Table 2 in Ref. 17. It can also be proved that $I_G = 0$ in circuit number 13 in Table 2 in Ref. 17 as well.

In the generalized BOTA circuit of Fig. 6 the parasitic resistances of the CCII or ICCII are acting in series with the resistor $R$ connected between the $X$ ports and ground resulting in an actual resistor value $R_a$ equal to $R + R_x$. This can be compensated by subtracting the value of $R_x$ of the GC from the design value of $R$.

## 5. Pathological Realizations of BOTA Using Two Grounded $G$

Four pathological realizations of BOTA using one floating $G$ were generated in Ref. 1 using NAM expansion. In addition only two pathological realizations of BOTA using two grounded $G$ were introduced in Ref. 1. It is desirable to complete the set of the realizations of BOTA using two grounded $G$. There are two alternative methods to realize the BOTA using two grounded $G$, the first method is based on current subtraction and the second method is based on voltage subtraction.

### 5.1. *BOTA realization based on current subtraction*

Six pathological realizations of the BOTA using two grounded $G$ are summarized in Table 5. Realization number 3 in Table 5 was reported before in Ref. 1, the other five realizations are new.

### 5.2. *BOTA realization based on voltage subtraction*

Four pathological realizations of the BOTA based on using two VM to subtract the two input voltages and using two grounded $G$ are summarized in Table 6. Realization number 2 in Table 6 was reported before in Ref. 1, the other three realizations are new.

Table 5. Pathological realizations of the BOTA based on current subtraction.

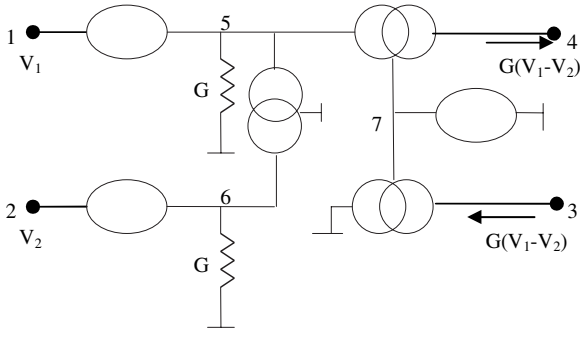
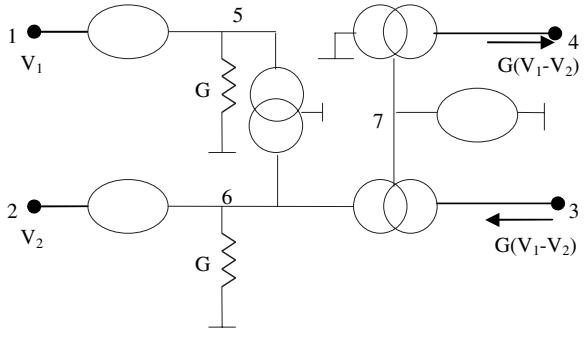
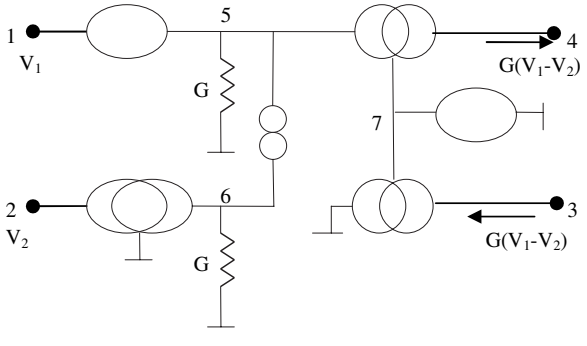
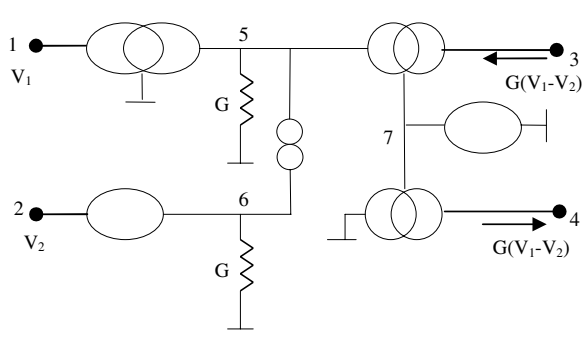
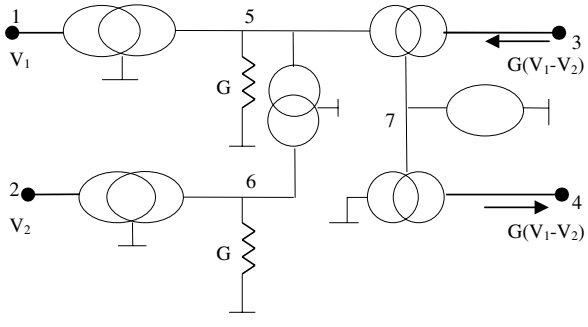
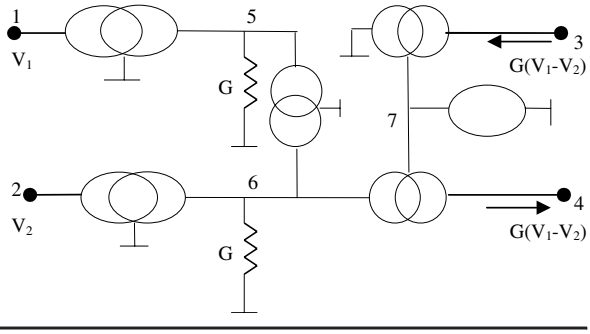
| Realization | Six realizations of the BOTA using two grounded $G$ |
|---|---|
| 1<br>3 nullator 3 CM |  |
| 2<br>3 nullator 3 CM |  |
| 3<br>2 nullator 1 VM 1 norator 2 CM[1] |  |

Table 5. (*Continued*)

| Realization | Six realizations of the BOTA using two grounded $G$ |
|---|---|
| 4<br>2 nullator 1 VM 1 norator 2 CM |  |
| 5<br>1 nullator 2 VM 3 CM |  |
| 6<br>1 nullator 2 VM 3 CM |  |

## 6. Pathological Realizations of FDDTA

Several applications of the FDDTA are available in the literature. The FDDTA is realizable as a cascade of differential voltage stage followed by a BOTA stage. Pathological realization of the differential voltage stage is obtained directly from Table 3. Figure 7(a) is based on taking the two sections of the input stage as

Table 6. Pathological realizations of the BOTA based on voltage subtraction.

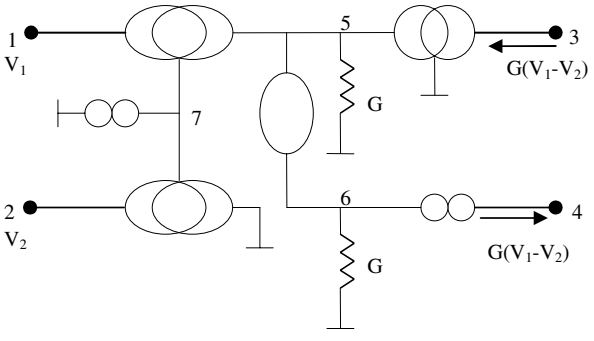
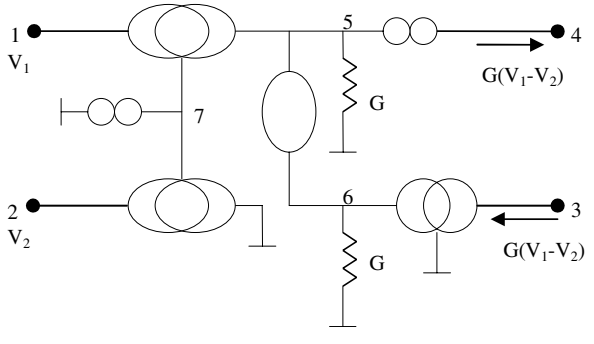
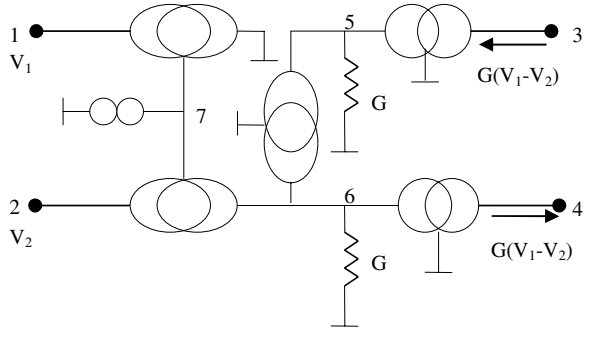
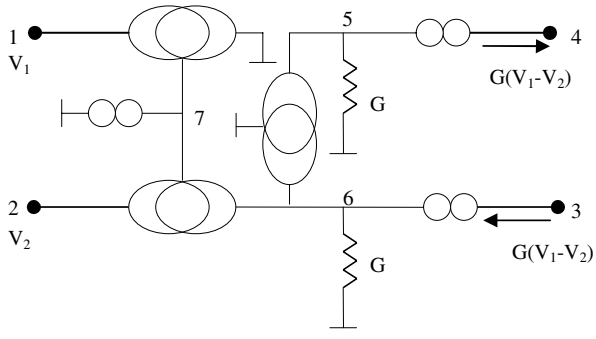
| Realization | Four realizations of the BOTA using two grounded $G$ |
|---|---|
| 1<br>1 nullator 2 VM 2 norator 1 CM |  |
| 2<br>1 nullator 2 VM 2 norator 1 CM[1] |  |
| 3<br>3 VM 1 norator 2 CM |  |

Table 6. (*Continued*)

| Realization | Four realizations of the BOTA using two grounded $G$ |
|---|---|
| 4<br>3 VM 3 norator |  |

realization 1 from Table 3. Figure 7(b) is based on taking the two sections of the input stage as realization 2 from Table 3. Similarly for Figs. 7(c) and 7(d), it is also possible to take two alternative realizations from Table 3 to realize the two input sections. As an example Fig. 7(e) uses realization 1 of Table 3 to realize $V_{12} = V_1 - V_2$ and realization 2 of Table 3 to realize $V_{34} = V_3 - V_4$.

The realization of the second stage namely the BOTA can be taken from any of the pathological realizations given in Fig. 5 resulting in a FDDTA that employs 10 grounded $G$. The BOTA realization can also be taken from any of the pathological realizations given in Table 5 or 6 resulting in a FDDTA that employs eight grounded $G$.

It is also possible to realize the differential voltage stage without any $G$ as shown in Fig. 8 which realizes first stage using only two VM and two norators.[18] It is worth noting that this realization is based on voltage subtraction a feature that is provided by VM.[18,19] The realization of the BOTA can be taken from any of the pathological realizations given in Fig. 5 resulting in a FDDTA that employs four grounded $G$. The BOTA realization can also be taken from any of the pathological realizations given in Table 5 or 6 resulting in a FDDTA that employs only two grounded $G$.

## 7. Simulation Results

Simulation results of the BOTA circuit are given in this section using the differential voltage current conveyor (DVCC).[20]

The CMOS circuit realizing the DVCC is shown in Fig. 9 and the transistor aspect ratios are given in Table 7 based on the 0.5 $\mu$m CMOS model from MOSIS. The supply voltages used are $\pm 1.5$ V and $V_{B1} = -0.52$ V and $V_{B2} = 0.33$ V.

The CCII+ and CCII− are obtained by using $Y_1$ as the $Y$ input and grounding $Y_2$, on the other-hand the ICCII+ and ICCII− are obtained by using $Y_2$ as the $Y$ input and grounding $Y_1$.

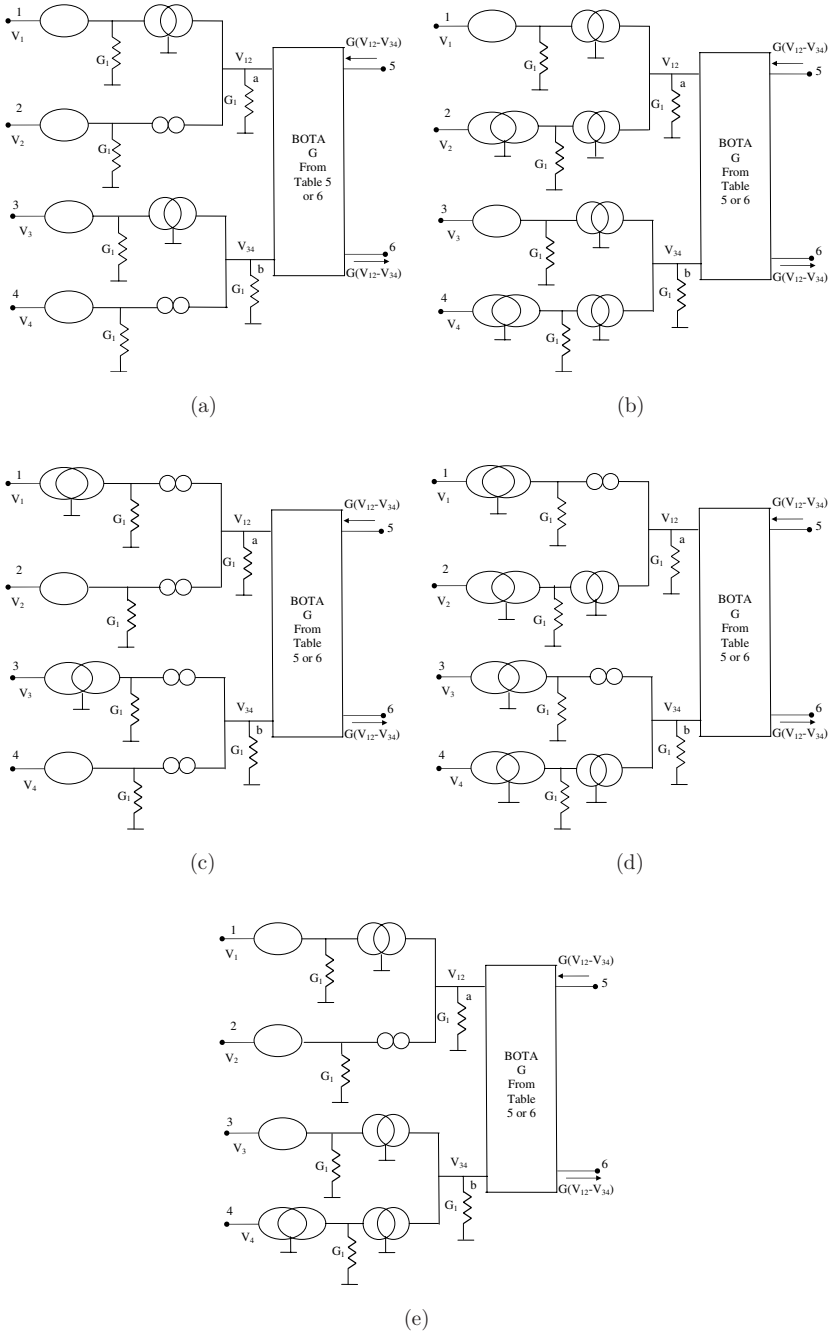



Fig. 7. (a) Realization 1 of FDDTA as a two stage based on current subtraction. (b) Realization 2 of FDDTA as a two stage based on current subtraction. (c) Realization 3 of FDDTA as a two stage based on current subtraction. (d) Realization 4 of FDDTA as a two stage based on current subtraction. (e) Realization 5 of FDDTA as a two stage based on current subtraction.

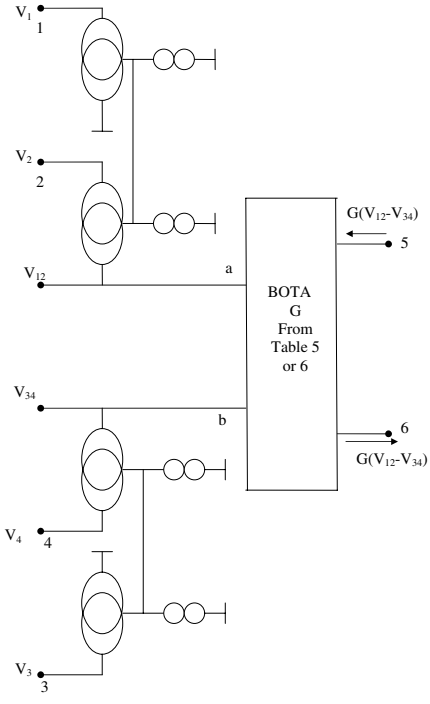



Fig. 8. Realization of FDDTA as a two stage based on voltage subtraction.

Four alternative circuits based on the generalized circuit shown in Fig. 6 are simulated taking $V_1 = 15\,\text{mV}$, $V_2 = 5\,\text{mV}$. The grounded resistors at the four X terminals are taken to be $1\,\text{k}\Omega$ each and the grounded load resistors at the terminals 3 and 4 are taken to be $10\,\text{k}\Omega$ each.

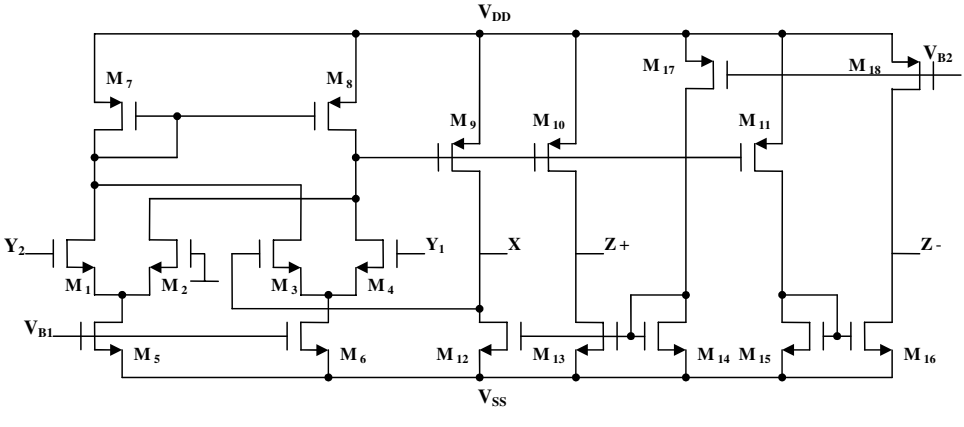



Fig. 9. CMOS circuit of the DVCC.[20]

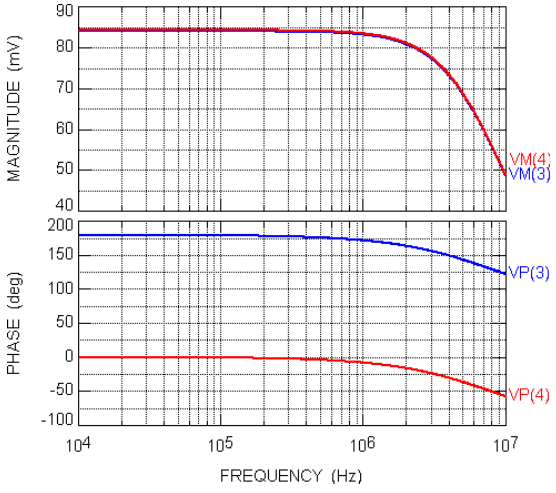
Table 7. Transistor aspect ratios of the CMOS circuit shown in Fig. 9.

| MOS transistors | $W(\mu m)/L(\mu m)$ |
|---|---|
| $M_1$, $M_2$, $M_3$, $M_4$ | 2.5/1 |
| $M_5$, $M_6$ | 8/1 |
| $M_{12}$, $M_{13}$, $M_{14}$, $M_{15}$, $M_{16}$ | 20/2.5 |
| $M_7$, $M_8$ | 10/1 |
| $M_9$, $M_{10}$, $M_{11}$, $M_{17}$, $M_{18}$ | 40/2 |

Figure 10(a) represents the magnitude and phase response of circuit number 2 in Table 4 which belongs to the generalized conveyor BOTA of Fig. 6. It is seen that the magnitude of the voltage at terminals 3 and 4 are identical and is slightly less than the theoretical expected value of 100 mV due to the parasitic resistances $R_x$ at the four X terminals of the CCII and ICCII.

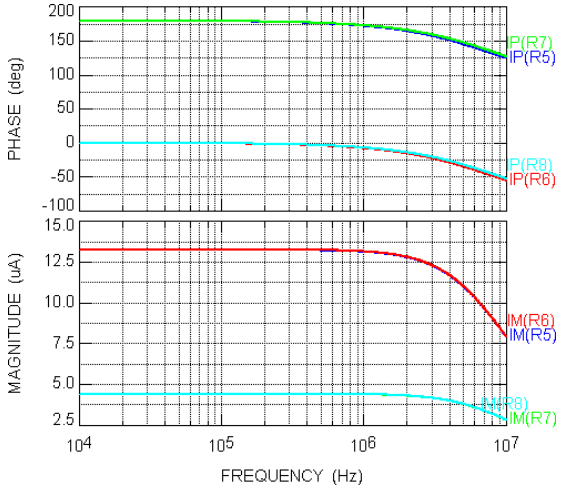
On the other hand the phase of the voltage at terminals 3 and 4 are 180° out of phase as expected. The frequency band is limited by the parasitic capacitances $C_Z$ of the CCII and ICCII. Figure 10(b) represents the currents in the grounded resistors connected to ports X of the CCII and ICCII. It is seen that the phase of the currents in $R_6$ and $R_8$ is zero where as the phase of the currents in $R_5$ and $R_7$ is 180°. From the magnitude and phase responses it is seen that $I_G$ is zero for this circuit. The total power dissipation is given by 4.07935 mW.

Similarly Fig. 11(a) represents the output voltages at nodes 3 and 4 of the circuit number 3 in Table 4. Figure 11(b) shows also that the current $I_G$ is zero for this circuit. The total power dissipation is given by 4.08005 mW.




(a)

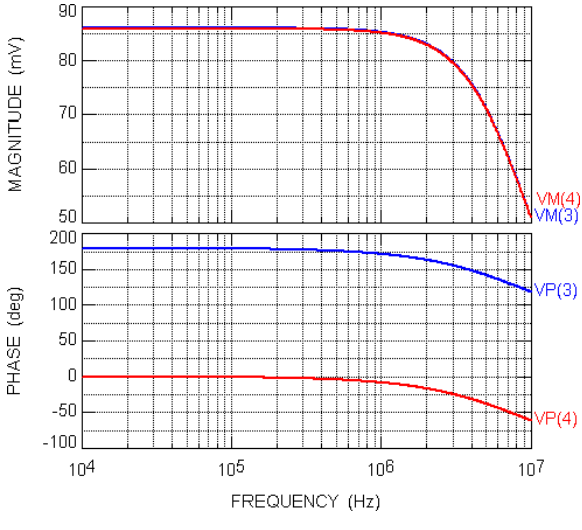
Fig. 10. (a) Simulation results of output voltage of circuit number 2 in Table 4. (b) Simulation results of currents in the circuit number 2 in Table 4.




(b)

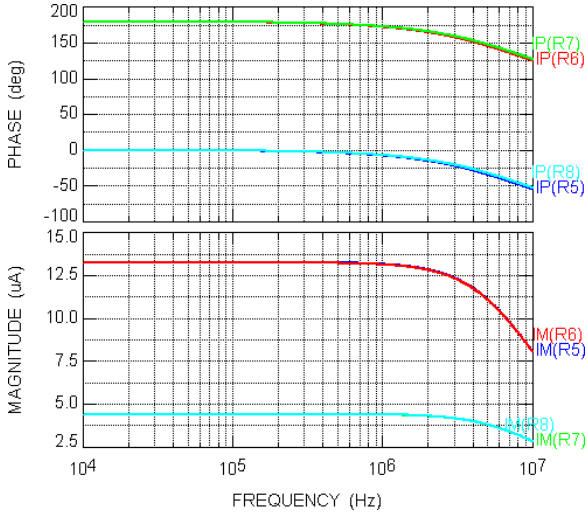
Fig. 10. (*Continued*)

Similarly Fig. 12(a) represents the output voltages at nodes 3 and 4 of the circuit number 5 in Table 4. Figure 12(b) shows also that the current $I_G$ is not zero for this circuit since all the four currents in the resistors $R_5$ to $R_8$ are in phase. The total power dissipation is given by 4.08005 mW.




(a)

Fig. 11. (a) Simulation results of output voltage of circuit number 3 in Table 4. (b) Simulation results of currents in the circuit number 3 in Table 4.

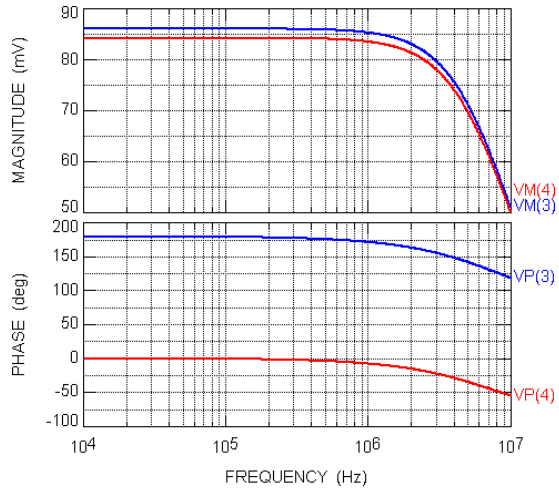



(b)

Fig. 11. (*Continued*)

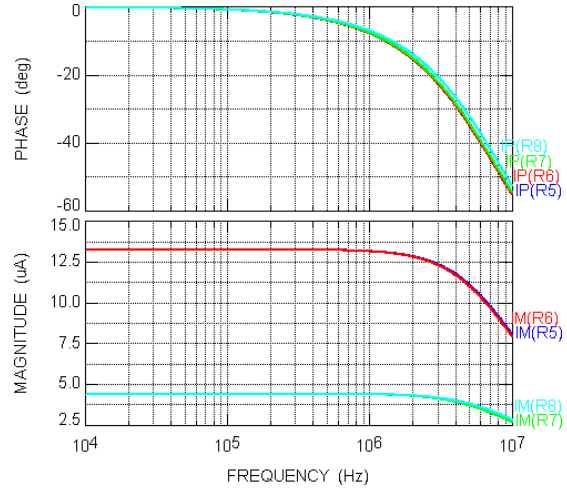
Finally Fig. 13(a) represents the output voltages at nodes 3 and 4 of the circuit number 6 in Table 4. Figure 13(b) shows also that the current $I_G$ is not zero for this circuit. The total power dissipation is given by 4.07970 mW.

As a second example a balanced output integrator is realized using the BOTA circuit number 12 in Table 4 which uses four ICCII and is excited at port 1 by 1.2 V




(a)

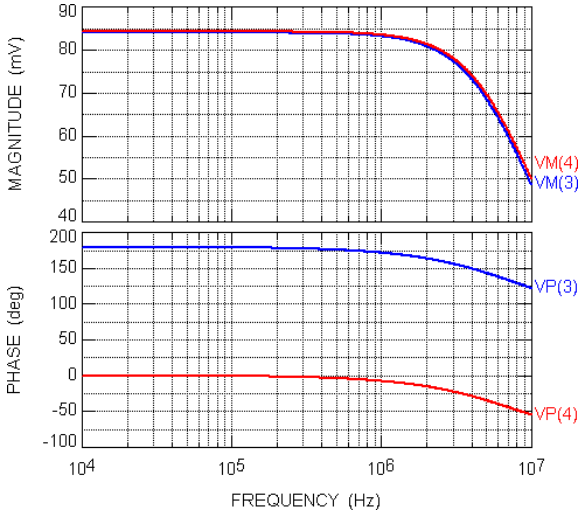
Fig. 12. (a) Simulation results of output voltage of circuit number 5 in Table 4. (b) Simulation results of currents in the circuit number 5 in Table 4.




(b)

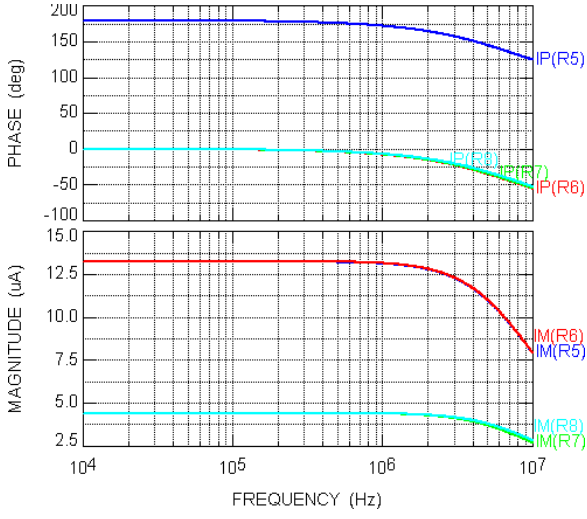
Fig. 12. (*Continued*)

and at port 2 by 0.2 V. The grounded resistors at the four X terminals are taken equal to 1 kΩ each and the grounded load capacitors at terminals 3 and 4 are taken equal to 10 nF each. Figure 14 represents the magnitude and phase responses of the balanced output voltages $V_3$ and $V_4$ of the integrator circuit. The total power dissipation is given by 4.08212 mW.




(a)

Fig. 13. (a) Simulation results of output voltage of circuit number 6 in Table 4. (b) Simulation results of currents in the circuit number 6 in Table 4.




(b)

Fig. 13. (*Continued*)

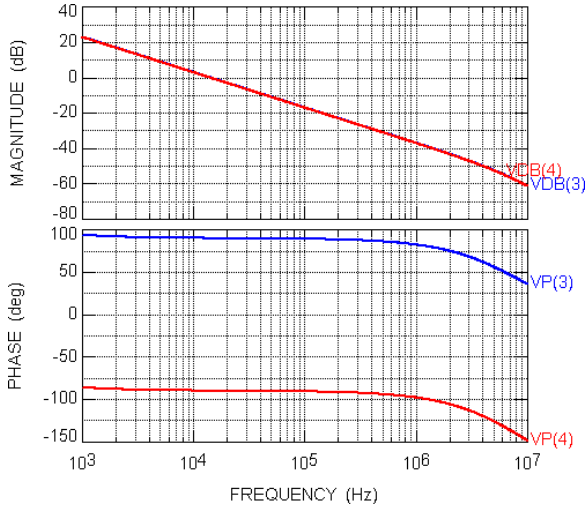



Fig. 14. Simulation results of balanced output integrator using the circuit number 12 in Table 4.

## 8. Conclusion

Additional important applications of the pathological mirror elements[19,21] in the realization of BOTA and FDDTA are given in this paper.

Sixteen pathological realizations of the BOTA using four grounded $G$ are generated. One of these circuits is realizable using four CCII, another one is realizable

using four ICCII and the remaining 14 circuits are realizable using a combination of CCII and ICCII. Six new pathological realizations of the BOTA using two grounded $G$ based on current subtraction are introduced. Four new pathological realizations of the BOTA using two grounded $G$ based on voltage subtraction are introduced. New pathological realizations of the FDDTA are also given.

Several applications of the TA in realizing integrators, filters and oscillators are available in the literature[22–28] and the pathological realizations given provide additional new ideally equivalent circuits.

The importance of pathological realization in active circuit modeling has been recently demonstrated in Ref. 29.

## Acknowledgment

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