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Three port gyrator circuits using transconductance amplifiers or generalized conveyors

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ABSTRACT

The three port gyrator was introduced and defined in [1] in two alternative forms of the admittance matrix (Y). Four alternative realizations of the three port gyrator using three transconductance amplifiers (TA) are given, three of them are new. Sixteen alternative three port gyrator circuits using four current conveyors (CCII) or four inverting current conveyors (ICCII) or a combination of both of them and four grounded resistors are given. Eight alternative three port gyrator circuits using two CCII or two ICCII or a combination of both of them, balanced output current conveyors (BOCCII) and three grounded resistors are also introduced. Eight alternative three port gyrator circuits using two CCII or two ICCII or a combination of both of them, differential voltage current conveyors (DVCC) and three grounded resistors are also introduced. Finally four equivalent three port gyrator circuits using a combination of DVCC and BOCCII and two grounded resistors are also introduced, three of them are new.

1. Introduction

The most commonly used active circuit for the realization of a grounded inductor is the gyrator. The gyrator is a positive impedance inverter. The ideal gyrator is a passive, lossless and nonreciprocal circuit element. Several realizations of the gyrator using operational amplifiers (Op Amp) are available in the literature [1–4]. The realization of the gyrator using two CCII was introduced in [5]. A single CCII realization of the ideal gyrator was given in [6]. The gyrator is also known as the type 1 LC mutator [7] and two alternative realizations of the type 1 LC mutator were introduced in [8].

The three port gyrator was first defined in [1] as a three port circuit which realizes a floating inductor between two of its ports when the third port is terminated by a capacitor. Additional study of the three port gyrator and its realizations using TA and CCII was given in [9,10].

2. Three port gyrators

Before considering the three port gyrators, a brief review of the two port gyrators is given next.

2.1. Two port gyrators

The two port gyrator shown symbolically in Fig. 1(a) is a positive impedance inverter which realizes an ideal grounded inductor at one port when the other port is terminated by a capacitor. The Y matrix of the ideal two port gyrator is defined by one of the following two types:

$$Y = \begin{bmatrix} 0 & \pm G \\ \mp G & 0 \end{bmatrix} \tag{1}$$

The ideal two port gyrator is a nonreciprocal, passive and lossless circuit element. There are two alternative realizations of the two port gyrator using two single input single-output TA. The generation of the two port gyrators using two CCII or ICCII or combination of both starting from the above Y matrix was given in [11].

2.2. Three port gyrators

The three port gyrator shown symbolically in Fig. 1(b) was introduced in [1] and it realizes an ideal floating inductor between two of its port when the third port is terminated by a capacitor. Four types of the Y matrix defining the three port gyrator are given next.

2.2.1. Type-A three port gyrator

$$Y = \begin{bmatrix} 0 & 0 & G_2 \\ 0 & 0 & -G_2 \\ -G_1 & G_1 & 0 \end{bmatrix} \tag{2}$$

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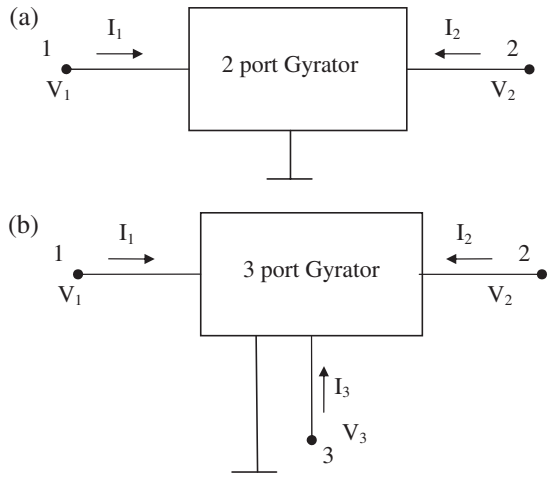


Fig. 1. (a) Symbol of two port gyrator and (b) symbol of three port gyrator.

2.2.2. Type-B three port gyrator

$$Y = \begin{bmatrix} 0 & 0 & -G_2 \\ 0 & 0 & G_2 \\ G_1 & -G_1 & 0 \end{bmatrix} \tag{3}$$

The *Y* parameter signs are opposite to the signs of the *Y* parameters of the type A. Both types A and B have been defined in [1].

2.2.3. Type-C three port gyrator

$$Y = \begin{bmatrix} 0 & 0 & -G_1 \\ 0 & 0 & G_1 \\ G_2 & -G_2 & 0 \end{bmatrix} \tag{4}$$

It is the transpose [12–14] of the *Y* matrix of type A and the circuit realizations are the adjoints of the circuits of type A and are obtained from the circuits of type A by interchanging ports 1 and 2 and G_1 and G_2.

2.2.4. Type-D three port gyrator

$$Y = \begin{bmatrix} 0 & 0 & G_1 \\ 0 & 0 & -G_1 \\ -G_2 & G_2 & 0 \end{bmatrix} \tag{5}$$

It is the transpose of the *Y* matrix of type B and the circuit realizations are the adjoints of the circuits of type B and are obtained from the circuits of type B by interchanging ports 1 and 2 and G_1 and G_2.

For the type A gyrator the total power absorbed by the three port gyrator is given by:

$$\sum ViIi = (G_2 - G_1)V_1V_3 - (G_2 - G_1)V_2V_3 \tag{6}$$

It is seen that the gyrator will be passive and lossless if G_2 equal to G_1 and this will be defined as an ideal gyrator. In the case of ideal gyrator the type C gyrator will be identical to type B gyrator and the type D gyrator will be identical to type A gyrator.

3. Transconductance realizations

In this section the TA realization of each of the four types of three port gyrators are given. A brief summary of six different types of TA and their adjoints is included in Table 1, two of them were also given in [13]. The TA realizations of the four types of the three port gyrators can be derived from Table 1 and are given in Fig. 2. The realization shown in Fig. 2(d) was reported before in [9,15].

4. Current conveyor realizations

Two alternative circuit configurations for the type A three port gyrator are given next. The first configuration is a seven node circuit and is derived using nodal admittance matrix (NAM) expansion [16–19]. Two alternative circuits that belong to this seven node configuration are derived using NAM expansion. The second configuration is a six node circuit and is obtained from the first realization by combining a CCII+ and a CCII− having a common *Y* terminal to realize a BOCCII.

4.1. Circuit configuration I

Starting from Eq. (2) and adding a fourth blank row and column, connecting a nullator between nodes 1, 4 and a current mirror (CM) between nodes 3, 4 in order to move $-G_1$ from 3, 1 position to become G_1 at the diagonal position 4, 4 thus:

$$Y = \begin{bmatrix} 0 & 0 & G_2 & 0 \\ 0 & 0 & -G_2 & 0 \\ 0 & G_1 & 0 & 0 \\ 0 & 0 & 0 & G_1 \end{bmatrix} \tag{7}$$

Adding a fifth blank row and column to Eq. (7), connecting a nullator between nodes 2, 5 and a norator between nodes 3, 5 in order to move G_1 from 3, 2 position to the diagonal position 5, 5 thus:

$$Y = \begin{bmatrix} 0 & 0 & G_2 & 0 & 0 \\ 0 & 0 & -G_2 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & G_1 & 0 \\ 0 & 0 & 0 & 0 & G_1 \end{bmatrix} \tag{8}$$

Adding a sixth blank row and column to Eq. (8), connecting a nullator between nodes 3, 6 and a norator between nodes 1, 6 in order to move G_2 from 1, 3 position to the diagonal position 6, 6 thus:

$$Y = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & -G_2 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & G_1 & 0 & 0 \\ 0 & 0 & 0 & 0 & G_1 & 0 \\ 0 & 0 & 0 & 0 & 0 & G_2 \end{bmatrix} \tag{9}$$

Adding a seventh blank row and column to Eq. (9), connecting a nullator between nodes 3, 7 and a CM between nodes 2, 7 in order to move $-G_2$ from 2, 3 position to become G_2 at the diagonal position 7, 7 thus:

Table 1
Different types of TA and their adjoints.

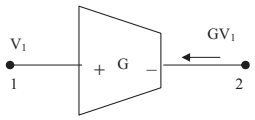
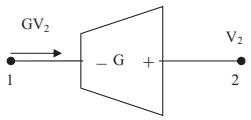
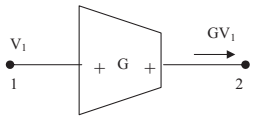
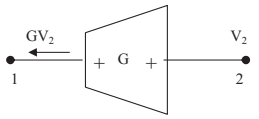
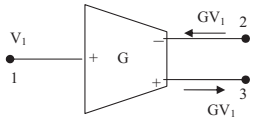
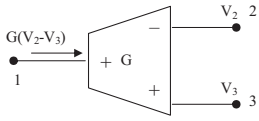
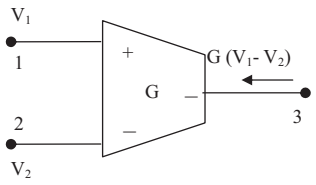
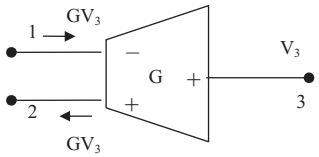
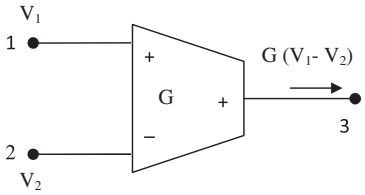
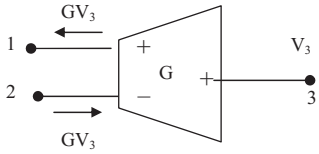
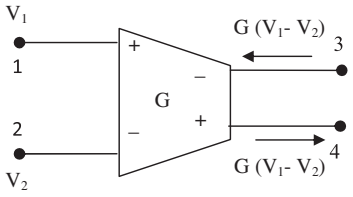
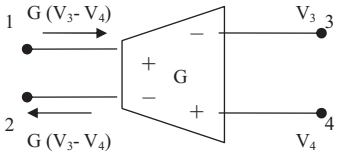
TA	TA and *Y* matrix	Adjoint TA and *Y* matrix
1 Single input single output −	 $Y=\begin{bmatrix}0 & 0\\ G & 0\end{bmatrix}$	 $Y=\begin{bmatrix}0 & G\\ 0 & 0\end{bmatrix}$
2 Single input single output +	 $Y=\begin{bmatrix}0 & 0\\ -G & 0\end{bmatrix}$	 $Y=\begin{bmatrix}0 & -G\\ 0 & 0\end{bmatrix}$
3 Single input balanced output	 $Y=\begin{bmatrix}0 & 0 & 0\\ G & 0 & 0\\ -G & 0 & 0\end{bmatrix}$	 $Y=\begin{bmatrix}0 & G & -G\\ 0 & 0 & 0\\ 0 & 0 & 0\end{bmatrix}$
4 Differential input single output −	 $Y=\begin{bmatrix}0 & 0 & 0\\ 0 & 0 & 0\\ G & -G & 0\end{bmatrix}$	 $Y=\begin{bmatrix}0 & 0 & G\\ 0 & 0 & -G\\ 0 & 0 & 0\end{bmatrix}$
5 Differential input single output +	 $Y=\begin{bmatrix}0 & 0 & 0\\ 0 & 0 & 0\\ -G & G & 0\end{bmatrix}$	 $Y=\begin{bmatrix}0 & 0 & -G\\ 0 & 0 & G\\ 0 & 0 & 0\end{bmatrix}$

Table 1 (*Continued*)

TA	TA and *Y* matrix	Adjoint TA and *Y* matrix
6 Differential input balanced output	 $Y=\begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ G & -G & 0 & 0 \\ -G & G & 0 & 0 \end{bmatrix}$	 $Y=\begin{bmatrix} 0 & 0 & G & -G \\ 0 & 0 & -G & G \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix}$

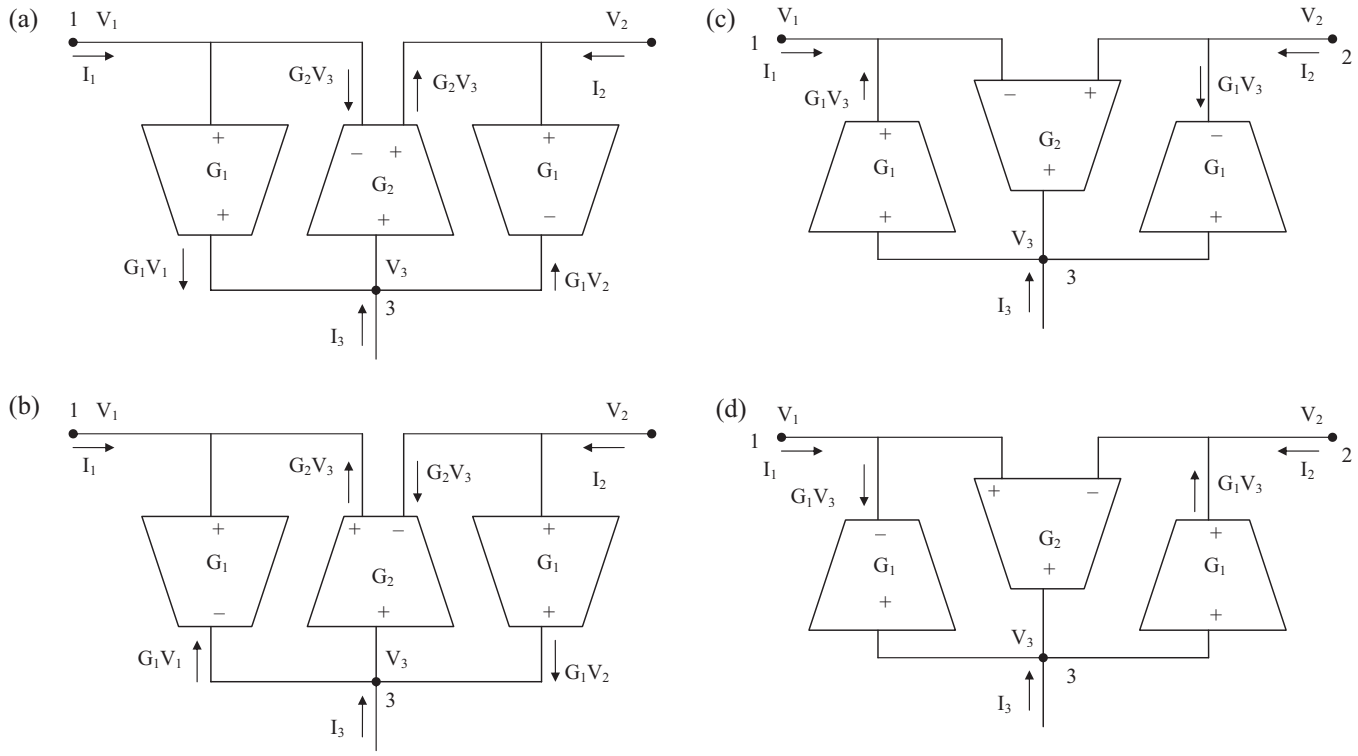


Fig. 2. (a) Three TA realization of type A three port gyrator, (b) three TA realization of type B three port gyrator, (c) three TA realization of type C three port gyrator and (d) three TA realization of type D three port gyrator [9,15].

$$Y=\begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & G_1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & G_1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & G_2 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & G_2 \end{bmatrix} \quad (10)$$

The pathological realization of the seven nodes NAM equation is shown in Fig. 3(a) which includes four nullators, two norators and two CM. The CCII realization of Fig. 3(a) using two CCII+ and two CCII− is shown in Fig. 3(b). A slightly different circuit and using same number of circuit components was given in the literature in [9,20]. An alternative ideally equivalent realization can be obtained from Eq. (2) by adding a fourth blank row and column, connecting a voltage mirror (VM) between nodes 1, 4 and a norator between nodes 3, 4 in order to move $-G_1$ from 3, 1 position to become G_1 at the diagonal position 4, 4 then using similar steps as in the previous realization, the following NAM matrix is obtained:

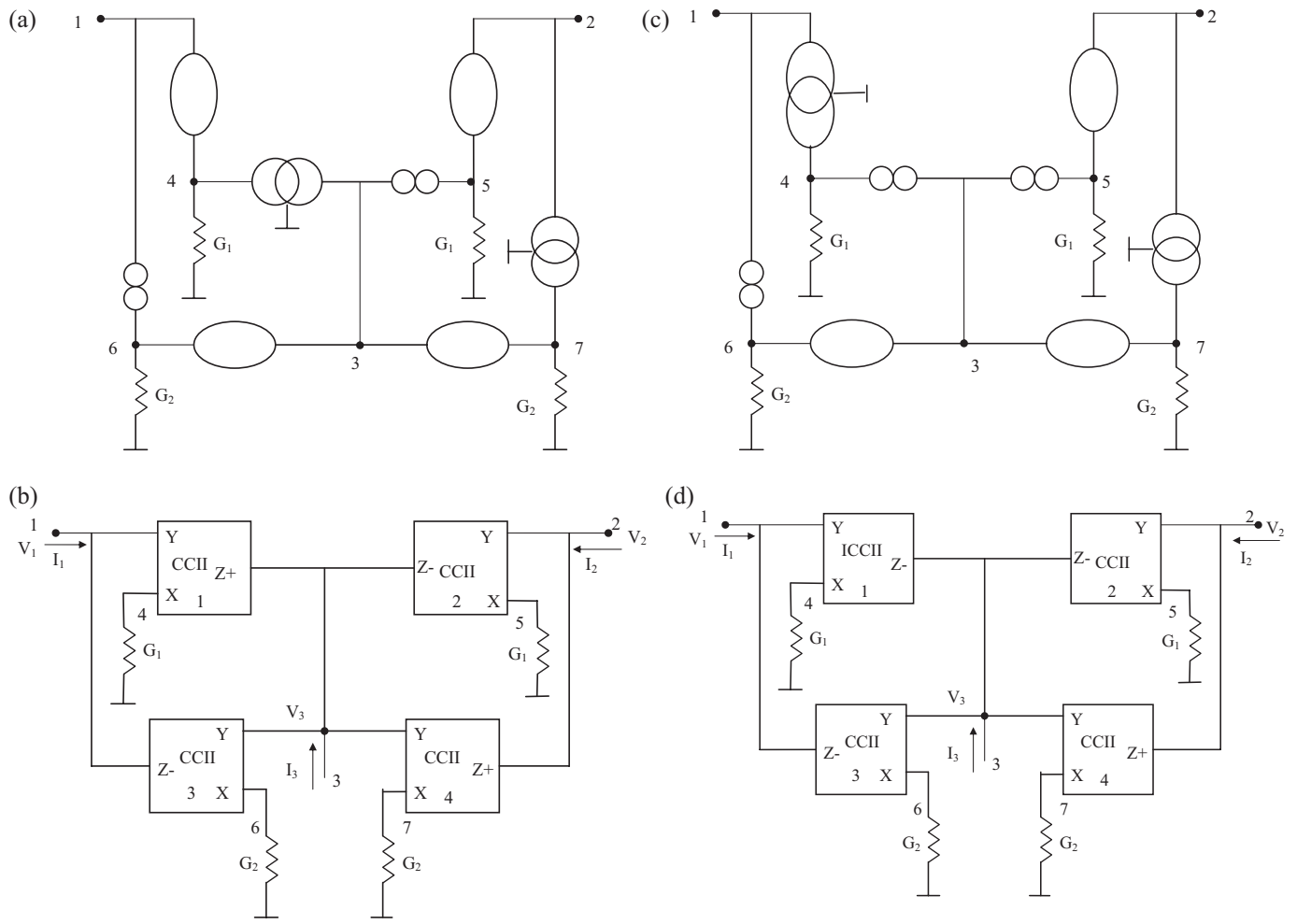


Fig. 3. (a) Pathological realization of the *Y*-matrix of Eq. (10), (b) four CCII grounded resistors realization of (a), (c) pathological realization of the *Y*-matrix of Eq. (11) and (d) four CCII grounded resistors realization of (c).

$$Y = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & G_1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & G_1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & G_2 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & G_2 \end{bmatrix} \quad (11)$$

The pathological realization of Eq. (11) is shown in Fig. 3(c) which includes three nullators, one VM, three norators and one CM. The CCII realization of Fig. 3(c) using CCII+, two CCII− and one ICCII− is shown in Fig. 3(d).

4.2. Circuit configuration II

The circuit of Fig. 3(b) can be modified by combining the CCII− number 3 and the CCII+ number 4 having a common *Y* terminal to form a BOCCII as shown in Fig. 4 [21]. The circuit shown in Fig. 4 is a six node circuit and equivalent realization is available in the literature in [10].

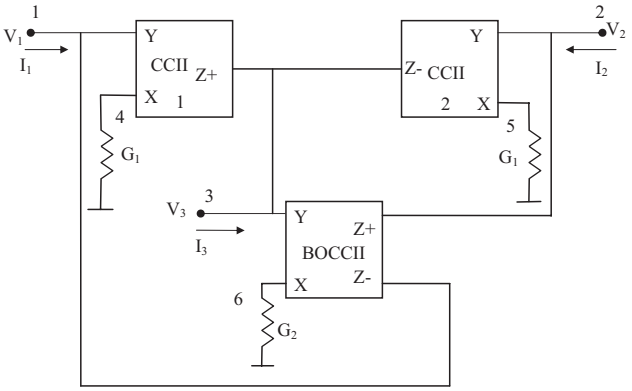


Fig. 4. Three CCII grounded resistors realization of type A gyrator.

5. Generalized conveyor realizations

The circuits reported in the previous section represent special cases of families of circuits. Although the members of the families of circuits can be generated using NAM expansion, it is easier to generate them from the general known topology as will be demonstrated next.

Table 2
Alternative GC realizations for type A gyrator of Fig. 5(a).

Circuit	a_1	K_1	a_2	K_2	a_3	K_3	a_4	K_4	GC1	GC2	GC3	GC4
1	+	+	–	+	–	+	+	+	CCII+	ICCII+	ICCII+	CCII+
2	+	+	–	+	–	+	–	–	CCII+	ICCII+	ICCII+	ICCII–
3	+	+	–	+	+	–	+	+	CCII+	ICCII+	CCII–	CCII+
4	+	+	–	+	+	–	–	–	CCII+	ICCII+	CCII–	ICCII–
5	+	+	+	–	–	+	+	+	CCII+	CCII–	ICCII+	CCII+
6	+	+	+	–	–	+	–	–	CCII+	CCII–	ICCII+	ICCII–
7	+	+	+	–	+	–	+	+	CCII+	CCII–	CCII–	CCII+
8	+	+	+	–	+	–	–	–	CCII+	CCII–	CCII–	ICCII–
9	–	–	–	+	–	+	+	+	ICCII–	ICCII+	ICCII+	CCII+
10	–	–	–	+	–	+	–	–	ICCII–	ICCII+	ICCII+	ICCII–
11	–	–	–	+	+	–	+	+	ICCII–	ICCII+	CCII–	CCII+
12	–	–	–	+	+	–	–	–	ICCII–	ICCII+	CCII–	ICCII–
13	–	–	+	–	–	+	+	+	ICCII–	CCII–	ICCII+	CCII+
14	–	–	+	–	–	+	–	–	ICCII–	CCII–	ICCII+	ICCII–
15	–	–	+	–	+	–	+	+	ICCII–	CCII–	CCII–	CCII+
16	–	–	+	–	+	–	–	–	ICCII–	CCII–	CCII–	ICCII–

Table 3
Alternative GC realizations for type A gyrator Fig. 5(b).

Circuit	a_1	K_1	a_2	K_2	a_3	K_3	GC 1	GC 2	BOGC 3
1	+	+	–	+	–	+	CCII+	ICCII+	ICCII+ –
2	+	+	–	+	+	–	CCII+	ICCII+	CCII– +
3	+	+	+	–	–	+	CCII+	CCII–	ICCII+ –
4	+	+	+	–	+	–	CCII+	CCII–	CCII– +
5	–	–	–	+	–	+	ICCII–	ICCII+	ICCII+ –
6	–	–	–	+	+	–	ICCII–	ICCII+	CCII– +
7	–	–	+	–	–	+	ICCII–	CCII–	ICCII+ –
8	–	–	+	–	+	–	ICCII–	CCII–	CCII– +

5.1. Four grounded resistor circuits

The circuit reported in Fig. 3(b) is generalized as shown in Fig. 5(a).

The GC is defined by:

$$I_Y = 0, \quad V_X = aV_Y \quad \text{and} \quad I_Z = KI_X \tag{12}$$

where $a = 1$ for CCII and $a = -1$ for ICCII.

$K = 1$ for CCII+ and ICCII+ and $K = -1$ for CCII– and ICCII–.

By direct analysis to the circuit of Fig. 5(a), the necessary conditions for realizing type A three port gyrator are given by

$$a_1K_1 = +1, \quad a_2K_2 = -1, \quad a_3K_3 = -1, \quad a_4K_4 = +1 \tag{13}$$

Sixteen alternative circuits satisfy the above equation as given in Table 2. Among the reported circuits there is only one circuit that uses only CCII members namely circuit number 7 in Table 2. Among the reported circuits there is only one circuit that uses only ICCII members namely circuit number 10 in Table 2. Among the reported circuits there is only one circuit that has $I_G = 0$ which is circuit number16 in Table 2.

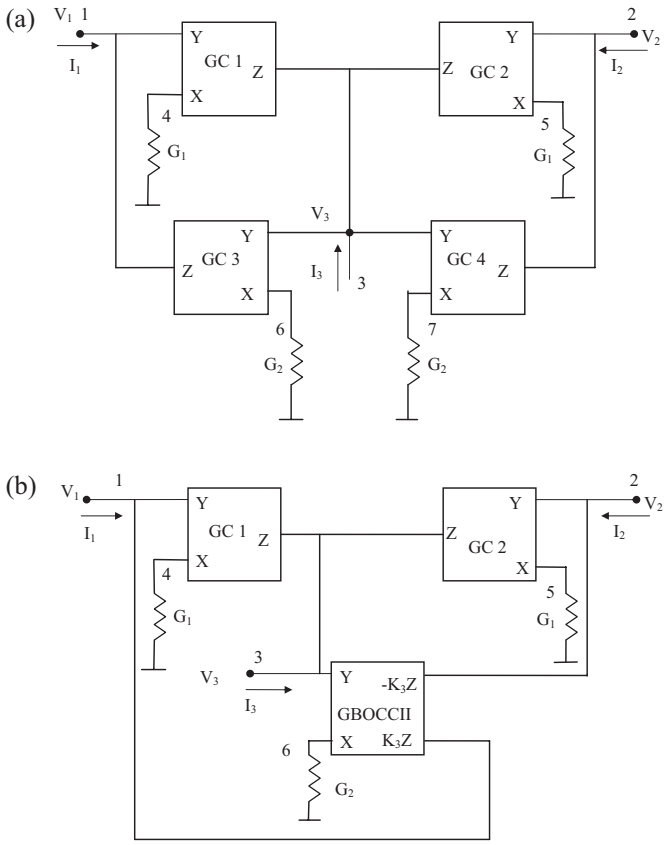


Fig. 5. (a) Generalized four CCII grounded resistors gyrator and (b) generalized three CCII grounded resistors type A gyrator.

Similarly the necessary conditions for realizing type B three port gyrator are given by

$$a_1K_1 = -1, \quad a_2K_2 = +1, \quad a_3K_3 = +1, \quad a_4K_4 = -1 \tag{14}$$

Sixteen alternative circuits satisfy the above equation can be generated and they are the same as the type A circuits with ports 1 and 2 interchanged. The sixteen type C circuits are generated from the type B circuits by interchanging G_1 and G_2. Finally the sixteen type D circuits are generated from the type A circuits by interchanging G_1 and G_2.

Table 4
Properties of the four types of the three port gyrator.

Gyrator type	Y matrix	Properties
A	$Y = \begin{bmatrix} 0 & 0 & G_2 \\ 0 & 0 & -G_2 \\ -G_1 & G_1 & 0 \end{bmatrix}$	TA realization shown in Fig 2(a). 16 GC realizations, Table 2,8 GC realizations, Table 3,4 realizations, Fig. 6
B	$Y = \begin{bmatrix} 0 & 0 & -G_2 \\ 0 & 0 & G_2 \\ G_1 & -G_1 & 0 \end{bmatrix}$	TA realization shown in Fig. 2(b) Y matrix is the negative of type A Y matrix
C	$Y = \begin{bmatrix} 0 & 0 & -G_1 \\ 0 & 0 & G_1 \\ G_2 & -G_2 & 0 \end{bmatrix}$	TA realization shown in Fig. 2(c) Ideal gyrator type C is identical to type B
D	$Y = \begin{bmatrix} 0 & 0 & G_1 \\ 0 & 0 & -G_1 \\ -G_2 & G_2 & 0 \end{bmatrix}$	TA realization shown in Fig. 2(d) Ideal gyrator type D is identical to type A

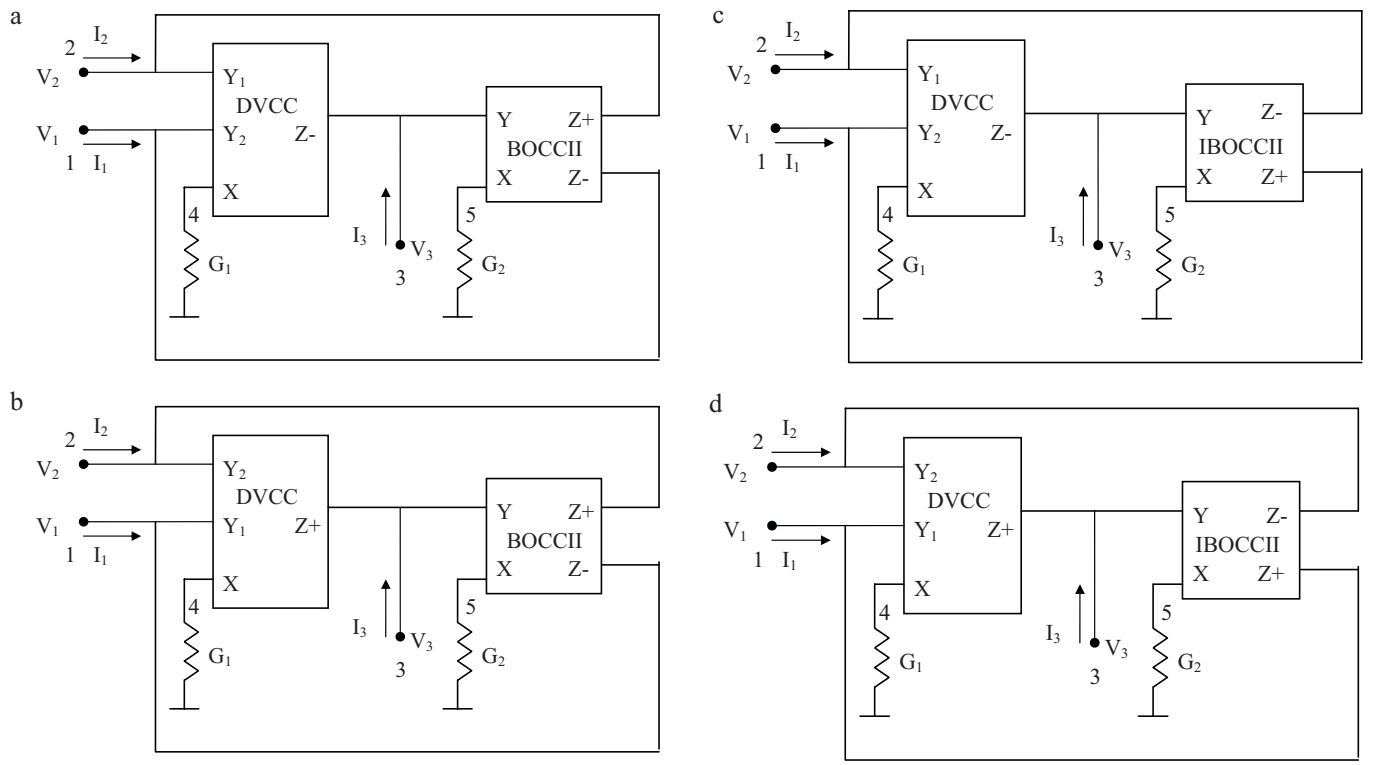


Fig. 6. (a) Two grounded resistors realization 1 of type A gyrator, (b) two grounded resistors realization 2 of type A gyrator [19], (c) two grounded resistors realization 3 of type A gyrator and (d) two grounded resistors realization 4 of type A gyrator.

5.2. Three grounded resistor circuits

The circuit reported in Fig. 4 is generalized as shown in Fig. 5(b). By direct analysis to the circuit of Fig. 5(b), the necessary conditions for realizing type A three port gyrator are given by

$$a_1K_1 = +1, \quad a_2K_2 = -1, \quad a_3K_3 = -1 \tag{15}$$

Eight alternative circuits satisfy the above equation as given in Table 3. Among the reported circuits there is only one circuit that uses only CCII members namely circuit number 4 in Table 3. Among the reported circuits there is only one circuit that uses only ICCII members namely circuit number 5 in Table 3.

Similarly the necessary conditions for realizing type B three port gyrator are given by

$$a_1K_1 = -1, \quad a_2K_2 = +1, \quad a_3K_3 = +1 \tag{16}$$

Eight alternative circuits satisfy the above equation can be generated and they are the same as the type A circuits with ports 1 and 2 interchanged. The eight type C circuits are generated from the type B circuits by interchanging G_1 and G_2. Finally the eight type D circuits are generated from the type A circuits by interchanging G_1 and G_2.

5.3. Two grounded resistor circuits

The six node circuit of Fig. 4 can be modified to a five node circuit by combining the CCII+ number 1 and the CCII− number 2 having a common Z terminal to form a DVCC− as shown in Fig. 6(a). The DVCC− is defined by the following matrix [22]:

$$\begin{bmatrix} Vx \\ I_{Y1} \\ I_{Y2} \\ I_{Z-} \end{bmatrix} = \begin{bmatrix} 0 & 1 & -1 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ -1 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} Ix \\ V_{Y1} \\ V_{Y2} \\ V_{Z-} \end{bmatrix} \tag{17}$$

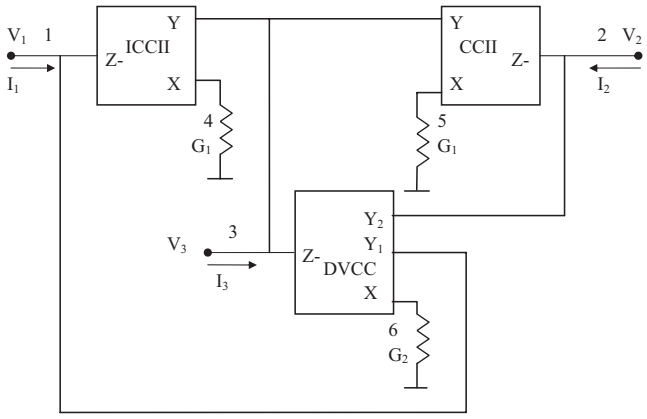


Fig. 7. Three grounded resistors realization of type C gyrator.

The circuit topology with DVCC+, BOCCII and two grounded resistors and shown in Fig. 6(b) was introduced before in [19]. Two more equivalent circuits can be generated either by NAM expansion or from a generalized circuit to Fig. 6(a) and are shown in Fig. 6(c) and (d).

Four alternative circuits realizing type B gyrator can be generated from the type A circuits by interchanging ports 1 and 2. The four type C circuits are generated from the type B circuits by interchanging G_1 and G_2. Finally the four type D circuits are generated from the type A circuits by interchanging G_1 and G_2.

6. Conclusions

Four types of the three port gyrator introduced in [1] also known as the three port LC mutator are considered. Four realizations are given using TA as shown in Fig. 2; three of them are new. Sixteen new realizations using four GC are reported for the type A

three port gyrator. Eight new realizations using two GC and one BOCCII are also given. Four realizations using two grounded resistors, one DVCC and a BOCCII are introduced three of them are new. Table 4 summarizes the definitions of the four gyrator types and how they are related to each other. Additional circuits can be generated and are not included to limit paper length. For example Fig. 7 represents one realization of the type C representing the adjoint of the circuit of Fig. 4. Seven more circuits having the same topology as that of Fig. 7 can also be generated to complete this family of the two CCII or two ICCII or a combination of both of them and a DVCC.

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