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Low Voltage Low Power Fully Differential CMOS Current Mode Digitally Controlled Variable Gain Amplifier

Ein durchgängig differentiell aufgebauter CMOS-Verstärker mit kleiner Leistung und Spannung vom Stromtyp mit digital einstellbarer Verstärkung

Abstract
In this paper, a fully differential current mode variable gain amplifier (VGA) is presented. The gain of the proposed VGA can be digitally controlled from 0 dB to 50.7 dB, with a 2.8 dB step. The proposed VGA consists of two coarse control stages with a gain step of 16.9 dB and a fine control stage with a gain step of 3.38 dB. A novel current division technique is used to control the gain of the VGA. SpectreS simulations based on the AMI 0.5 µm n-well BSIM3 parameters are in agreement with the presented work. Simulations showed that the bandwidth is about 50MHz at the maximum gain (50.7 dB). Owing to the class AB operation of the proposed VGA circuit, the power dissipation is about 1.5 mW and the equivalent input referred noise is 2.76 pA/√Hz.

Übersicht
In dieser Arbeit wird ein durchgängig differentiell aufgebauter Verstärker vom Stromtyp mit variabler Verstärkung (VGA) vorgestellt. Die Verstärkung des vorgeschlagenen VGA's kann digital zwischen 0 dB und 50,7 dB in Schritten von 2,8 dB eingestellt werden. Der Verstärker besteht aus zwei grob einstellbaren 16,9 dB Stufen und einer fein einstellbaren 3,38-dB-Stufe. Zur Steuerung der Verstärkung des VGA wird eine neue Stromaufteilungstechnik verwendet. SpectreS-Simulationen auf Basis der AMI 0,5 µm n-well BSIM3 Parameter stimmen mit den Ergebnissen in dieser Arbeit überein. Die Simulationen zeigten, daß die Bandbreite bei maximaler Verstärlung (50,7 dB) 50 MHz beträgt. Infolge des AB-Betriebs der vorgeschlagenen VGA-Schaltung beträgt die Verlustleistung 1,5 mW. Die äquivalente spektrale Rauschstromdichte am Eingang beträgt 2.76 pA/√Hz.

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Für die Dokumentation
Differentieller CMOS Verstärker / Stromtyp / variable Verstärkung

1. Introduction

Virtually all communications systems have an unpredictable received power. To isolate the receiver signal processing circuits from changes in the input signal amplitude, a variable gain amplifier (VGA) [1-7] is employed in an automatic gain control (AGC) loop. In other systems, such as disk drives, the VGA forms an important part of the read channel and helps to stabilize the voltage supplied to the detector and filter sections of the read channel [8-9]. In general, the purpose of the AGC is to maximize the dynamic range of the overall system. Further, in portable communication systems, the portability of the terminal puts stringent requirements on the supply voltage used and the power dissipation. Another requirement of the VGA is to have a constant bandwidth which is independent of the gain. These requirements suggest the use of current mode techniques. Examples of such techniques are those based on current followers [10] or current conveyors. Although these techniques have limited linearity due to mismatches in the current mirrors, this is quite tolerable in some applications. However, in other systems, higher linearity might be required. In such systems, the required accuracy can be achieved using negative feedback to correct the error.

Every AGC contains two critical blocks, a variable gain amplifier (VGA) and the power detector circuit which feeds back the control signal(s) used to adjust the gain of the VGA. In modern wireless systems, all of the baseband signal processing is implemented digitally by a DSP processor. Hence, a primary requirement of the VGA is to be digitally controlled. Another requirement is that the gain should increase linearly on the decibel scale in order to achieve wide gain control. In this paper, a current mode VGA that satisfies all the above mentioned requirements is presented.

2. The Digitally Controlled Current Follower

The circuit realization of the proposed digitally controlled current follower (DCCF) is shown in **Fig. 1**. The input current I_X is sensed by the low impedance input terminal X and multiplied by the large output resistance at node A. Cascade transistors are used to increase the output resistance. The voltage V_A is then applied to a digitally controlled transconductor whose output current is fed back to the input terminal X. Transistors M9 and M10 form a level shifter to control the standby current in the N and P parts of the digitally controlled transconductors. This feedback loop guarantees the virtual ground voltage at the X terminal. The current gain of the DCCF is then given by

$$\frac{I_Z}{I_X} = \frac{I_{N2} - I_{P2}}{I_{N3} - I_{P3}}. \tag{1}$$

It will be shown in the next section that

$$\frac{I_{N2}}{I_{N3}} = \frac{I_{P2}}{I_{P3}} = \frac{1 + \dfrac{D}{2^n}}{1 - \dfrac{D}{2^n}}. \tag{2}$$

From (1) and (2)

$$\frac{I_Z}{I_X} = \frac{1 + \dfrac{D}{2^n}}{1 - \dfrac{D}{2^n}} \approx e^{b\frac{D}{2^{n-1}}} \tag{3}$$

where D is the digital control input control word, n is the number of control bits, and b is a variable that depends on the range of $D/2^n$. For example, when $D/2^n$ is varied from 0 to 0.75, the optimum value of b (for better approximation of the exponential function) is 1.21. The deviation of the pseudo exponential char-

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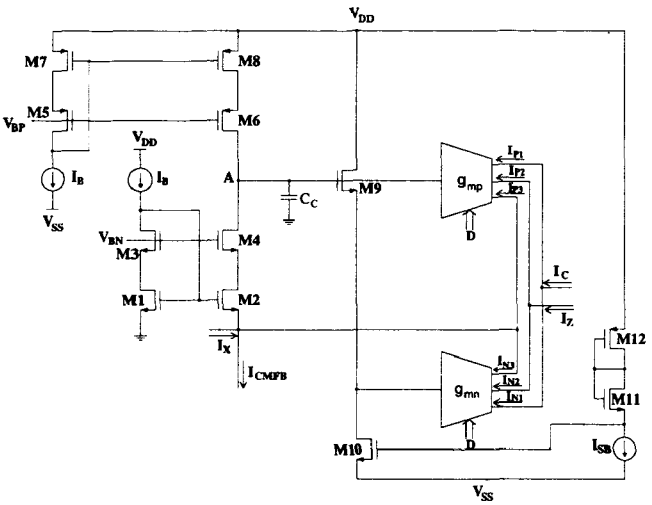

Fig. 1: The DCCF

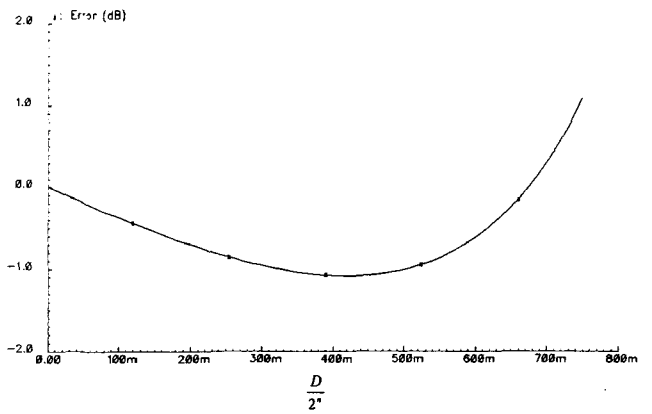

Fig. 2: The gain error

acteristic in (3) from the ideal exponential is illustrated in **Fig. 2**, from which it can be shown that the gain error is below 1.1 dB for $D/2^n < 0.75$.

The bandwidth of the proposed DCCF is determined by the sum of the parasitic and compensation capacitances at node A and the transconductance value of the digitally controlled transconductor from the A to the X terminals

$$\text{Bandwidth} = \frac{g_m}{(C_P + C_C)\left(1 + \frac{1}{g_{m2} r_o}\right)} \approx \frac{g_{m0}\left(1 - \frac{D}{2^n}\right)}{(C_P + C_C)\left(1 + \frac{1}{g_{m2} r_o}\right)} \qquad (4)$$

where g_m is the small signal transconductance of the digitally controlled transconductor, g_{m0} is its transconductance when $D = 0$, r_o is the output resistance of the input current source, and g_{m2} is that transconductance of M2. Unfortunately, the bandwidth of the DCCF is a function of the digital input control word D. To circumvent this problem, a programmable compensation capacitor is used as will be shown in section 3. The implementation of the digitally controlled transconductor is based on a novel current division technique that will be described in the next section.

3. The Current Division Principle

The traditional approach to implement the current division network (CDN) is to use the well-known resistive ladder circuit as shown in **Fig. 3**. For proper operation of the circuit, all the resistors in the network must be matched. This may be very difficult

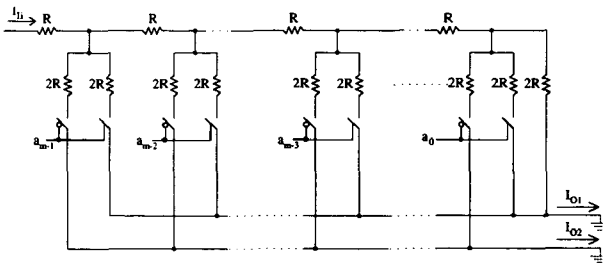

Fig. 3: Classical resistive ladder

to achieve in practice specially when using a large CDN. Furthermore, the switches which are used to switch the current either to the I_{O1} or I_{O2} branches are usually implemented using MOS transistors which have finite on-resistances. These finite resistances affect the accuracy of current division. Another drawback is that the output resistance of the resistive CDN depends on the resistance value and the digital control word. Moreover, for accurate current division, the output nodes I_{O1} or I_{O2} should be at virtual ground voltages. This means that the output resistance of the CDN should be sufficiently larger than the input resistance of the next stage. Also, the resistive ladder has an input resistance of R. Therefore, to be able to handle high current levels in low voltage applications, it is necessary to reduce the value of R. However, this reduction results in a smaller output resistance and puts a stringent requirement on the next stage input resistance. Hence there is a trade off between the input and output resistances by choosing the value of R.

A better approach to implement the CDN is to use the MOS ladder circuit. Although the structure of this circuit is similar to the classical resistor based R-$2R$ ladder; the transistors do not have to emulate identical resistors. It can be shown that in spite of the nonlinear relationship between current and voltage of an MOS transistor, the current division function is inherently linear. The CDN is based on the linear current division principle, the basic circuit of which is depicted in **Fig. 4** [11]. Voltage V is a dc voltage and may have any value as long as the transistors are in the on state. The input current is divided into two currents, I_{d1} and I_{d2}. The ratio of the two currents is given by

$$\frac{I_{d1}}{I_{d2}} = \frac{\frac{W_1}{L_1}}{\frac{W_2}{L_2}}. \qquad (5)$$

This ratio is independent of the value of I_I, implying low distortion. Also, it is independent of the values of V_g and V. Finally, it is insensitive to second order effects like mobility degradation and body effect and independent of the operation region of the two

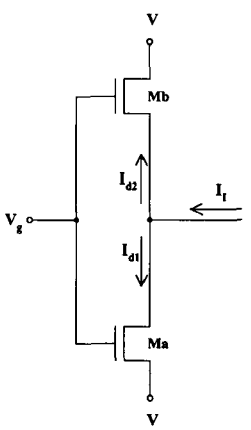

Fig. 4: The basic principle of current division

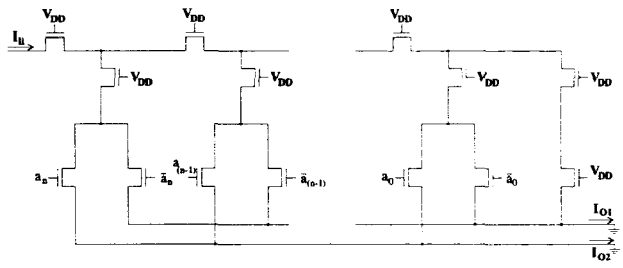

Fig. 5: The current division network

MOS transistors. The MOS ladder based CDN is shown in **Fig. 5**. This CDN has an advantage over its resistor-based counterpart that the MOS transistors are used as switches and as resistive elements. That is the MOS switch is a part of the network, while in the resistive ladder the MOS transistor is used only for switching the current and its resistance should be as small as possible. Furthermore, in order to have finite input resistance, the MOS transistors should not operate in the saturation region. However, MOS ladder CDN still suffers from the drawbacks of the resistive ladder stated above such as the finite output resistance and the need for matching all the transistors in the circuit.

The proposed approach to implement the CDN that overcomes the drawbacks mentioned above is based on the current steering cell (CSC) shown in **Fig. 6**. In such cell, the input current I_{i+1} is divided equally between two branches by the matched PMOS transistors MAi which are assumed to operate in the saturation region. However, if the two output nodes are assumed to be at the same voltage, the circuit will operate correctly regardless of the region of operation of the two transistors. In spite of that, if the transistors operate in the ohmic region, the output resistance of the CSC will be low which will have detrimental effects on the bandwidth of the VGA as it is clear from (4). Consequently, the biasing voltage $V_{BP(n-i)}$ will be adjusted such that the two transistors operate in the saturation region.

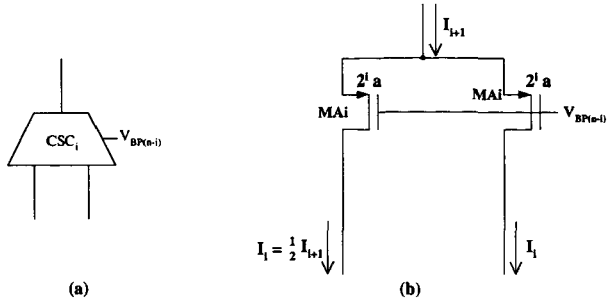

Fig. 6: The current steering cell (CSC)

The P part of the digitally controlled transconductor based on the proposed CSC is shown in **Fig. 7**. A similar circuit for the N part is realized using NMOS transistors. In Fig. 7, the current I_P is divided by CSC_n into two equal currents. One of these currents is fed to the output node I_{P2} passing through the MA(n) transistors which are added to equalize the load resistance at the outputs of CSC_n. Hence, the two output nodes of CSC_n will be at the same voltage and channel length modulation will have no effect on the current division action of CSC_n. The other output current of CSC_n is further divided by $CSC_{(n-1)}$, and so on. The final divided currents are then switched either to I_{P2} or I_{P3} using current demultiplexers which are implemented using MOS transistors as shown in **Fig. 8**. The output currents I_{P1}, I_{P2}, and I_{P3} are expressed as

$$I_{P1} = I_P \frac{W_B / L_B}{2^n a} \tag{6}$$

$$I_{P2} = \frac{I_P}{2}\left(1 + \frac{D}{2^n}\right) \tag{7}$$

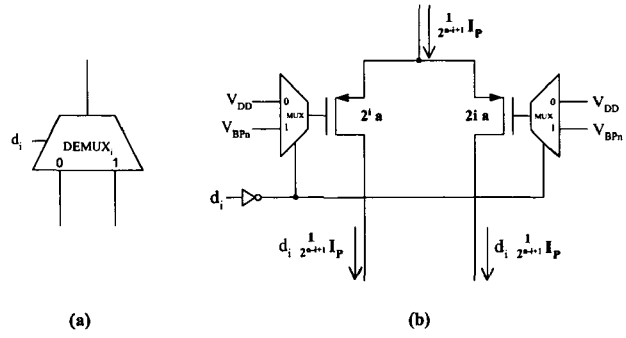

Fig. 8: The current demultiplexer
(a) symbol
(b) realization

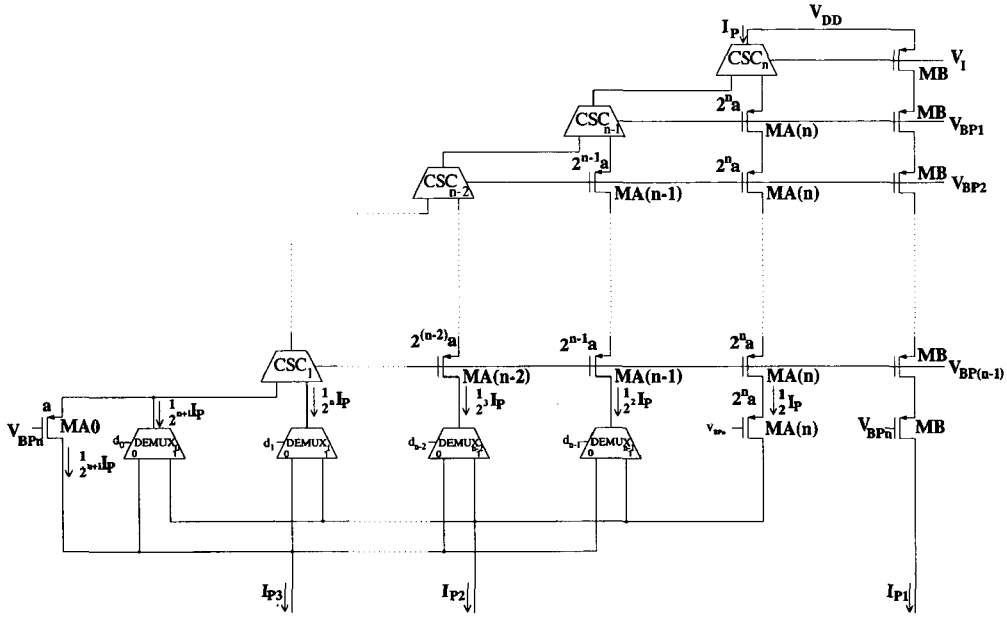

Fig. 7: The P part of the proposed digitally controlled transconductor

$$I_{P3} = \frac{I_P}{2}\left(1 - \frac{D}{2^n}\right) \tag{8}$$

where

$$I_P = \frac{K_{An}}{2}\left(V_{DD} - V_I - V_{TN}\right)^2. \tag{9}$$

Hence the ratio between I_{P2} and I_{P3} is given by

$$\frac{I_{P2}}{I_{P3}} = \frac{1 + \frac{D}{2^n}}{1 - \frac{D}{2^n}} \tag{10}$$

where D is given by:

$$D = d_0 + 2d_1 + 4d_2 + \cdots + 2^n d_n. \tag{11}$$

Since the output currents are drawn from the drain of the transistors, the output resistance is very high. Hence, there is no need for virtual ground voltage at the output nodes. Consequently, the aspect ratios of the transistors can be chosen arbitrary to achieve the required current level without putting stringent requirement on the next stage. However, if the output nodes are at virtual ground voltage, then the accuracy of the current gain will not be affected by the channel length modulation and the body effect. Besides, matching requirements are relaxed in the sense that only the transistors comprising a differential pair are required to be matched rather than matching all the transistors in the entire circuit. Although certain relations between the aspect ratios of the transistors in the circuit have to be satisfied, these relations are put to minimize the channel length modulation effect. Hence, mismatches in the transistors that are not in the same differential pair will have a very little effect on the accuracy of current division. Additionally, higher current drive capability is expected than in the case of MOS ladder for the same aspect ratios of the transistors, as the transistors are assumed to operate in the saturation region. Finally the circuit is independent of the body effect as sources of the transistors to be matched are either connected or have the same voltage. The biasing voltages V_{Bi} (i = 0, 1, 2, ..., n) are generated from the circuit shown in **Fig. 9**. Where I_M is the maximum current that can flow in the circuit. The aspect ratio of the diode connected transistor MCi is given by

$$\left(\frac{W}{L}\right)_i = \frac{2^{n-1}a}{(i+1)^2}. \tag{12}$$

This relation guarantees that the all the transistors in the circuit will remain in the saturation region as long as the current I_P is less than I_M.

According to equation (12), the minimum compliance voltage required to operate the CDN is given by:

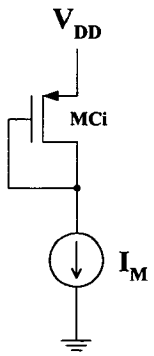

Fig. 9: The biasing circuit of the proposed transconductor

$$V_{min} = \sum_{i=0}^{n} V_{dsati} = \sum_{i=0}^{n} \sqrt{\frac{I_i}{K_i}} = (n+1)\sqrt{\frac{I_M}{K_n}} = (n+1)V_{dsatn} \tag{13}$$

where V_{dsati} is the saturation voltage of the i^{th} CSC. The above equation reveals the interesting property of the CDN that only the saturation voltages of the transistors are added to V_{min} by stacking the CSC cells.

4. Mismatch Effects

In this section, the effect of the threshold voltage mismatch and the gain mismatch on the current division is studied. It can be shown that the mismatch in the output current of the i^{th} CSC is given by

$$\Delta I_i = \sqrt{\frac{K_i I_i}{2}}\Delta V_{Ti} + \frac{\Delta r_i}{2} I_i - \frac{1}{2}\Delta I_{i+1} \tag{14}$$

where:

ΔV_{Ti} is the threshold voltage mismatch in the i^{th} CSC cell

Δr_i is the aspect ratio mismatch in the i^{th} CSC cell.

Substituting the K_i and I_i in terms of K_n and I_n respectively, the following equation can be obtained:

$$\begin{aligned}\Delta I_i &= \frac{1}{2^{n-i}}\left(\sqrt{\frac{K_n I_n}{2}}\Delta V_{Ti} + \frac{\Delta r_i}{2} I_n\right) - \frac{1}{2}\Delta I_{i+1} \\ &= \frac{1}{2^{n-i}}\Delta_i - \frac{1}{2}\Delta I_{i+1}\end{aligned} \tag{15}$$

where

$$\Delta_i = \sqrt{\frac{K_n I_n}{2}}\Delta V_{Ti} + \frac{\Delta r_i}{2} I_n$$

This is a recursive equation which can be simplified to:

$$\Delta I_i = \frac{1}{2^{n-i}} \sum_{\ell=i}^{n} (-1)^{\ell-i} \Delta_\ell. \tag{16}$$

The maximum current error occurs when $|\Delta_i| = \Delta_{max}$ and the polarity Δ_i is alternating, then:

$$\left|\Delta I_{i\,max}\right| = \Delta_{max} \frac{n-i+1}{2^{n-i}}. \tag{17}$$

In this case, the polarity of ΔI_{imax} will be alternating. The output currents I_{P2} and I_{P3} can be written as:

$$I_{P2} = \sum_{i=0}^{n-1} d_i I_i + \frac{I_n}{2} \tag{18}$$

$$I_{P3} = I_P - I_{P2}. \tag{19}$$

Then,

$$\Delta I_{P2} = -\Delta I_{P3} = \Delta_{max}\left(\sum_{i=0}^{n-1} (-1)^i d_i \frac{n-i+1}{2^{n-i}} + (-1)^n\right). \tag{20}$$

The gain of the VGA is given by

$$G = \frac{I_{N2} - I_{P2}}{I_{N3} - I_{P3}}. \tag{21}$$

Because of the class AB operation, the gain can be approximated as:

$$G = \frac{I_{P2}}{I_{P3}} \qquad \text{when } I_x < 0$$

and

$$G = \frac{I_{N2}}{I_{N3}} \qquad \text{when } I_x > 0. \tag{22}$$

Then,

$$\frac{\Delta G}{G} = \frac{\Delta\left(\frac{I_{P2}}{I_{P3}}\right)}{\frac{I_{P2}}{I_{P3}}} = \frac{\Delta I_{P2}}{I_{P2}} - \frac{\Delta I_{P3}}{I_{P3}} = \Delta I_{P2}\left(\frac{1}{I_{P2}} + \frac{1}{I_P - I_{P2}}\right)$$

when $I_x < 0$

and

$$\frac{\Delta G}{G} = \Delta I_{N2}\left(\frac{1}{I_{N2}} + \frac{1}{I_N - I_{N2}}\right) \qquad \text{when } I_x > 0. \tag{23}$$

5. The Fully Differential VGA

The DCCF presented in the previous section deals with single ended signals. However, in mixed mode applications, fully differential signal processing is necessary to suppress the common mode noise generated by digital circuits that are the most serious source of noise due to clock feedthrough and charge injection. Block diagram of a fully differential DCCF is shown in **Fig. 10**. Common mode feedback is achieved via the two differential pairs (M13 through M16) and the output currents I_{C+} and I_{C-} of the two DCCFs. The gain of the fully differential DCCF (FDDCCF) is the same as that given by (3).

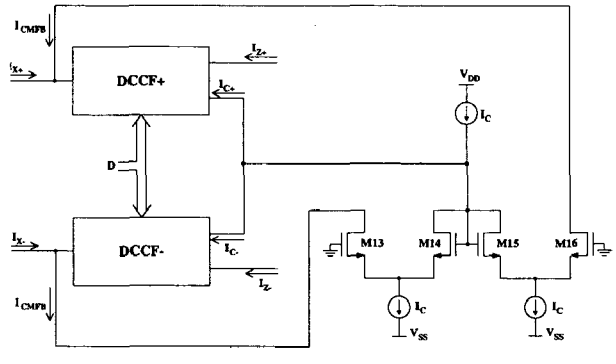

Fig. 10: The fully differential DCCF (FDDCCF)

The block diagram of the fully differential VGA is shown in **Fig. 11**. It consists of three FDDCCF stages. In the first two stages, n = 2, and the gain has only two values, 1 (0 dB when $D_{1,2}$ = 0) and 7 (16.9 dB when $D_{1,2}$ = 3). This is achieved by shorting the two digital input bits d_0 and d_1 in each of the first two stages. Hence, the gain of the first two stages has only three values, 0, 16.9, or 33.8 dB. This is a relatively large gain step. Fine gain control is achieved through the third stage in which n = 3 and the gain is varied between 0 dB (D_3 = 0) to 16.9 dB (D_3 = 6) with an average step of 2.8 dB.

The overall bandwidth of the VGA is determined by the bandwidths of the individual stages which is shown to be dependent

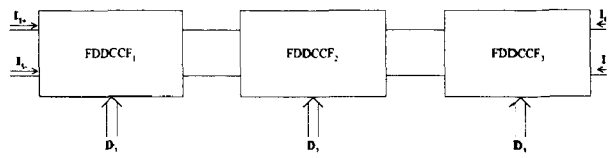

Fig. 11: The fully differential VGA

on the digital input control (4). One of the design goals of the VGA is to have a constant bandwidth. In other words, the bandwidth of the VGA should be independent of the selected gain. To achieve this constant bandwidth in the presence of the variable transconductance, a digitally controlled compensation capacitor shown in **Fig. 12** is used. The equivalent input capacitance of the circuit (neglecting the MOS resistance) is given by

$$C_C = C + \Delta C(\overline{d_0} + 2\overline{d_1} + \cdots + 2^{n-1}\overline{d_{n-1}}) = C + \Delta C(2^n - 1 - D). \tag{24}$$

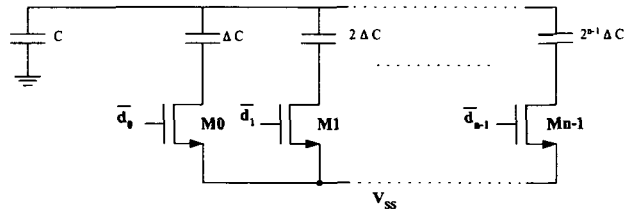

Fig. 12: The digitally controlled compensation capacitor

The attentive reader may note that the sources of the transistor switches are connected to the V_{SS} terminal not the ground terminal to decrease the on-resistances of the MOS switches.

From (4) and (24), it can be shown that the condition for constant bandwidth is

$$\Delta C = C_P + C. \tag{25}$$

For the first two stages, there are two control bits which are shorted together to give two gain values. Hence the circuit of Fig. 12 can be simplified by lumping the transistors into a single transistor together with a capacitor.

6. Simulation Results

The proposed current mode VGA circuit has been simulated with SpectreS using the AMI 0.5 μm BSIM models provided by MOSIS. The aspect ratios of the transistors are given in **Table 1**. Supply voltages used are ±1.5 V. Simulation is performed with the bodies of all transistors connected to the appropriate supply voltage. The biasing currents and voltages and other parameters used in the simulation are given in **Table 2**. **Fig. 13** shows the short circuit output current when the input current is swept from -3 μA to 3 μA at the maximum gain (50.7 dB). Frequency response of the VGA is shown in **Fig. 14** for different gain values. From the figure it is seen that the bandwidth is approximately constant (about 21 MHz). **Fig. 15** shows the intermodulation distortion (IMD) with differential input current at 5 MHz and 6 MHz, both with an amplitude of 0.5 μA at the maximum VGA gain. It can be seen that the IMD components at 4 MHz and 7 MHz are 41 dB below. Step response of the proposed VGA is shown in **Fig. 16** when a square wave of 1 MHz and 0.5 μA is applied to the input when the gain is set to its maximum value (50.7 dB). Due to the class AB operations, the total harmonic distortion (THD) is expected to increase when the input amplitude is decreased. This is depicted in **Fig. 17**, when a differential sinusoidal current is applied to the input with 10 MHz frequency and amplitude varies from 0 to

Table 1: Aspect ratios of the transistors

Transistor	Aspect ratio (*W/L*)
M1, M2, M3, M4	9.6/2.4
M5, M6, M7, M8	19.2/2.4
M9, M10	2.4/2.4
M11	24/2.4
M12	76/2.4
M13, M14, M15, M16	12/1.2

Table 2: Biasing currents and voltages, and other parameters used in the simulation

Element	Value
I_B, I_{SB}	20 μa
I_C	40 μa
V_{BN}	1.11 V
V_{BP}	0.089 V
a (P part, 1st and 2nd stages)	18/0.6
a (N part, 1st and 2nd stages)	6/0.6
a (P part, 3rd stage)	9/0.6
a (N part, 3rd stage)	3/0.6
C (1st and 2nd stages)	0.2 pF
ΔC(1st and 2nd stages)	0.7 pF

0.5 μA at the maximum gain of the VGA. The actual gain profile is shown in **Fig. 18** together with the ideal gain profile. The maximum gain error is below 2 dB. The simulated equivalent input density of white noise is 2.76 pA/$\sqrt{\text{Hz}}$ and the total power dissipation is 1.5 mW.

7. Conclusion

In this paper, a fully differential digitally controlled current mode VGA is presented. The proposed VGA is based on a novel current division technique. Class AB output stage is used to control the standby current consumption. The circuit can operate from supply voltages as low as ±1.5V.

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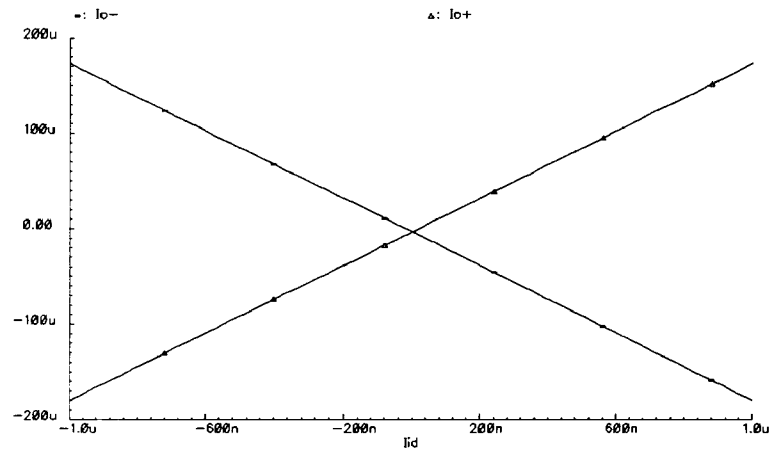

Fig. 13: The balanced output currents versus the differential input current (gain 50.7 dB)

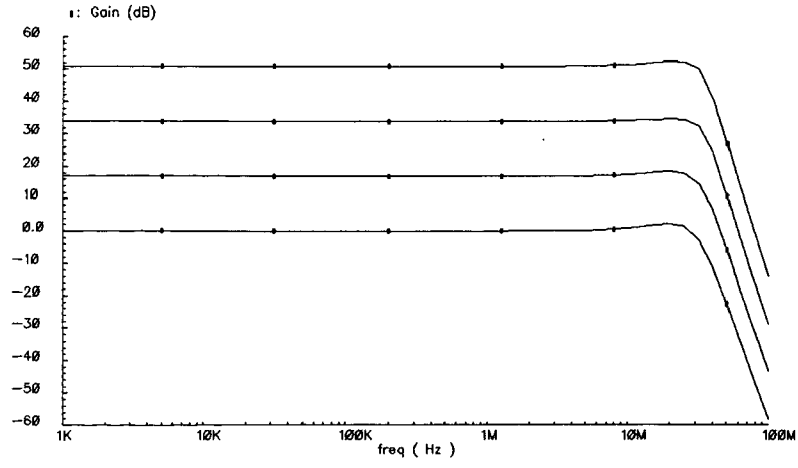

Fig. 14: Frequency response of the VGA (gain 50.7 dB)

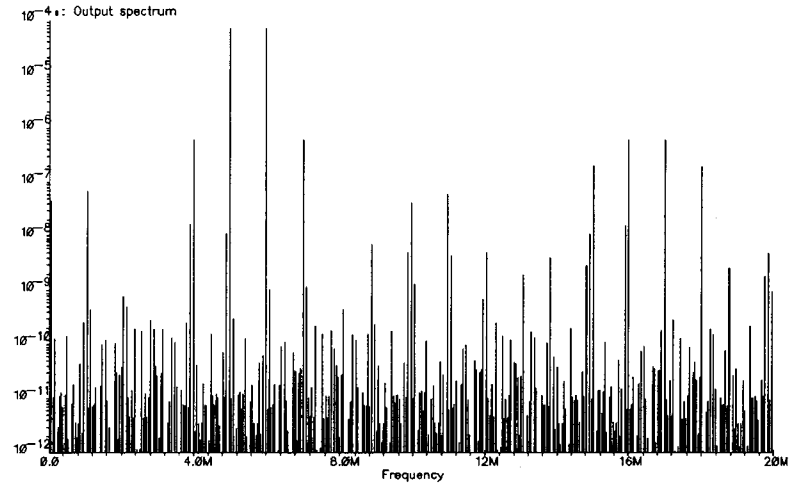

Fig. 15: IMD with a 5 MHz and 6 MHz input with 0.5 μA amplitude each

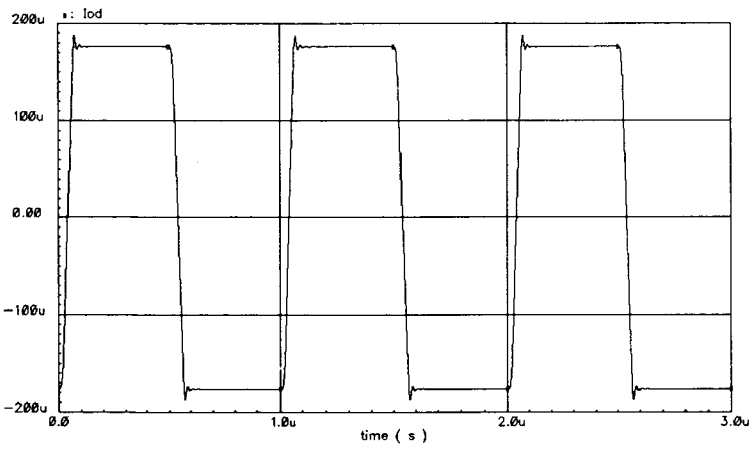

Fig. 16: Step response of the VGA

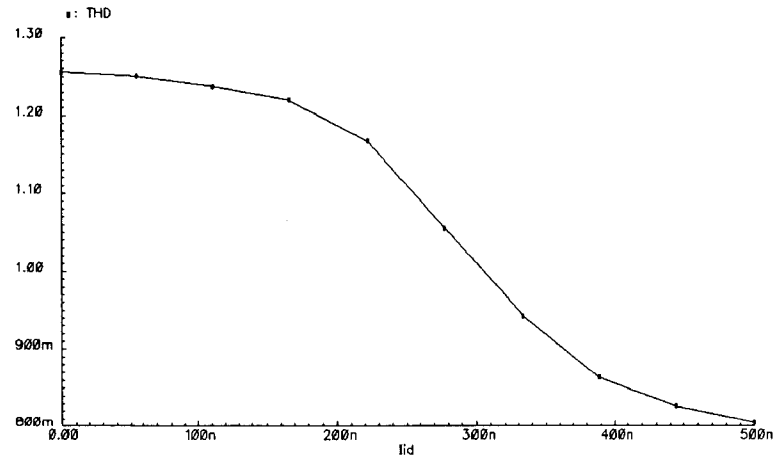

Fig. 17: THD versus the amplitude of the sinusoidal input current

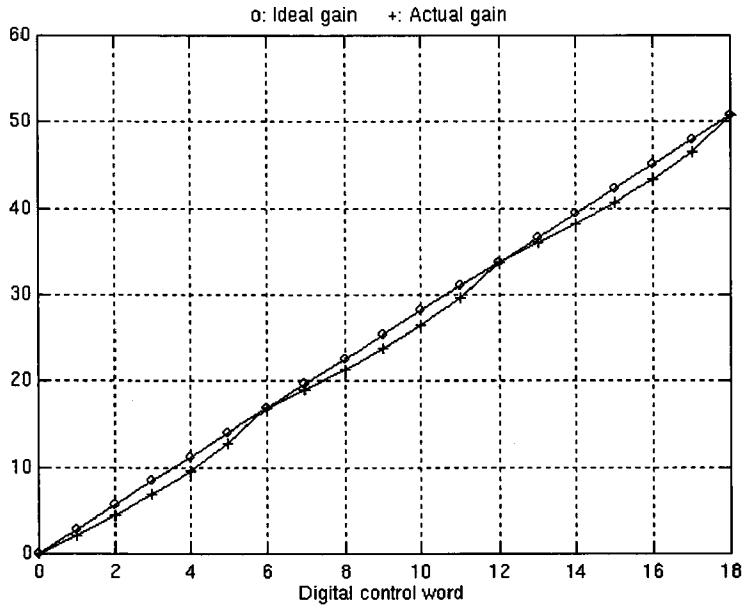

Fig. 18: Actual and ideal gain profiles

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