Journal of Circuits, Systems, and Computers
Vol. 21, No. 1 (2012) 1250010 (17 pages)

DOI: 10.1142/S0218126612500107

World Scientific
www.worldscientific.com

CLASSIFICATION AND PATHOLOGICAL REALIZATIONS OF TRANSCONDUCTANCE AMPLIFIERS*

AHMED M. SOLIMAN

Electronics and Communication Engineering Department,
Faculty of Engineering, Cairo University, Egypt 12613
asoliman@ieee.org

Received 27 October 2010
Accepted 18 August 2011
Published 29 February 2012

Classification of transconductance amplifiers (TA) based on the number of input ports and output ports is given. A systematic generation method of TA based on using nullator, norator elements, and pathological mirror elements is used to provide pathological realizations of different types of TA. Four pathological realizations of the single input balanced output TA each using two grounded G are given. Four pathological realizations of the differential input single output TA each using two grounded G are given.

Six pathological realizations of the differential input balanced output TA known as BOTA are given. Three pathological realizations for each of the two types of the differential input double output TA are also given. Finally, four alternative ideally equivalent realizations of the BOTA using two current conveyors (CCII) or two inverting current conveyors (ICCII) are generated from the pathological realizations.

Keywords: Transconductor; nullator; norator; voltage mirror; current mirror.

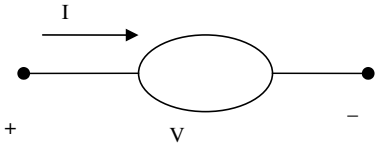
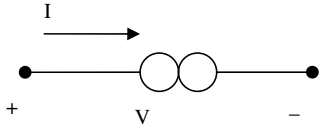
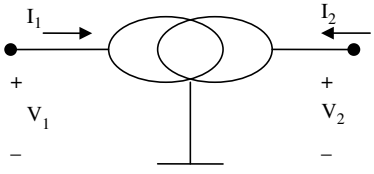
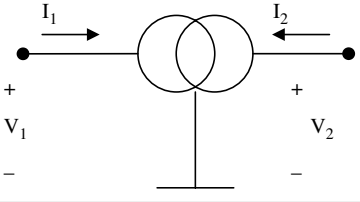
1. Introduction

Several CMOS realizations of the transconductance amplifier (TA) have been reported in the literature.[1–14] The use of TA as a basic building block in active circuits has been demonstrated in several papers.[15–27] Only very few nullor representations of the TA have appeared in the literature.[26–30]

In this paper the nodal admittance matrix (NAM) expansion method introduced in Ref. 28 to realize active building blocks is extended to accommodate the pathological voltage mirror (VM) and the pathological current mirror (CM) together with the nullator and norator[31] thus resulting in a complete set of active circuits realizing TA. For a physically realizable circuit, all the voltages and currents are

*This paper was recommended by Regional Editor Piero Malcovati.

Table 1. Summary of the definitions and symbols of the pathological elements.

Pathological element	Definition	Symbol
Nullator	$V = I = 0$.	
Norator	V and I are arbitrary	
Voltage mirror	$V_1 = -V_2$, $I_1 = I_2 = 0$.	
Current mirror	V_1 and V_2 are arbitrary $I_1 = I_2$, and they are also arbitrary	

always uniquely and definitely determined. This in turn implies that in the ideal representation of a physically realizable circuit, nullators (or VM) and norators (or CM) must occur in a pair.[32–37] Table 1 includes a summary of the four pathological elements and their definitions.

The key steps in the NAM expansion are summarized as follows:

(a) A nullator connected between two columns moves a circuit element from one column to the other column with the same sign.
(b) A norator connected between two rows moves a circuit element from one row to the other row with the same sign.
(c) A VM connected between two columns moves a circuit element from one column to the other column with opposite sign.
(d) A CM connected between two rows moves a circuit element from one row to the other row with opposite sign.

The nullator and norator are represented by straight brackets as in Ref. 28. VM and CM are represented by curved brackets as in Ref. 37.

There are two types of the single input single output TA according to the direction of the output current. The single input single output TA with output current pointing inward is defined as TA− and is also known as the voltage-controlled current source (VCCS). The single input single output TA with output current pointing outward is defined as TA+. The single input single output TA is not included in this paper as it is related to the systematic generation method of controlled sources using unity gain cells that has been introduced recently in the literature.[38]

2. Single Input Balanced Output TA

The admittance matrix of the single input balanced output TA is given by

$$Y = \begin{bmatrix} 0 & 0 & 0 \\ G & 0 & 0 \\ -G & 0 & 0 \end{bmatrix}. \tag{1}$$

From the above NAM it is seen that the single input balanced output TA is a floating active element.[39]

There are four alternative pathological realizations of the single input balanced output TA using two grounded G as will be explained below.

Adding a fourth blank row and column to Eq. (1) and connecting a nullator between columns 1 and 4 and a norator between rows 2 and 4 will move G to the diagonal position 4, 4 as follows:

$$Y = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ -G & 0 & 0 & 0 \\ 0 & 0 & 0 & G \end{bmatrix}. \tag{2}$$

Adding a fifth blank row and column to Eq. (2) and connecting a VM between columns 1 and 5 and a norator between rows 3 and 5 will move $-G$ to the diagonal position 5, 5 to become G as follows:

$$Y = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & G & 0 \\ 0 & 0 & 0 & 0 & G \end{bmatrix}. \tag{3}$$

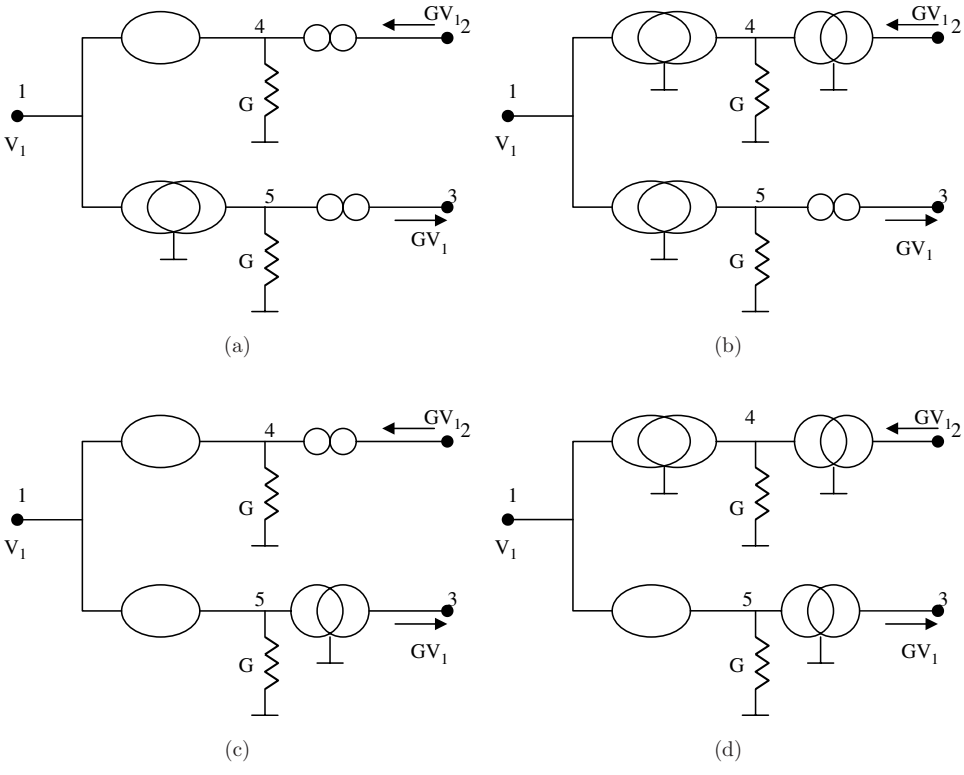


Fig. 1. (a) Realization 1 of the single input balanced output TA. (b) Realization 2 of the single input balanced output TA. (c) Realization 3 of the single input balanced output TA. (d) Realization 4 of the single input balanced output TA.

The above NAM is realized as shown in Fig. 1(a).

The other three realizations shown in Figs. 1(b)−1(d) can be obtained in a similar way.

3. Differential Input Single Output TA

The admittance matrix of the differential input single output TA is given by

$$Y = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ G & -G & 0 \end{bmatrix}. \tag{4}$$

There are four alternative pathological realizations of the differential input single output TA using two grounded G as will be explained later.

Adding a fourth blank row and column to Eq. (4) and connecting a nullator between columns 1 and 4 and a norator between rows 3 and 4 will move G to the

diagonal position 4, 4 as follows:

$$Y = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & -G & 0 & 0 \\ 0 & 0 & 0 & G \end{bmatrix} . \tag{5}$$

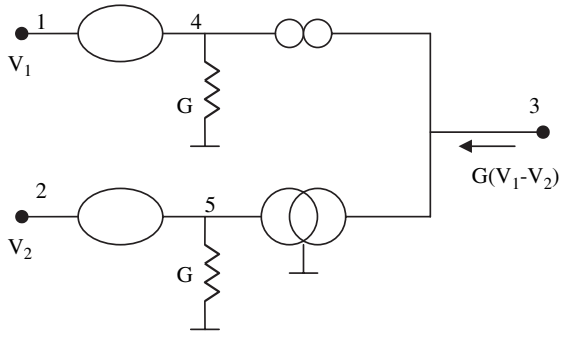
Adding a fifth blank row and column to Eq. (5) and connecting a nullator between columns 2 and 5 and a CM between rows 3 and 5 will move $-G$ to the diagonal position 5, 5 to become G as follows:

$$Y = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & G & 0 \\ 0 & 0 & 0 & 0 & G \end{bmatrix} . \tag{6}$$

The above NAM is realized as shown in Fig. 2(a).

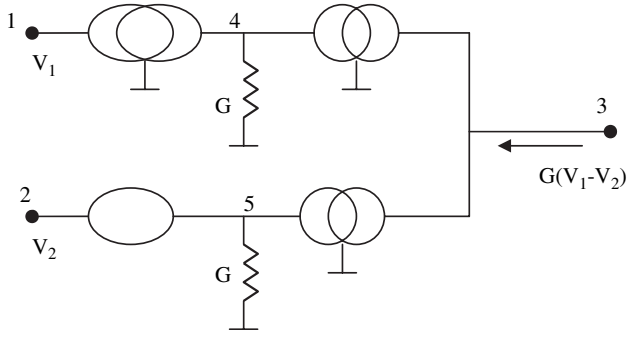
The other three realizations shown in Figs. 2(b)−2(d) can be obtained in a similar way.

Table 2 summarizes the properties of the different realizations of the single input balanced output TA and the differential input single output TA.

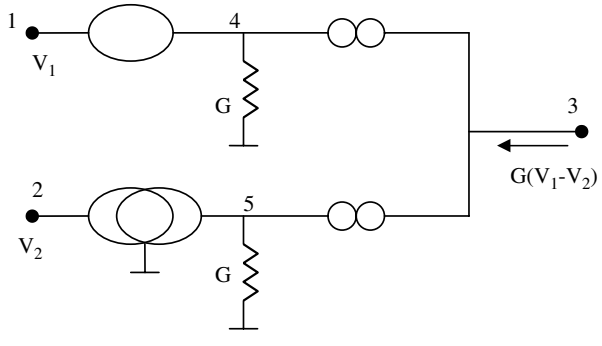


(a)

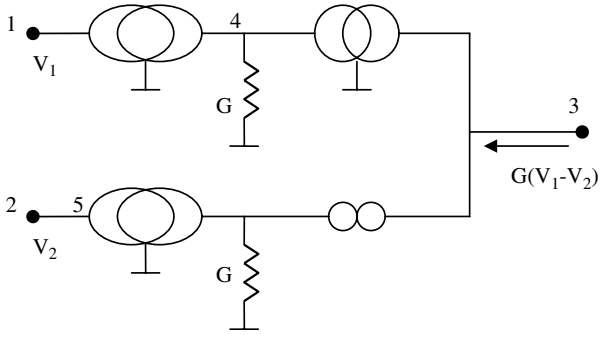
Fig. 2. (a) Realization 1 of the differential input single output TA. (b) Realization 2 of the differential input single output TA. (c) Realization 3 of the differential input single output TA. (d) Realization 4 of the differential input single output TA.



(b)



(c)



(d)

Fig. 2. (*Continued*)

4. Differential Input Two-Output TA

There are three types of the differential input two-output TA according to the directions of the output currents.

Table 2. Properties of single input balanced output TA and its adjoint (with input and output ports interchanged).

Figure no.	Nullator	VM	Norator	CM	Adjoint to figure no.
1(a)	1	1	2	0	2(a)
1(b)	0	2	1	1	2(b)
1(c)	2	0	1	1	2(c)
1(d)	1	1	0	2	2(d)
2(a)	2	0	1	1	1(a)
2(b)	1	1	0	2	1(b)
2(c)	1	1	2	0	1(c)
2(d)	0	2	1	1	1(d)

4.1. *Differential input balanced output TA (BOTA)*

The admittance matrix of the BOTA is given by

$$Y = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ G & -G & 0 & 0 \\ -G & G & 0 & 0 \end{bmatrix}. \tag{7}$$

From the above NAM it is seen that the summation of each column in the NAM is zero; thus, BOTA has the property of being a floating active element.[39]

There are four pathological realizations of BOTA using a floating G.

The generation method using NAM expansion for realization 1 of the BOTA is given next.

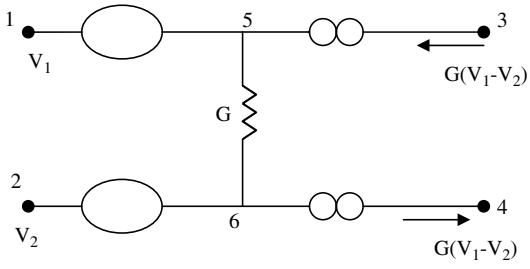
Adding two blank rows and columns to Eq. (7) and connecting two nullators between columns 1, 5 and 2, 6 and two norators between rows 3, 5 and 4, 6 result in the following expanded NAM:

$$Y = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & G & -G \\ 0 & 0 & 0 & 0 & -G & G \end{bmatrix}. \tag{8}$$

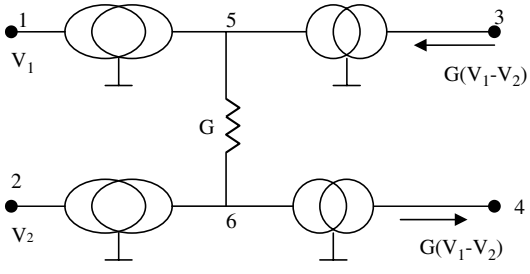
The above NAM is realized as shown in Fig. 3(a).

Similarly, the three other realizations can be obtained and are shown in Figs. 3(b)–3(d).

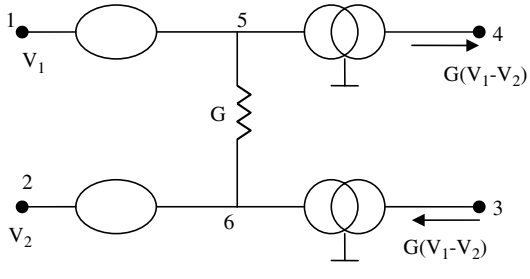
Two new realizations of the BOTA using two grounded G are shown in Figs. 4(a) and 4(b). It should be noted that the two realizations are adjoints to each other after interchanging inputs and output ports.



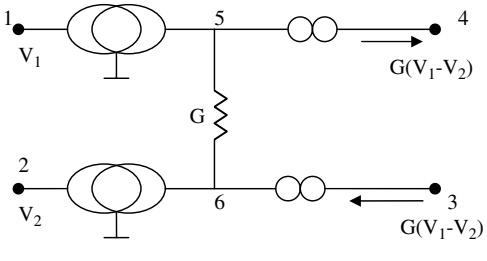
(a)



(b)

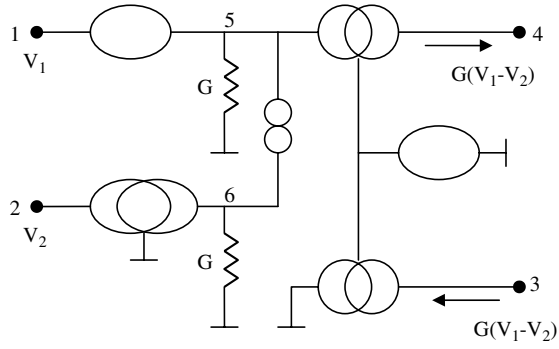


(c)

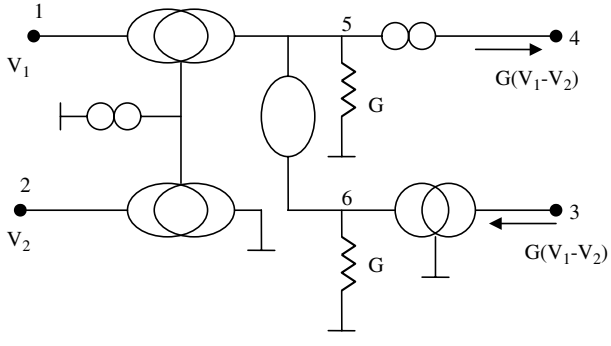


(d)

Fig. 3. (a) Realization 1 of the BOTA.[26,27] (b) Realization 2 of the BOTA. (c) Realization 3 of the BOTA. (d) Realization 4 of the BOTA.



(a)



(b)

Fig. 4. (a) Realization 1 of the BOTA using two grounded G. (b) Realization 2 of the BOTA using two grounded G.

Table 3 summarizes the properties of the six BOTA realizations and their adjoints. It should be noted that the adjoint TA realization is based on the inputs and output ports being interchanged.

Table 3. Properties of the BOTA and its adjoint (with inputs and output ports interchanged).

Figure no.	Nullator	VM	Norator	CM	Adjoint to figure no.
3(a)	2	0	2	0	3(a)
3(b)	0	2	0	2	3(b)
3(c)	2	0	0	2	3(d)
3(d)	0	2	2	0	3(c)
4(a)	2	1	1	2	4(b)
4(b)	1	2	2	1	4(a)

4.2. *Differential input double output TA− (DOTA−)*

The admittance matrix of the differential input DOTA with the two output currents pointing inward is described by

$$Y = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ G & -G & 0 & 0 \\ G & -G & 0 & 0 \end{bmatrix}. \tag{9}$$

There are two pathological realizations of the differential input DOTA− using a floating G. The generation method using NAM expansion for realization 1 is explained next.

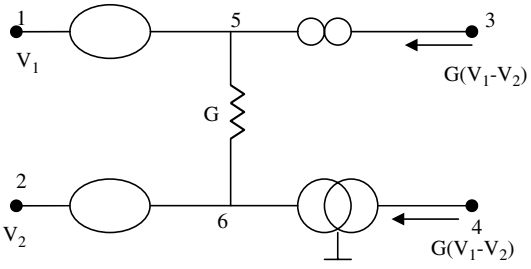
Adding two blank rows and columns to Eq. (9) and connecting two nullators between columns 1, 5 and 2, 6 and a norator between rows 3, 5 and a CM between rows 4, 6 result in the following expanded NAM:

$$Y = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & G & -G \\ 0 & 0 & 0 & 0 & -G & G \end{bmatrix}. \tag{10}$$

The above NAM is realized as shown in Fig. 5(a).

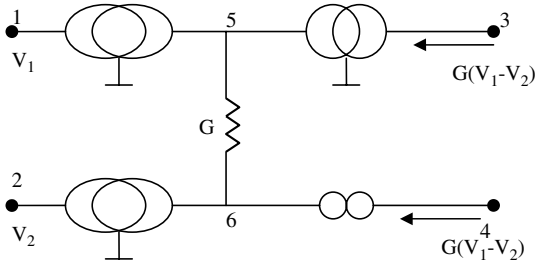
The other realization shown in Fig. 5(b) can be obtained in a similar way.

A new realization of the DOTA− using two grounded G is given in Fig. 5(c).

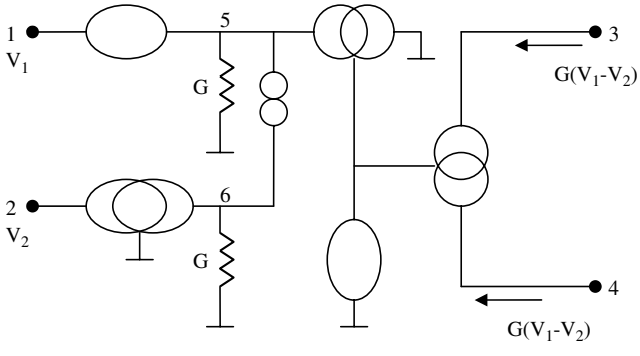


(a)

Fig. 5. (a) Realization 1 of the differential input DOTA−. (b) Realization 2 of the differential input DOTA−. (c) Realization of the DOTA− using two grounded G.



(b)



(c)

Fig. 5. (*Continued*)

4.3. *Differential input double output TA+ (DOTA+)*

The admittance matrix of the differential input DOTA with the two output currents pointing outward is described by

$$Y = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ -G & G & 0 & 0 \\ -G & G & 0 & 0 \end{bmatrix}. \tag{11}$$

Two new realizations of the differential input DOTA+ are shown in Fig. 6, and can be derived as in the previous case.

A new realization of the DOTA+ using two grounded G is given in Fig. 6(c).

Table 4 summarizes the properties of the three different realizations of DOTA− and DOTA+.

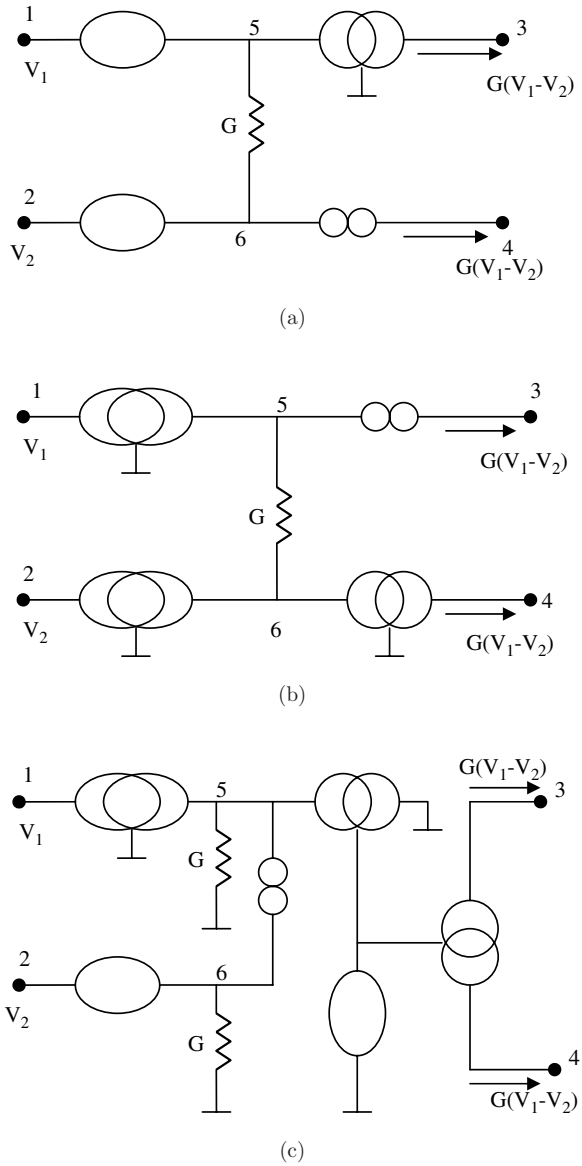


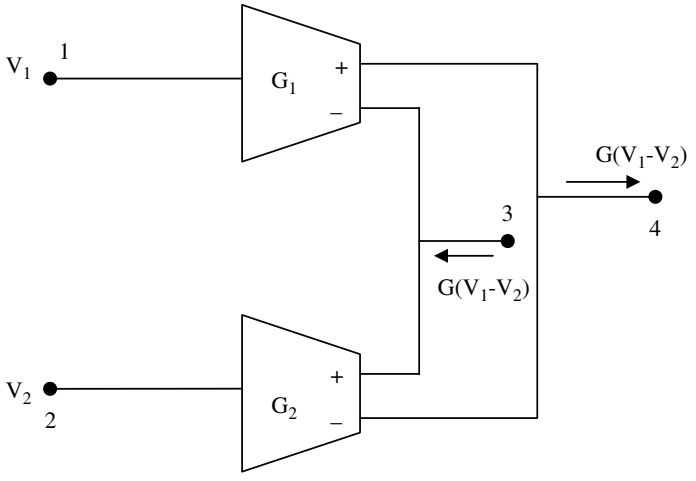
Fig. 6. (a) Realization 1 of the differential input DOTA+. (b) Realization 2 of the differential input DOTA+. (c) Realization of the DOTA+ using two grounded G.

5. Properties and Alternative Realizations of BOTA

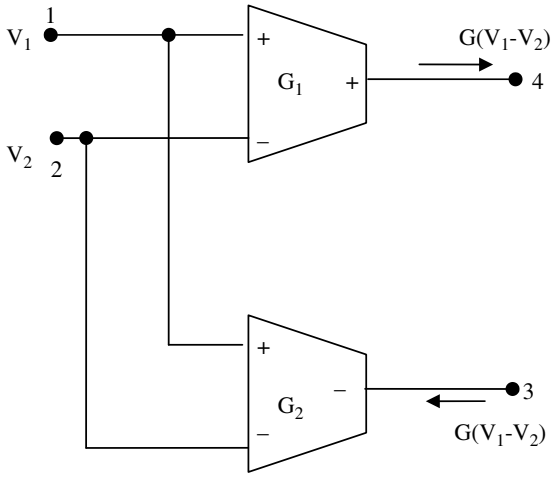
Among all different types of TA considered in this paper, BOTA is the only TA that is floating and its adjoint is also a BOTA as seen from Table 3. It can also be seen that the BOTA circuits of Figs. 3(a) and 3(b) are self-adjoint.

Table 4. Properties of differential input DOTA.

Figure no.	Nullator	VM	Norator	CM
5(a), 6(a)	2	0	1	1
5(b), 6(b)	0	2	1	1
5(c), 6(c)	2	1	1	2



(a)



(b)

Fig. 7. (a) Realization of BOTA from two matched single input balanced output TA. (b) Realization of BOTA from two differential input single output TA.

In this section, realizations of BOTA from other types of TA as well as from current conveyors (CCII)[40] or inverting current conveyors (ICCII)[32] are briefly discussed.

5.1. *Realization of BOTA from other TA*

BOTA can be realized from two matched single input balanced output TA as shown in Fig. 7(a). Two differential input single output TA having G_1 equal to G_2 can also be used to realize the BOTA as given in Fig. 7(b).[41]

5.2. *Realization of BOTA from CCII or ICCII*

This section demonstrates the importance of the pathological realizations in obtaining alternative ideally equivalent realizations.

The two CCII− circuit realizing the BOTA and shown in Fig. 8(a) is generated from Fig. 3(a). It can be seen that this is a self-adjoint circuit.[39]

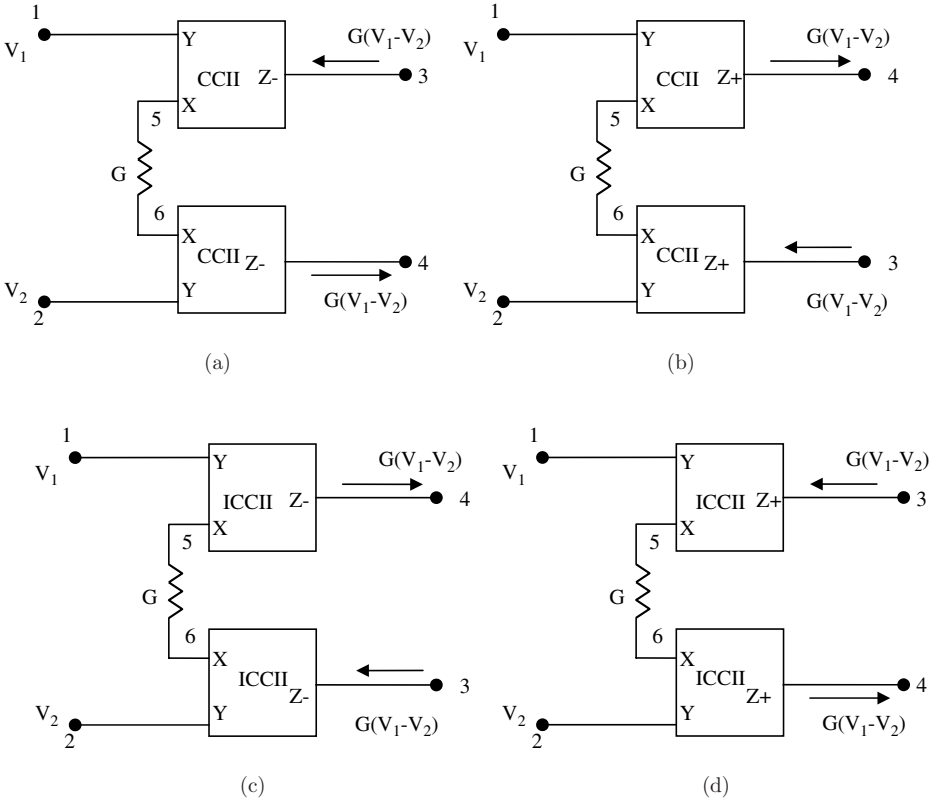


Fig. 8. (a) Realization of BOTA using two CCII−. (b) Realization of BOTA using two CCII+. (c) Realization of BOTA using two ICCII−. (d) Realization of BOTA using two ICCII+.

The two CCII+ circuit realizing the BOTA and shown in Fig. 8(b) is generated from Fig. 3(c). This is not a self-adjoint circuit; on the other hand its adjoint circuit is shown in Fig. 8(c) and is realized from the pathological circuit shown in Fig. 3(d).

The two ICCII+ circuit realizing the BOTA and shown in Fig. 8(d) is generated from Fig. 3(b) and it is self-adjoint.

For each of the four CCII and ICCII circuits realizing BOTA given in Fig. 8, the parasitic resistances of the two CCII or ICCII act in series with the resistor R connected between two X ports resulting in an actual resistor value R_a equal to $R + 2R_X$.

6. Conclusions

A systematic generation method of TA based on using nullator, norator elements, and pathological mirror elements is used to provide pathological realizations of different types of TA. Four pathological realizations of the single input balanced output TA each using two grounded G are given. Four pathological realizations of the differential input single output TA each using two grounded G are given.

Six pathological realizations of the BOTA are given. Finally, three pathological realizations for each of the two types of the differential input double output TA are also given.

References

1. A. Nedungadi and T. R. Viswanthan, Design of linear CMOS transconductor elements, *IEEE Trans. Circuits Syst.* **31** (1984) 891−894.
2. J. L. Pennock, CMOS triode tranconductor for continuous-time active integrated filters, *Electron. Lett.* **21** (1985) 817−818.
3. Y. Tsividis, Z. Czarnul and S. C. Fang, MOS transconductors and integrators with high linearity, *Electron. Lett.* **22** (1986) 245−246.
4. E. Seevinck and R. F. Wassenaar, A versatile CMOS linear transconductor square-law function circuit, *IEEE J. Solid-State Circuits* **22** (1987) 366−377.
5. Y. T. Wang, F. Lu and A. A. Abidi, A 12.5 MHz CMOS continuous time band pass filter, *IEEE Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers* (1989), pp. 198−199.
6. F. Krummencher and N. Joehl, A 4 MHz CMOS continuous-time filter with on chip automatic tuning, *IEEE J. Solid-State Circuits* **23** (1988) 750−758.
7. S. L. Wong, Novel drain-biased transconductance building blocks for continuous-time active filters, *Electron. Lett.* **25** (1989) 100−101.
8. U. Gatti, F. Maloberti, G. Palmisano and G. Torelli, CMOS triod-transistor transconductor for high-frequency continuous-time filters, *IEE Proc. Circuits Dev. Syst.* **141** (1994) 462−468.
9. E. Sanchez-Sinencio and J. Silva-Martivnez, CMOS trans-conductance amplifiers, architectures and active filters: A tutorial, *IEE Proc. Circuits Dev. Syst.* **147** (2000) 3−12.

10. A. M. Ismail, S. K. El-Meteny and A. M. Soliman, A new family of highly linear transconductors based on the current tail differential pair, *Microelectron. J.* **30** (1999) 753−767.
11. A. A. El-Adawy and A. M. Soliman, A low voltage single input class AB transconductor with rail-to-rail input range, *IEEE Trans. Circuits Syst. I* **47** (2000) 236−242.
12. A. M. Ismail and A. M. Soliman, Novel CMOS linear transconductance element using adaptively biased source-coupled differential pair, *Int. J. Electron. Commun. (AEU)* **54** (2000) 87−92.
13. S. A. Mahmoud and A. M. Soliman, A CMOS programmable balanced output transconductor for analog signal processing, *Int. J. Electron.* **82** (1997) 605−620.
14. S. A. Mahmoud and A. M. Soliman, A new CMOS programmable balanced output transconductor and application to a mixed mode universal filter, *Analog Integr. Circuits Signal Process.* **19** (1999) 241−254.
15. A. M. Soliman, A new active C differential input integrator using the DVCCS/DVCVS, *Int. J. Circuit Theor. Appl.* **7** (1979) 272−275.
16. R. L. Geiger and E. Sanchez-Sinenciio, Active filter design using operational transconductance amplifiers: A tutorial, *IEEE Circuits Dev. Mag.* **1** (1985) 20−32.
17. R. L. Geiger, E. Sanchez-Sinenciio and H. N. Lozano, Generation of continuous time two integrator loop OTA filter structures, *IEEE Trans. Circuits Syst.* **35** (1988) 936−946.
18. P. V. A. Mohan, Generation of OTA-C filter structures from active RC filter structures, *IEEE Trans. Circuits Syst.* **37** (1990) 656−659.
19. J. Mahattanakul and C. Toumazou, Current mode versus voltage mode Gm-C biquad filters: What the theory says, *IEEE Trans. Circuits Syst. II* **45** (1998) 173−186.
20. Y. Tao and J. K. Fidler, Electronically tunable dual-OTA second-order sinusoidal oscillators/filters with non-interacting controls: A systematic synthesis approach, *IEEE Trans. Circuits Syst. I* **47** (2000) 117−129.
21. M. A. Tan and R. Schaumann, Design of a general biquadratic filter section with only transconductances and grounded capacitors, *IEEE Trans. Circuits Syst.* **35** (1988) 478−780.
22. R. Nawrocki and U. Klein, New OTA-capacitor realization of a universal biquad, *Electron. Lett.* **22** (1986) 50−51.
23. N. P. J. Greer, R. K. Henderson, L. Ping and J. I. Sewell, Matrix methods for the design of transconductor ladder filters, *IEE Proc. Circuits Dev. Syst.* **141** (1994) 89−100.
24. R. Schaumann, M. S. Ghausi and K. R. Laker, *Design of Analog Filters Passive, Active RC and Switched Capacitor* (Prentice Hall, New Jersey, 1990).
25. A. Payne and C. Toumazou, Analog amplifiers: Classification and generalization, *IEEE Trans. Circuits Syst. I* **43** (1996) 43−50.
26. C. M. Chang, B. M. Al-Hashimi and J. N. Ross, Unified active filter biquad structures, *IEE Proc. Circuits Dev. Syst.* **151** (2004) 273−277.
27. W. G. Hua, Y. Fukui, K. Kubota and K. Watanabe, Voltage-mode to current-mode conversion by an extended dual transformation, *IEEE Int. Symp. Circuits Syst. ISCAS* **3** (1991) 1833−1836.
28. D. G. Haigh, F. Q. Tan and C. Papavassiliou, Systematic synthesis of active-RC circuit building-blocks, *Analog. Integr. Circuits Signal Process.* **43** (2005) 297−315.
29. L. T. Bruton, *RC Active Circuits Theory and Design* (Prentice Hall, Inc., New Jersey, 1980).
30. S. K. Mitra, *Analysis and Synthesis of Linear Active Networks* (John Wiley, New York, 1969).

31. H. J. Carlin, Singular network elements, *IEEE Trans. Circuit Theory* **11** (1964) 67−72.
32. I. A. Awad and A. M. Soliman, Inverting second-generation current conveyors: The missing building blocks, CMOS realizations and applications, *Int. J. Electron.* **86** (1999) 413−432.
33. I. A. Awad and A. M. Soliman, On the voltage mirrors and the current mirrors, *Analog Integr. Circuits Signal Process.* **32** (2002) 79−81.
34. R. A. Saad and A. M. Soliman, Use of mirror elements in the active device synthesis by admittance matrix expansion, *IEEE Trans. Circuits Syst. I* **55** (2008) 2726−2735.
35. I. A. Awad and A. M. Soliman, A new approach to obtain alternative active building blocks realizations based on their ideal representations, *Frequenz* **54** (2000) 290−299.
36. A. M. Soliman, Synthesis of controlled sources by admittance matrix expansion, *J. Circuits Syst. Comp.* **19** (2010) 597−634.
37. R. A. Saad and A. M. Soliman, A new approach for using the pathological mirror elements in the ideal representation of active devices, *Int. J. Circuit Theory Appl.* **38** (2010) 148−178.
38. A. M. Soliman, Applications of voltage and current unity gain cells in nodal admittance matrix expansion, *IEEE Circuits Syst. Mag.* **9** (2009) 29−42.
39. A. M. Soliman, Adjoint network theorem and floating elements in NAM, *J. Circuits Syst. Comp.* **18** (2009) 597−616.
40. A. S. Sedra and K. C. Smith, A second generation current conveyor and its applications, *IEEE Trans. Circuit Theory* **17** (1970) 132−134.
41. W. M. Snelgrove and A. A. Shoval, A balanced 0.9 μm transconductance C filter tunable over the VHF range, *IEEE J. Solid-State Circuits* **27** (1992) 314−323.