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Generation and classification of CCII and ICCII based negative impedance converter circuits using NAM expansion

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SUMMARY

A new simplified generation method of negative impedance converter circuits (NIC) is introduced. The generation method is based on nodal admittance matrix expansion starting from the input admittance of the NIC circuit terminated by a load rather than treating the NIC as a two-port network element. The four pathological elements, namely nullator, norator, voltage mirror and current mirror, are used in the generation procedure. Two classes of the NIC pathological circuits are defined; each class includes two types. Eight pathological NIC circuits are generated for each class. Two alternative current conveyor and inverting current conveyor-based realizations for each pathological circuit based on alternative pairing of the pathological elements are defined resulting in a total of 16 NIC circuit for each class and a total of 32 NIC circuits. A new NIC-based circuits realizing floating negative impedances are also introduced.

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KEY WORDS: negative impedance converter; pathological VM; pathological CM; nullator; norator; current conveyors; inverting current conveyor

1. INTRODUCTION

An active circuit with the property that the driving-point immittance at one terminal-pair is the negative of the load immittance connected to the other terminal-pair is called a negative-impedance converter (NIC). The NIC is an important sub-network from which active RC filters are synthesized [1–3]. The nullator norator [4] modeling of the NIC leads directly to the corresponding transistor or operational amplifier (Op Amp) NIC circuits and is therefore of significance to the circuit designer.

The generalized NIC is defined by $V_1 = K_V V_2$, $I_1 = K_I I_2$; K_V is the voltage conversion factor and K_I is the current conversion factor. Two special types of NIC exist: the current inversion NIC (CNIC) in which K_V and K_I are both positive, the voltage inversion NIC (VNIC) in which K_V and K_I are both negative.

Five equivalent realizations of CNIC and five equivalent realizations of VNIC circuits using nullators and norators were given in [5].

The first realizations of the CNIC using current conveyors (CC) were given in [6]. The first realization uses CCI which is in fact a CNIC, the second realization uses a CCII+ with Z and Y connected together [6]. These two realizations have unity K_V and K_I.

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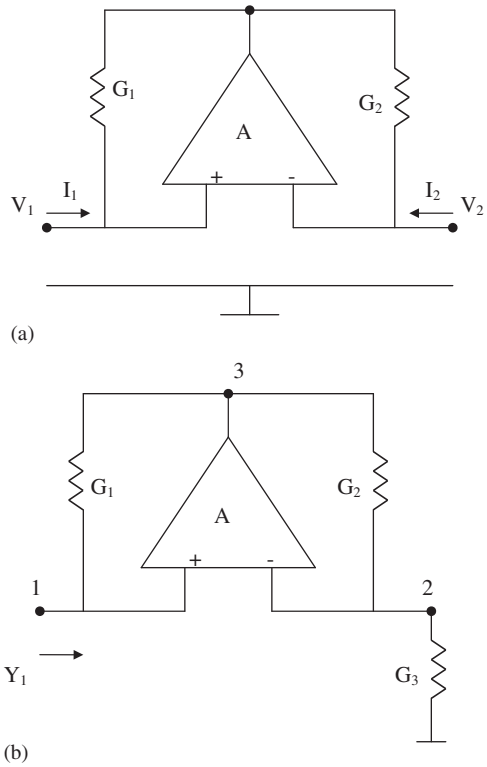

Figure 1. (a) The NIC as a two-port network [1] and (b) the NIC with a load as a one-port network.

Two realizations of the CNIC with controllable K_I and using two CCII+ and two grounded resistors were introduced in [7]. In addition, two realizations of the VNIC with controllable K_V and using two CCII− and two grounded resistors were introduced in [7].

A systematic method of the generation of CNIC based on nodal admittance matrix (NAM) expansion was introduced in [8]. The familiar Op Amp CNIC circuit shown in Figure 1(a) was generated in [8] starting from the expanded NAM of the impedance converter. Stamps for the impedance converters obtained by infinity variable scaling, which are useful in the generation of converter circuits, were given in [9]. The NAM expansion method given in [8, 9] is limited to the use of nullor elements, namely nullators and norators.

Recently, the systematic synthesis method based on NAM expansion and using nullor elements has been extended to accommodate voltage mirror (VM) and current mirror (CM) elements [10–12]. This results in a generalized framework encompassing all pathological elements for the ideal description of active elements [13–16]. Accordingly, more alternative realizations are possible and a wide range of active devices can be used in the generation method. The first part of this paper introduces a new approach for the generation of NIC circuits and results in a 32 NIC circuits. The second part introduces a new circuits realizing floating negative impedances.

2. GENERATION OF CLASS I NIC

Systematic generation method of the CNIC circuits is given next. Two classes of the CNIC circuits are introduced; each class includes two types as discussed next. The generation method introduced in [8] is based on treating the NIC as a two-port network and uses the expanded NAM of the converters given in Tables in [8, 9].

The new approach to be used in this paper for the generation of NIC circuits is based on treating the NIC as a one port by terminating port 2 by a conductance G_3 as shown in Figure 1(b).

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The input admittance is given by:

$$Y = -\frac{G_1 G_3}{G_2} \tag{1}$$

The starting point in the proposed generation method is based on alternative NAM expansions of the above equation. After obtaining the complete pathological realization, the load conductance G_3 is to be removed from the circuit to create port 2 again and have a two-port NIC circuit.

Eight equivalent pathological circuits of Class I NIC are generated. Two alternative types of the Class I NIC circuits are defined next.

2.1. Pathological realizations of class I type A NIC

Successive NAM expansion steps will be applied to Equation (1) with the objective of having G_1, G_2 and G_3 to be moved to diagonal positions in particular it is desirable to move G_3 to the diagonal position 2, 2.

The first step is to apply pivotal expansion to Equation (1) after adding two rows and two columns therefore:

$$Y = \begin{bmatrix} 0 & 0 & -G_1 \\ 0 & 0 & 0 \\ -G_3 & 0 & G_2 \end{bmatrix} \tag{2}$$

Adding a fourth blank row and column and connecting a nullator between nodes 3 and 4 and a CM between nodes 1 and 4 in order to move $-G_1$ to the diagonal position 4, 4 with positive sign; therefore:

$$Y = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ -G_3 & 0 & G_2 & 0 \\ 0 & 0 & 0 & G_1 \end{bmatrix} \tag{3}$$

Next connecting a nullator between nodes 1 and 2 and a CM between nodes 3 and 2 in order to move $-G_3$ to the diagonal position 2, 2 with positive sign; therefore:

$$Y = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & G_3 & 0 & 0 \\ 0 & 0 & G_2 & 0 \\ 0 & 0 & 0 & G_1 \end{bmatrix} \tag{4}$$

The above equation is realized as shown in Figure 2(a).

The second realization starts from Equation (3) and connecting a VM between nodes 1 and 2 and a norator between nodes 3 and 2 in order to move $-G_3$ to the diagonal position 2, 2 with positive sign as follows:

$$Y = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & G_3 & 0 & 0 \\ 0 & 0 & G_2 & 0 \\ 0 & 0 & 0 & G_1 \end{bmatrix} \tag{5}$$

The above equation is realized as shown in Figure 2(b).

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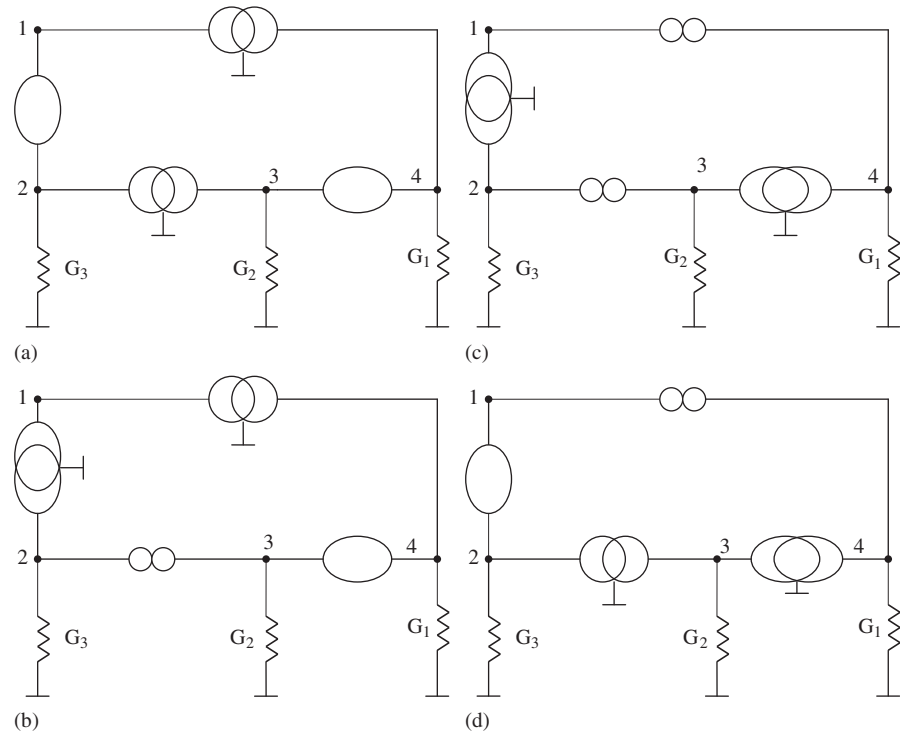

Figure 2. Pathological realizations of class I type A NIC.

The third realization starts from Equation (2) and adding a fourth blank row and column and connecting a VM between nodes 3 and 4 and a norator between nodes 1 and 4 in order to move $-G_1$ to the diagonal position 4, 4 with positive sign; therefore:

$$Y=\begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ -G_3 & 0 & G_2 & 0 \\ 0 & 0 & 0 & G_1 \end{bmatrix} \tag{6}$$

Next connecting a VM between nodes 1 and 2 and a norator between nodes 3 and 2 in order to move $-G_3$ to the diagonal position 2, 2 with positive sign; therefore:

$$Y=\begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & G_3 & 0 & 0 \\ 0 & 0 & G_2 & 0 \\ 0 & 0 & 0 & G_1 \end{bmatrix} \tag{7}$$

The above equation is realized as shown in Figure 2(c).

The fourth realization starts from Equation (6) and connecting a nullator between nodes 1 and 2 and a CM between nodes 3 and 2 in order to move $-G_3$ to the diagonal position 2, 2 with positive sign as follows:

$$Y=\begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & G_3 & 0 & 0 \\ 0 & 0 & G_2 & 0 \\ 0 & 0 & 0 & G_1 \end{bmatrix} \tag{8}$$

The above equation is realized as shown in Figure 2(d).

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2.2. Pathological realizations of class I type B NIC

Adding two rows and two columns to Equation (1) and apply pivotal expansion with opposite signs in the positions 1, 3 and 3, 1 from type A; therefore:

$$Y = \begin{bmatrix} 0 & 0 & G_1 \\ 0 & 0 & 0 \\ G_3 & 0 & G_2 \end{bmatrix} \tag{9}$$

Following successive steps as in type A, the following NAM expansion is obtained as follows:

$$Y = \begin{bmatrix} \overbrace{0 & 0}^{} & \overbrace{0 & 0}^{} \\ 0 & G_3 & 0 & 0 \\ 0 & 0 & G_2 & 0 \\ 0 & 0 & 0 & G_1 \end{bmatrix} \tag{10}$$

The above equation is realized as shown in Figure 3(a) [5]. The second NAM expansion is given by:

$$Y = \begin{bmatrix} \overbrace{0 & 0}^{} & \overbrace{0 & 0}^{} \\ 0 & G_3 & 0 & 0 \\ 0 & 0 & G_2 & 0 \\ 0 & 0 & 0 & G_1 \end{bmatrix} \tag{11}$$

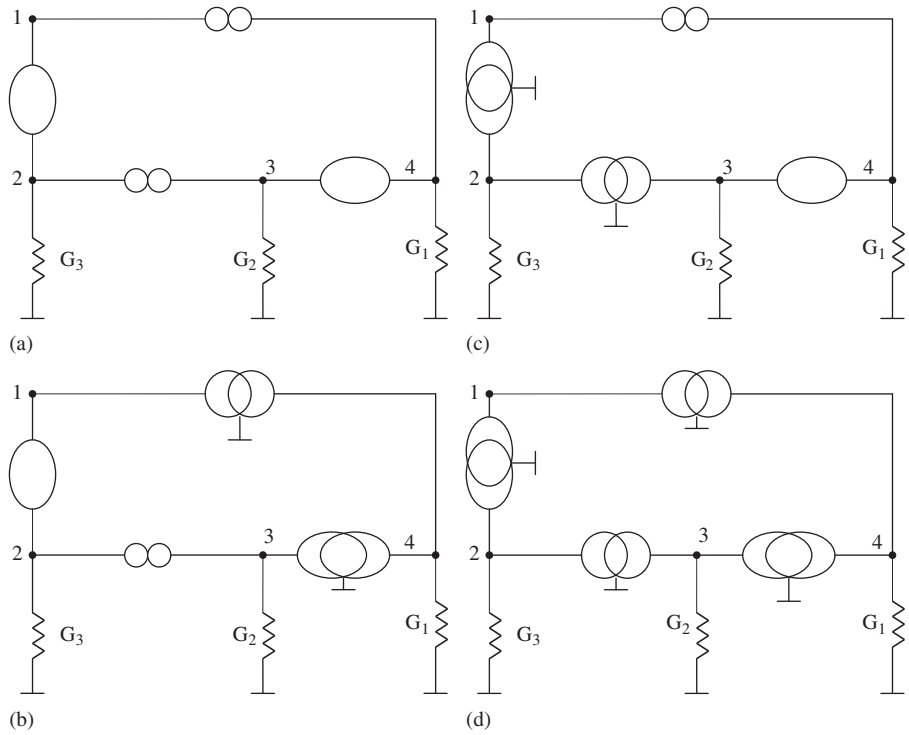

Figure 3. Pathological realizations of class I type B NIC.

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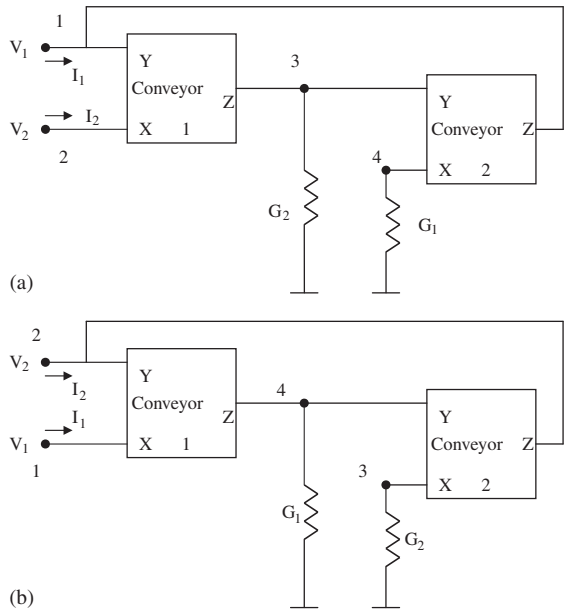

Figure 4. (a) Generalized conveyor realization I of class I NIC and (b) generalized conveyor realization II of class I NIC.

The above equation is realized as shown in Figure 3(b). The third NAM expansion is given by:

$$Y=\begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & G_3 & 0 & 0 \\ 0 & 0 & G_2 & 0 \\ 0 & 0 & 0 & G_1 \end{bmatrix} \tag{12}$$

The above equation is realized as shown in Figure 3(c). The fourth NAM expansion is given by:

$$Y=\begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & G_3 & 0 & 0 \\ 0 & 0 & G_2 & 0 \\ 0 & 0 & 0 & G_1 \end{bmatrix} \tag{13}$$

The above equation is realized as shown in Figure 3(d).

2.3. Converting pathological realizations to CCII and ICCII circuits

The eight generated circuits based on the use of pathological elements and shown in Figures 2 and 3 can lead to the following two realizations of circuits based on alternative pairing of the pathological elements.

Realization I shown in Figure 4(a) includes eight CCII and ICCII circuits obtained from Figures 2 and 3 by taking nodes 1, 2, 3 to represent *Y*, *X* and *Z* terminals of conveyor 1 and nodes 3, 4, 1 to represent *Y*, *X* and *Z* terminals of conveyor 2. Table I includes the description of each of the eight NIC circuits belong to class I realization I.

Realization II shown in Figure 4(b) includes eight CCII and ICCII circuits obtained from Figures 2 and 3 by taking nodes 2, 1, 4 to represent *Y*, *X* and *Z* terminals of conveyor 1 and nodes 4, 3, 2 to represent *Y*, *X* and *Z* terminals of conveyor 2. Table II includes the description of each of the eight NIC circuits belong to class I realization II.

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Table I. Conveyors used in realization I of class I NIC in Figure 4(a).

Type	Conveyor 1	Conveyor 2	Figure	NIC type	Reference
A	CCII+	CCII+	2(a)	CNIC	7
A	ICCII−	CCII+	2(b)	VNIC	New
A	ICCII−	ICCII−	2(c)	VNIC	New
A	CCII+	ICCII−	2(d)	CNIC	New
B	CCII−	CCII−	3(a)	CNIC	5
B	CCII−	ICCII+	3(b)	CNIC	New
B	ICCII+	CCII−	3(c)	VNIC	New
B	ICCII+	ICCII+	3(d)	VNIC	New

Table II. Conveyors used in realization II of class I NIC in Figure 4(b).

Type	Conveyor 1	Conveyor 2	Figure	NIC type	Reference
A	CCII+	CCII+	2(a)	CNIC	7
A	ICCII+	CCII−	2(b)	VNIC	New
A	ICCII−	ICCII−	2(c)	VNIC	New
A	CCII−	ICCII+	2(d)	CNIC	New
B	CCII−	CCII−	3(a)	CNIC	5
B	CCII+	ICCII−	3(b)	CNIC	New
B	ICCII−	CCII+	3(c)	VNIC	New
B	ICCII+	ICCII+	3(d)	VNIC	New

3. GENERATION OF CLASS II NIC

3.1. Pathological realizations of class II type A NIC

Adding two rows and two columns to Equation (1) and apply pivotal expansion; therefore:

$$Y=\begin{bmatrix} 0 & 0 & -G_3 \\ 0 & 0 & 0 \\ -G_1 & 0 & G_2 \end{bmatrix} \tag{14}$$

The above equation is different from Equation (2) in that the elements in the positions 1, 3 and 3, 1 are interchanged.

Following successive steps as in the previous section, the following NAM expansion is obtained as follows:

$$Y=\begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & G_3 & 0 & 0 \\ 0 & 0 & G_2 & 0 \\ 0 & 0 & 0 & G_1 \end{bmatrix} \tag{15}$$

The above equation is realized as shown in Figure 5(a). The second NAM expansion is given by:

$$Y=\begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & G_3 & 0 & 0 \\ 0 & 0 & G_2 & 0 \\ 0 & 0 & 0 & G_1 \end{bmatrix} \tag{16}$$

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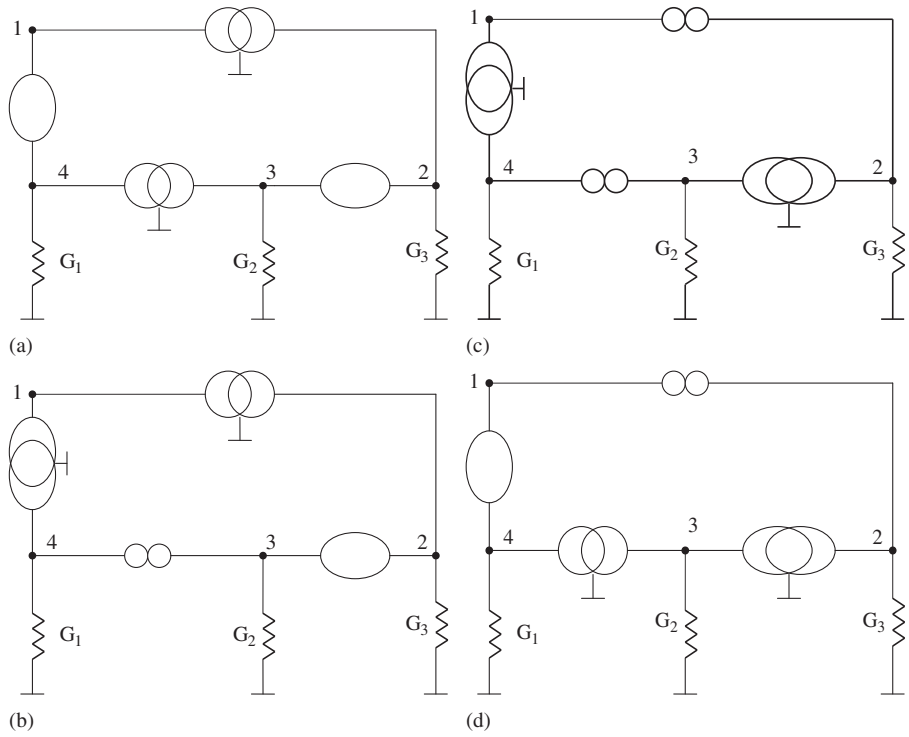

Figure 5. Pathological realizations of class II type A NIC.

The above equation is realized as shown in Figure 5(b). The third NAM expansion is given by:

$$Y=\begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & G_3 & 0 & 0 \\ 0 & 0 & G_2 & 0 \\ 0 & 0 & 0 & G_1 \end{bmatrix} \tag{17}$$

The above equation is realized as shown in Figure 5(c).The fourth NAM expansion is given by:

$$Y=\begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & G_3 & 0 & 0 \\ 0 & 0 & G_2 & 0 \\ 0 & 0 & 0 & G_1 \end{bmatrix} \tag{18}$$

The above equation is realized as shown in Figure 5(d).

3.2. Pathological realizations of class II type B NIC

Adding two rows and two columns to Equation (1) and apply pivotal expansion; therefore: The above equation is different from Equation (14) in that the elements in the positions 1, 3 and 3, 1 are positive.

$$Y=\begin{bmatrix} 0 & 0 & G_3 \\ 0 & 0 & 0 \\ G_1 & 0 & G_2 \end{bmatrix} \tag{19}$$

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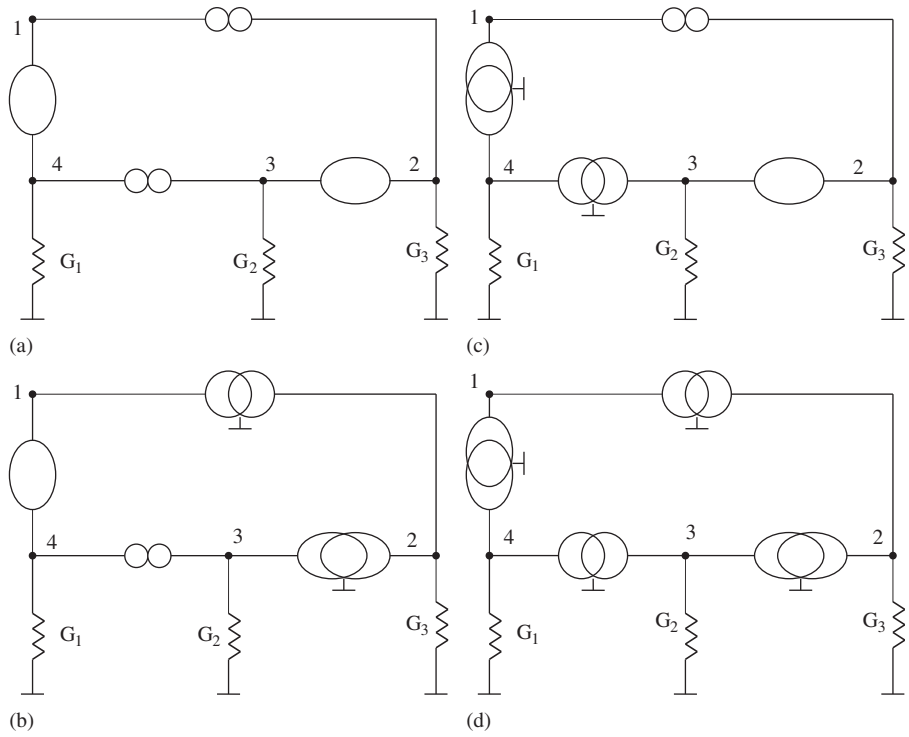

Figure 6. Pathological realizations of class II type B NIC.

Following successive steps as in the previous section, the following NAM expansion is obtained as follows:

$$Y=\begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & G_3 & 0 & 0 \\ 0 & 0 & G_2 & 0 \\ 0 & 0 & 0 & G_1 \end{bmatrix} \tag{20}$$

The above equation is realized as shown in Figure 6(a) [5]. The second NAM expansion is given by:

$$Y=\begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & G_3 & 0 & 0 \\ 0 & 0 & G_2 & 0 \\ 0 & 0 & 0 & G_1 \end{bmatrix} \tag{21}$$

The above equation is realized as shown in Figure 6(b), similarly the realizations in Figures 6(c) and (d) can be obtained.

3.3. Converting pathological realizations to CCII and ICCII circuits

The eight generated circuits based on the use of pathological elements and shown in Figures 5 and 6 can lead to the following two realizations of circuits based on alternative pairing of the pathological elements.

Realization I shown in Figure 7(a) includes eight CCII and ICCII circuits obtained from Figures 5 and 6 by taking nodes 1, 4, 3 to represent Y, X and Z terminals of conveyor 1 and nodes 3, 2, 1 to represent Y, X and Z terminals of conveyor 2. Table III includes the description of each of the eight NIC circuits belong to class II realization I.

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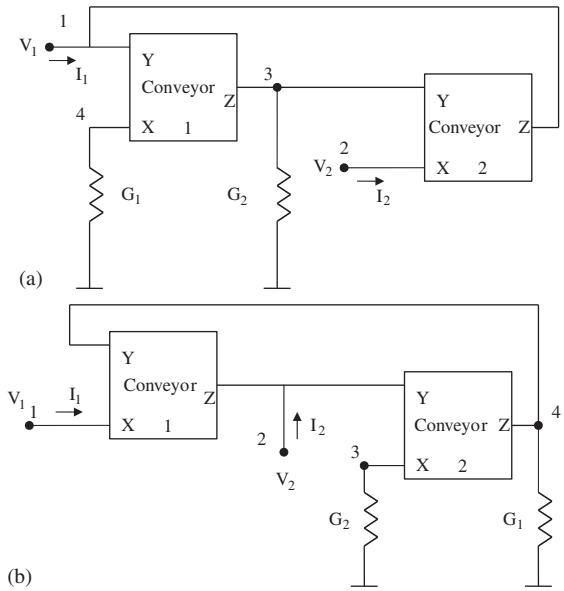

Figure 7. (a) Generalized conveyor realization I of class II NIC and (b) generalized conveyor realization II of class II NIC.

Table III. Conveyors used in realization I of class II NIC in Figure 7(a).

Type	Conveyor 1	Conveyor 2	Figure	NIC type	Reference
A	CCII+	CCII+	5(a)	CNIC	New
A	ICCII−	CCII+	5(b)	CNIC	New
A	ICCII−	ICCII−	5(c)	VNIC	New
A	CCII+	ICCII−	5(d)	VNIC	New
B	CCII−	CCII−	6(a)	VNIC	5,7
B	CCII−	ICCII+	6(b)	CNIC	New
B	ICCII+	CCII−	6(c)	VNIC	New
B	ICCII+	ICCII+	6(d)	CNIC	New

Table IV. Conveyors used in realization II of class II NIC in Figure 7(b).

Type	Conveyor 1	Conveyor 2	Figure	NIC type	Reference
A	CCII+	CCII+	5(a)	CNIC	New
A	ICCII+	CCII−	5(b)	CNIC	New
A	ICCII−	ICCII−	5(c)	VNIC	New
A	CCII−	ICCII+	5(d)	VNIC	New
B	CCII−	CCII−	6(a)	VNIC	5,7
B	CCII+	ICCII−	6(b)	CNIC	New
B	ICCII−	CCII+	6(c)	VNIC	New
B	ICCII+	ICCII+	6(d)	CNIC	New

Realization II shown in Figure 7(b) includes eight CCII and ICCII circuits obtained from Figures 5 and 6 by taking nodes 4, 1, 2 to represent Y, X and Z terminals of conveyor 1 and nodes 2, 3, 4 to represent Y, X and Z terminals of conveyor 2. Table IV includes the description of each of the eight NIC circuits belong to class II realization II.

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4. PARASITIC ELEMENT EFFECTS

A brief evaluation of the NIC circuits based on the parasitic element effects is considered in this section. First the circuit shown in Figure 4(a) is considered.

4.1. Class I NIC circuits

The two parameters that are affecting the conversion factors K_I and K_V of the different NIC class I circuits are R_{X2} and C_{Z1}. In realization I, R_{X2} can be compensated by subtracting its value from the design value of R_1. In realization II, R_{X2} can be compensated by subtracting its value from the design value of R_2.

The effect of C_{Z1} is to modify the conversion factor K_I to be frequency dependant and is given by:

$$K_{Ia} = \pm K_I \frac{1}{1 + s\dfrac{C_{Z1}}{G_2}} \tag{22}$$

The positive sign applies to CNIC and the negative sign applies to VNIC.

The above equation sets the frequency limitation of the class I realization I NIC.

4.2. Class II NIC circuits

The two parameters that are affecting the conversion factors K_I and K_V of the class II realization I NIC circuits are R_{X1} and C_{Z1}. R_{X1} can be compensated by subtracting its value from the design value of R_1. The effect of C_{Z1} is to modify the conversion factor K_V to be frequency dependant and is given by:

$$K_{Va} = \pm K_V \left[1 + s\frac{C_{Z1}}{G_2}\right] \tag{23}$$

The positive sign applies to CNIC and the negative sign applies to VNIC.

The above equation sets the frequency limitation of the realization I class II NIC circuits.

The two parameters that are affecting the conversion factors K_I and K_V of the class II realization II NIC circuits are R_{X2} and C_{Z2}. R_{X2} can be compensated by subtracting its value from the design value of R_2. The effect of C_{Z2} is to modify the conversion factor K_V to be frequency dependant and is given by:

$$K_{Va} = \pm K_V \frac{1}{1 + s\dfrac{C_{Z2}}{G_1}} \tag{24}$$

The positive sign applies to CNIC and the negative sign applies to VNIC.

The above equation sets the frequency limitation of the realization II class II NIC circuits.

5. FLOATING NIC

In this section a brief discussion on the realization of floating negative impedance is given. The circuit shown in Figure 8(a) is based on three stage cascaded connection of two NIC with the positive floating impedance as the intermediate stage. The two terminals of the generated negative impedance are the X ports of the two CCII+ and given in [17].

Figure 8(a) is a similar circuit but with the two terminals of the generated negative impedance are the Y-Z ports of the two CCII+ and given in [17, 18]. Figure 8(c) uses two CCII− with the two terminals of the generated negative impedance are the X ports of the two CCII− and is new. Figure 8(d) also uses two CCII− and reported in [18].

Figure 9 represents four new circuits using two ICCII+ or two ICCII−.

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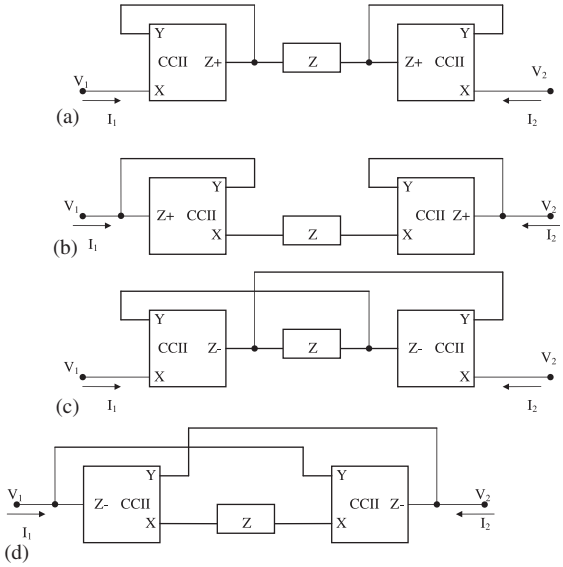

Figure 8. Four alternative floating NIC circuits using two CCII.

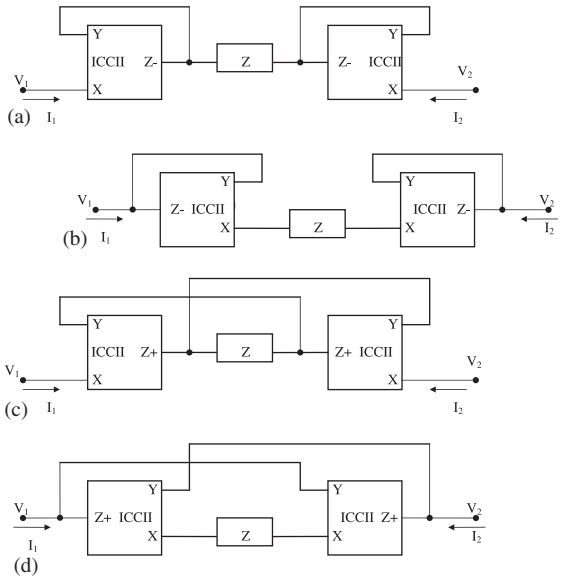

Figure 9. Four alternative floating NIC circuits using two ICCII.

6. CONCLUSIONS

It is well known that there is only one CNIC using a single CCII+ with the $Z+$ terminal connected to Y [6] and there is only one VNIC using a single ICCII− with the $Z-$ terminal connected to Y [19]. It is shown in this paper that there are 16 CNIC circuits using two CCII or ICCII or combination of both and having a controllable conversion factor by varying a grounded resistor. It is also shown in this paper that there are 16 VNIC circuits using two CCII or ICCII or combination of both and having a controllable conversion factor by varying a grounded resistor.

Each of the class I eight CNIC circuits has $K_V = 1$ and $K_I = G_1/G_2$.
Each of the class I eight VNIC circuits has $K_V = -1$ and $K_I = -G_1/G_2$.

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Each of the class II eight CNIC circuits has $K_V = G_2/G_1$ and $K_I = 1$.
Each of the class II eight VNIC circuits has $K_V = -G_2/G_1$ and $K_I = -1$.

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