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Novel CMOS Composite Transistor for Low Voltage Low Power Applications

Ein neuartiger CMOS Composite-Transistor für Anwendungen mit niedriger Versorgungsspannung und kleiner Leistung

Abstract
In this paper, a novel CMOS composite transistor based on a differential pair is proposed. It is shown that the use of the proposed composite transistor offers many advantages and leads to a reduction in the power consumption which makes it suitable to operate in low voltage low power applications. PSpice simulation results are given.

Übersicht
In dieser Arbeit wird ein neuartiger CMOS Composite-Transistor in einer Differentialschaltung vorgeschlagen. Es wird gezeigt, daß der vorgestellte Transistor viele Vorteile bietet. Er führt zu einer Reduzierung des Verlustleistung, dieses macht ihn geeignet für Anwendungen mit niedriger Versorgungsspannung und kleiner Leistung. Die Eigenschaften werden mit PSpice simuliert.

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Für die Dokumentation
CMOS analog circuits / Composite transistor

1. Introduction

Portable equipment is rapidly being made available in this decade. It is natural that the power source for such portable equipment are, in general, batteries. Portable equipment operating at very low voltage is supplied from a single battery cell [1–12]. Nevertheless, considering today's technical trends, the importance and necessity of circuit engineering for very low-voltage operation are continually increasing. Because of economical constraints, the standard CMOS technology is suited in this type of applications. The majority of analog building blocks designed in this technology are exploiting the square law characteristics of the MOS transistor operating in the saturation region [1–9]. In order to obtain a better usage of this squaring characteristics in an easier and more versatile way, the composite transistor proposed in [1, 2] and shown in **Fig. 1** has been introduced. The equation illustrating the I-V characteristics of this composite transistor is given by:

$$I_D = K_{eq}\left(V_G - V_S - V_{Teq}\right)^2 \tag{1}$$

where K_{eq} and V_{Teq} are the equivalent transconductance parameter and threshold voltage for the composite transistor respectively, and are given by:

$$\frac{1}{\sqrt{K_{eq}}} = \frac{1}{\sqrt{K_n}} + \frac{1}{\sqrt{K_p}} \tag{2}$$

$$V_{Teq} = V_{Tn} + |V_{Tp}| \tag{3}$$

where K_n and V_{Tn} are the transconductance parameter and threshold voltage for the NMOS transistor respectively. K_p and V_{Tp} are the transconductance parameter and threshold voltage for the PMOS transistor respectively.

Despite of its desirable two high input impedance feature, this composite transistor has one main drawback in low voltage applications, i.e. a larger threshold voltage as compared to a single MOS transistor as shown by (3) which limits the operating range of the transistor to a small fraction of the total supply voltage range or in worst case prevents the composite transistor from operating. Most recently, some implementations for low voltage composite transistors have been presented [3, 4] as shown in **Fig. 2**. However, these implementations require the use of current sources of high values which increase dramatically the power consumption. In addition, the square law identity is based on an approximation assuming that I_B is much larger than I_D which represents a source of nonlinearity.

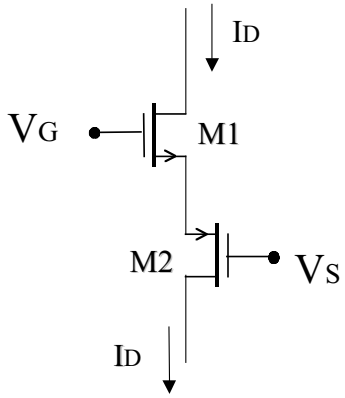

Fig. 1: The composite transistor proposed in [1, 2]

In this paper, a novel composite transistor with a very low threshold voltage and low standby power is presented. It is shown that such architecture gives many additional advantages like insensitivity to transistor threshold voltage variation and immunity to body effect. Finally, as an application, the composite transistor is used in the design of a four-quadrant analog multiplier. Simulation results for both the composite transistor and the analog multiplier are given.

2. Proposed Composite Transistor (CT)

Consider the circuit shown in **Fig. 3**. All the transistors used are operating in the saturation region, where the drain current of the NMOS transistor operating in that region (neglecting the channel length modulation effect) is given by

$$I = \frac{K_n}{2}\left(V_{GS} - V_{Tn}\right)^2 \tag{4}$$

$$K_n = \left(\mu_n C_{ox}\right)\left(\frac{W}{L}\right). \tag{5}$$

Since the transistors M1 and M2 have a common source terminal, i.e.:

$$V_{S1} = V_{S2} \tag{6}$$

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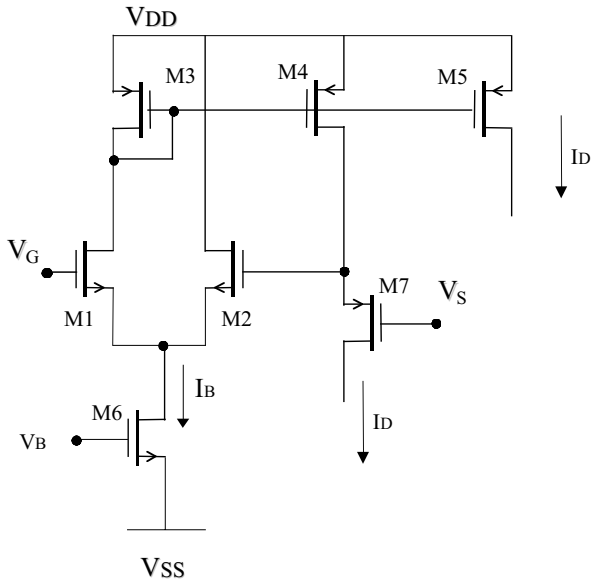

Fig. 2: The low voltage composite transistor proposed in [3, 4]

Therefore, assuming that all body terminals are connected to the proper supply voltages, one obtains:

$$V_G - \sqrt{\frac{2I}{K_{n1}}} - V_{Tn} = V_S - \sqrt{\frac{2(b-1)I}{K_{n2}}} - V_{Tn} \tag{7}$$

where I is the current flowing in transistor M1, b is a constant factor realized by adjusting the aspect ratios of transistors M3 and M4. It is noted that, for proper operation of the circuit:

$$1 < b < 2. \tag{8}$$

From (7), one obtains:

$$I = \frac{1}{2\left(\frac{1}{\sqrt{K_{n1}}} - \sqrt{\frac{b-1}{K_{n2}}}\right)^2}\left(V_G - V_S\right)^2. \tag{9}$$

Consequently, the output current I_D is obtained as:

$$I_D = \frac{b}{2\left(\frac{1}{\sqrt{K_{n1}}} - \sqrt{\frac{b-1}{K_{n2}}}\right)^2}\left(V_G - V_S\right)^2. \tag{10}$$

For the case when M1 and M2 are matched ($K_{n1} = K_{n2} = K_n$), the current I_D is given by

$$I_D = \frac{bK_n}{2\left(1 - \sqrt{b-1}\right)^2}\left(V_G - V_S\right)^2. \tag{11}$$

As seen from (11), the proposed composite transistor (CT) offers square law characteristics insensitive from the value of the threshold voltage of the MOS transistor. Also it is noted that the square law identity is obtained irrespective of the matching between M1 and M2.

In order to prevent the circuit from switching OFF in the case of zero signal ($V_G = V_S$), transistor M9 is added supplying the circuit with a small standby current I_X. This is necessary since, unlike the ordinary MOS transistor and all other previous implementations, the CT is not physically supplied from its adjacent circuitry. Therefore, its biasing must be done inherently. To avoid the violation of the square law identity because of this standby source, M10 is necessarily added to supply a current of I_X as shown in **Fig. 3**.

Consequently, the CT has two modes of operation:

$$\text{For } \left|V_G - V_S\right| < \sqrt{\frac{2I_X}{bK_n}}\left(1 - \sqrt{b-1}\right). \tag{11a}$$

In this range, the output current is not following the square law identity driven before. Therefore, it is undesirable to operate in this region.

$$\text{For } \left|V_G - V_S\right| \geq \sqrt{\frac{2I_X}{bK_n}}\left(1 - \sqrt{b-1}\right). \tag{11b}$$

In this range, the normal operation illustrated by (4) through (11) is valid. The current I_X is chosen to a very small value (0.5 mA throughout the simulations) since it is only needed to keep the transistors ON during startup and signal switching. Consequently, the CT has a very small threshold voltage that can be adjusted

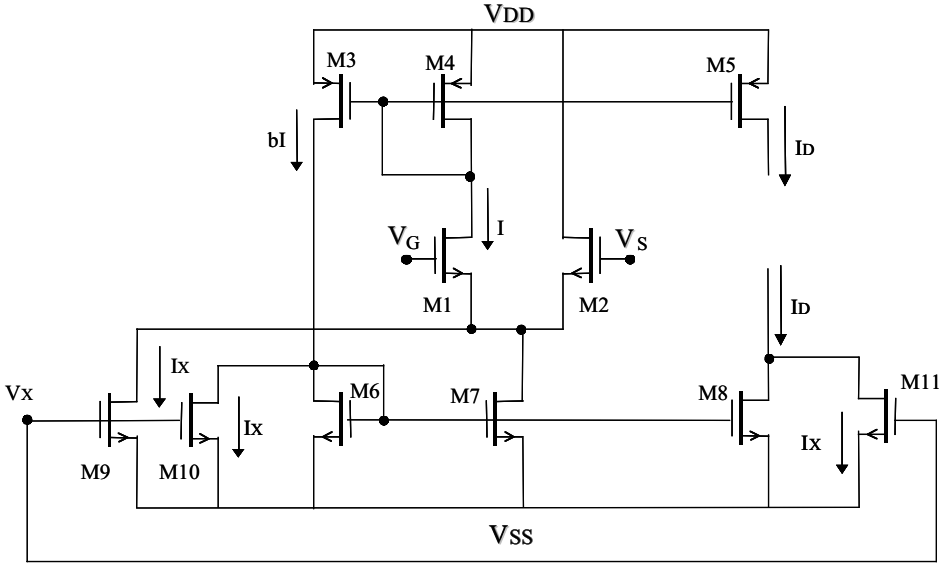

Fig. 3: The proposed composite transistor (CT)

by setting the optimum value of I_X and thus can be adjusted to very small values. As a result, the advantages of CT over previous topologies [1–4] can be summarized as follows:

1. A very small and controllable threshold voltage is obtained.
2. The obtained current is insensitive to the value of the threshold value of the used MOS transistors and hence insensitive to its variation.
3. Unlike the previous low-voltage topologies [3, 4], the standby current sources used can be adjusted to very small values. This reflects remarkably on the power consumption.
4. The CT output current is free from body effect.

In the next sections, the symbolic representation of the CT given in **Fig. 4** will be used to refer for the entire circuit.

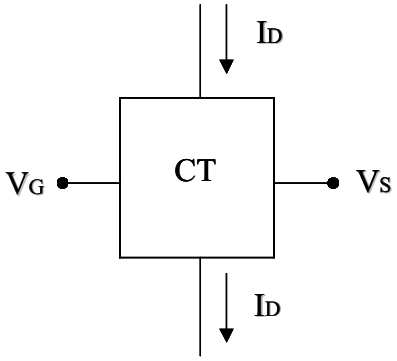

Fig. 4: The symbolic representation for the CT

3. Second Order Effects

The non-idealities represent the basic source of distortion in the implemented applications. One can assume that the transistor channels are enough long to neglect the effect of channel length modulation. Since the transistors M1–M2 have a common source, it is clear that there will not be a contribution of the body-effect in the distortion and as mentionned before, CT performance is independent of variations in the threshold voltage. Consequently, the main source of distortion that needs to be studied carefully is the mobility reduction that results from the vertical surface electric field. Due to this effect, the μ factor in (2) is given by $\mu_n = \mu_o/[1 + \theta(V_{GS} - V_T)]$ where μ_o is the zero field mobility of carriers and θ is a constant. In [1], it has been shown that this effect can be modeled as a source series resistance with value $R_S = \theta/K_n$ as shown in Fig. 4. Following the same analysis carried out in Section II taking R_S into consideration, the result is a third-order harmonic distortion of value:

$$HD_3 = \frac{K_n R_S (2-b)(V_G - V_S)}{\left(1-\sqrt{b-1}\right)^2}. \tag{12}$$

As for the error in the output current due to mismatch between transistors M1 and M2, one represents this mismatch by an equivalent error in the transconductance parameter ΔK_n. The relative error in the output current ($\Delta I_O/I_O$) due to ΔK_n is given by:

$$\frac{\Delta I_O}{I_O} = \frac{\sqrt{K_n + \Delta K_n}\left(1-\sqrt{b-1}\right)}{\sqrt{K_n + \Delta K_n} - \sqrt{K_n (b-1)}}. \tag{13}$$

It is clear that this mismatch does not introduce distortion in the circuit since the square law identity is irrespective of the matching between M1 and M2 as shown in the previous section.

4. Four Quadrant Analog Multiplier

Squaring circuits have been widely used for the design of multipliers in the literature [6–9]. Therefore, the four-quadrant multiplier is an excellent application for the CT. In order to obtain a four-quadrant multiplier circuit for two differential inputs, a four-transistor cell was introduced in [6]. The circuit is shown in **Fig. 5** after substituting every transistor by a CT. In addition to all the advantages mentionned before, the body effect which is one of the main sources of distortion in this circuit is cancelled directly by this one-to-one substitution. Assuming that all the CT cells are matched, the output current I_O is hence given by:

$$I_O = \frac{bK_n}{\left(1-\sqrt{b-1}\right)^2}(V_A - V_B)(V_2 - V_1). \tag{14}$$

The performance of this circuit will be shown in the next section through simulations.

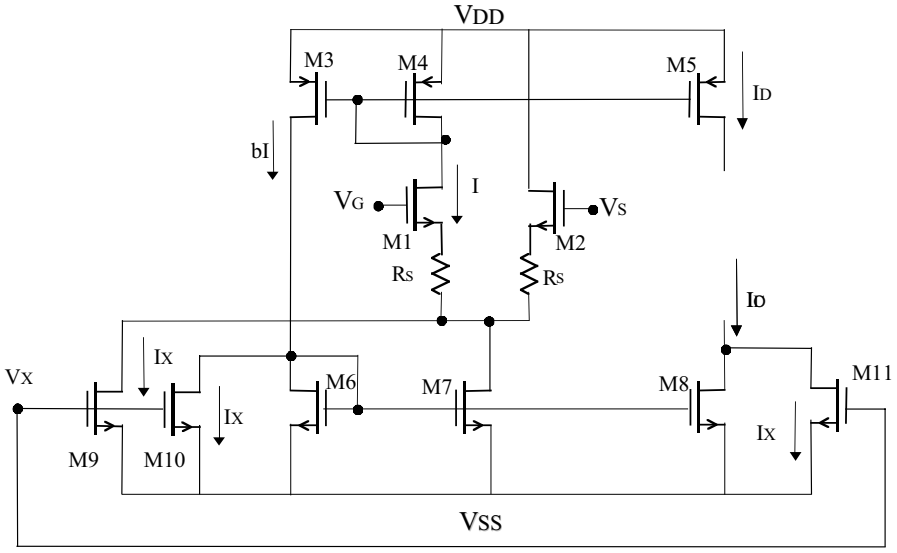

Fig. 5: The analog four-quadrant multiplier circuit using CT cells

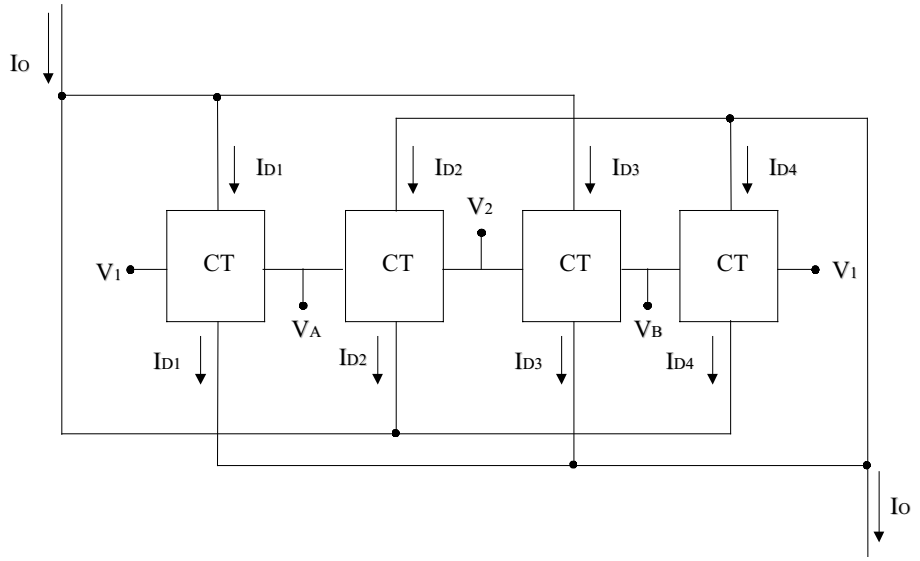

Fig. 6: The equivalent circuit of the CT taking in consideration the effect of mobility reduction

5. PSpice Simulations

Performance of the CT shown in Fig. 3 and the multiplier circuit are simulated using PSpice. Transistors aspect ratios are given in **Table 1** and 0.5 mm CMOS MIETIC process is assumed. Supply voltages are $V_{DD} = -V_{SS} = 1.5$ V.

Table 1: The aspect ratios of the transistors used in Fig. 3

Transistor	Aspect Ratio
M1,M2	1/1
M4	15/4
M3,M5	15/3.5
M6,M7,M8	15/1.5
M9,M10,M11	0.5/3

Fig. 7 shows the output current I_D of the CT versus (V_G - V_S) which is scanned from 0 V to 2.5 V. Simulation results confirm the validity of (11).

Fig. 8 shows the output current I_O for the four-quadrant multiplier shown in Fig. 5 versus (V_1 - V_2) which is scanned from -0.8 V to 0.8 V for different values of (V_A - V_B). It has been found that for an input of 1 V_{p-p}, the THD was less than 0.6 % at 100 kHz. **Fig. 9** represents the simulated output current of the multiplier circuit resulting from the multiplication of two fully differential input voltages of 10 MHz (sinusoidal) and 500 kHz (triangular) respectively. **Fig. 10** represents the frequency response of the four-quadrant multiplier circuit that shows that the 3-dB frequency is about 147 MHz.

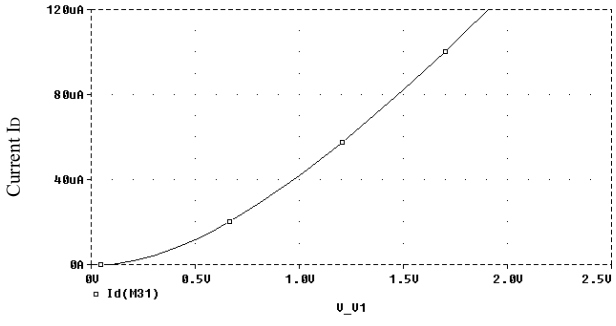

Fig. 7: The I-V characteristics for the composite transistor

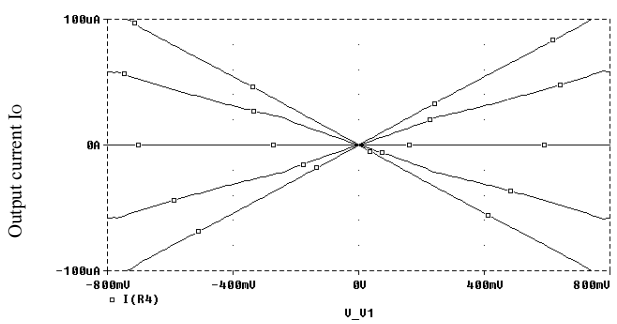

Fig. 8: The I-V characteristics for the four-quadrant multiplier circuit

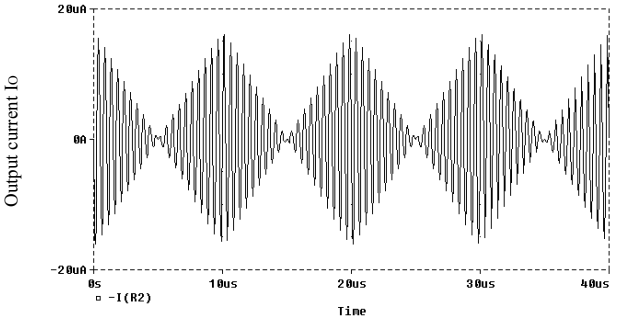

Fig. 9: The transient response of the output current of the multiplier circuit resulting from the multiplication of two differential input voltages

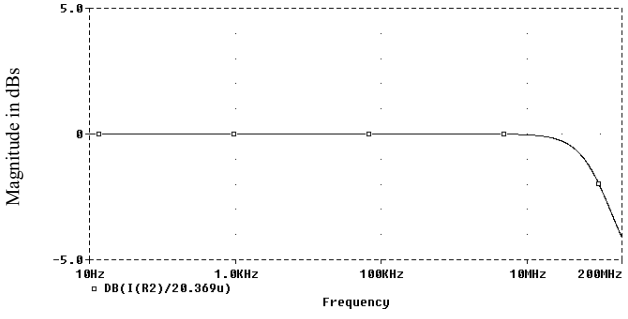

Fig. 10: The frequency characteristics for the four-quadrant multiplier circuit

6. Conclusion

A new composite transistor based on the LTP has been proposed. The advantages of this new composite transistor over previous topologies have been discussed. Also as an application, a four-quadrant analog multiplier was presented. Simulation results confirm the analysis, which makes this new composite transistor very suitable for many applications in analog signal processing.

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