INTERNATIONAL JOURNAL OF CIRCUIT THEORY AND APPLICATIONS
Int. J. Circ. Theor. Appl. 2011; **39**:697–717
Published online 22 March 2010 in Wiley Online Library (wileyonlinelibrary.com). DOI: 10.1002/cta.654

Generation of Kerwin-Huelsman-Newcomb biquad filter circuits using nodal admittance matrix expansion

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SUMMARY

Nodal admittance matrix (NAM) expansion is used to generate a family of grounded passive component Kerwin Huelsman Newcomb (KHN) circuits. The generated KHN circuits have independent control on the selectivity factor and the radian frequency as in the original KHN, besides they have independent control on the gain, which is not achievable in the original KHN circuit. The NAM expansion is based on using nullor elements and voltage mirror and current mirror as well. Two types of the KHN circuit are considered, each includes four classes. For each class it is found that there are 32 different KHN circuit; therefore, there is a total of 128 circuits that belong to type-A KHN and a similar number for type-B KHN circuits. Simulation results are included to support the generation method. Copyright © 2010 John Wiley & Sons, Ltd.

Received 23 April 2009; Revised 19 August 2009; Accepted 6 September 2009

KEY WORDS: universal filters; KHN circuit; nodal admittance matrix expansions; pathological elements

1. INTRODUCTION

The state variable filter known in the literature as the Kerwin Huelsman Newcomb (KHN) filter [1] is a basic building block in many analog signal processing applications. It provides simultaneously the three basic filtering functions namely the high-pass (HP), band-pass (BP) and low-pass (LP) responses at three different outputs. The circuit uses three operational amplifiers (Op Amps) as shown in Figure 1(a). The input voltage is applied to the non-inverting input terminal of the op amp as shown in Figure 1(a) and this is defined as KHN of type A. It is also possible to apply the input voltage to the inverting Op Amp terminal resulting in the inverted KHN filter shown in Figure 1(b) [2] and this is defined as KHN of type-B. Both KHN and the inverted KHN filters belong to the two integrator loop class of filters and they have independent control on the selectivity factor Q and the radian frequency ω_O. There is however no independent control on the gain. Such filters suffer from the finite gain bandwidth of the Op Amp, which results in a pole Q enhancement thus limiting the frequency of operation of the filter. The finite gain bandwidth effect on the filter performance has been studied [3] and methods of active compensation have been developed to improve the circuit operation [4].

Several realizations of the KHN circuit using current conveyor (CCII) [5] or the inverting current conveyor (ICCII) [6] or the differential voltage current conveyor [7, 8] have been introduced in the literature [9–12].

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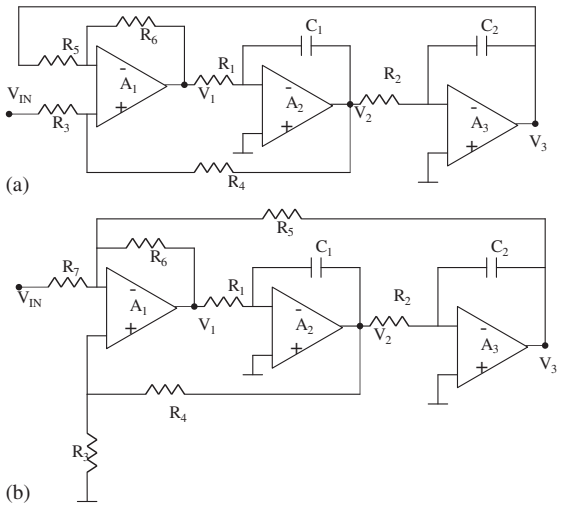

Figure 1. (a) Type A KHN circuit using three Op Amps [1]. (b) Type B inverted KHN circuit using three Op Amps [2].

In this paper new generation methods of CCII- and ICCII-based KHN family of circuits using nodal admittance matrix (NAM) expansion is introduced.

2. PATHOLOGICAL ELEMENTS

Before considering the NAM expansion to obtain the desirable KHN family of circuits, it may be useful to review briefly the four pathological elements that will be used.

The nullor elements are the nullators and norators shown in Figures 2(a), (b). The nullator and norator [13–16] are pathological elements that possess ideal characteristics and are specified according to the constraints they impose on their terminal voltages and currents. For the nullator, $V = I = 0$, while the norator imposes no constraints on its voltage and current.

Additional pathological elements called mirror elements shown in Figures 2(c), (d) were introduced in [6] to describe the voltage and current reversing actions. The VM is a lossless two-port network element used to represent an ideal voltage reversing action and it is described by:

$$V_1 = -V_2 \tag{1a}$$

$$I_1 = I_2 = 0 \tag{1b}$$

The CM is a two-port network element used to represent an ideal current reversing action and it is described by:

$$V_1 \quad \text{and} \quad V_2 \text{ are arbitrary} \tag{2a}$$

$$I_1 = I_2 \quad \text{and they are also arbitrary} \tag{2b}$$

Although the CM element shown in Figure 2(d) has the same symbol as the regular CM, it is a bi-directional element and has a theoretical existence.

Very recently, the systematic synthesis method based on NAM expansion using nullor elements [17–19] has been extended to accommodate mirror elements [20–22]. This results in a generalized framework encompassing all pathological elements for ideal description of active elements. Accordingly, more alternative realizations are possible and a wide range of active devices can be used in the synthesis.

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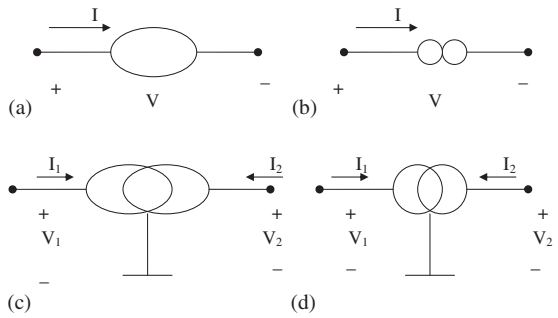

Figure 2. The pathological elements: (a) nullator; (b) norator; (c) voltage mirror (VM); and (d) current mirror (CM).

It should be noted that after the synthesis procedure is completed, the pathological elements are paired to realize the proper CCII or ICCII as follows:

The nullator and norator with a common terminal realize a CCII−.
The nullator and CM with a common terminal realize a CCII+.
The VM and norator with a common terminal realize an ICCII−.
The VM and CM with a common terminal realize an ICCII+.

3. NAM DESCRIPTION OF TWO TYPES OF KHN CIRCUITS

In this section the NAM equations of the two types of KHN circuits defined as types A and B and are generated from the Op Amp KHN circuits of Figures 1(a), (b) respectively.

Since there are four independent node voltages, the NAM equation will be of dimension four.

The first inverting integrator equation is written in the following form:

$$G_1 V_1 + sC_1 V_2 = 0 \tag{3}$$

In Figure 1(a), the capacitor C_1 is connected between node 2 and virtual ground.

It is desirable to have this capacitor as a grounded capacitor connected to node 2; therefore, the above equation will appear as the second row in the Y matrix equation with the term sC_1 as a diagonal element in the position 2, 2.

The second inverting integrator equation is written in the following form:

$$G_2 V_2 + sC_2 V_3 = 0 \tag{4}$$

Similarly, the capacitor C_2 is connected between node 3 and virtual ground and it is desirable to have this capacitor as a grounded capacitor connected to node 3; therefore, the above equation will appear as the third row in the Y matrix equation.

The summer stage of the KHN circuits relates the four voltages by multiplying factors of resistors ratios. Since the interest is in the generation of grounded passive elements circuit, the summer stage equation will be written as a current equation with different conductance coefficients maintaining the polarity relations between the four voltages.

Since it is desirable to have a very high input impedance KHN circuit, the V_{IN} of Figure 1(a) will be defined as V_4 in the summer stage equation as follows:

$$-G_6 V_1 + G_4 V_2 - G_5 V_3 + G_3 V_4 = 0 \tag{5}$$

Equation (5) is the proposed new equation maintaining the same sign coefficients as in the summer stage of the circuit of Figure 1(a). The interest is in the generation of grounded passive element KHN circuits with infinite input impedance.

DOI: 10.1002/cta

Table I. Circuit equations of the three stages of the type A -KHN.

Class	Summer stage	Integrator 1	Integrator 2
I	$-G_6V_1+G_4V_2-G_5V_3+G_3V_4=0$	$G_1V_1+sC_1V_2=0$	$G_2V_2+sC_2V_3=0$
II	$-G_6V_1-G_4V_2-G_5V_3+G_3V_4=0$	$G_1V_1-sC_1V_2=0$	$G_2V_2-sC_2V_3=0$
III	$G_6V_1-G_4V_2-G_5V_3+G_3V_4=0$	$G_1V_1+sC_1V_2=0$	$G_2V_2-sC_2V_3=0$
IV	$G_6V_1+G_4V_2-G_5V_3+G_3V_4=0$	$G_1V_1-sC_1V_2=0$	$G_2V_2+sC_2V_3=0$

Table II. The admittance matrix of the type A- KHN circuit.

Class	Admittance matrix Y	Polarity HP	Polarity BP	Polarity LP
I	$Y=\begin{bmatrix}0 & 0 & 0 & 0\\ G_1 & sC_1 & 0 & 0\\ 0 & G_2 & sC_2 & 0\\ -G_6 & G_4 & -G_5 & G_3\end{bmatrix}$	+	−	+
II	$Y=\begin{bmatrix}0 & 0 & 0 & 0\\ -G_1 & sC_1 & 0 & 0\\ 0 & -G_2 & sC_2 & 0\\ -G_6 & -G_4 & -G_5 & G_3\end{bmatrix}$	+	+	+
III	$Y=\begin{bmatrix}0 & 0 & 0 & 0\\ G_1 & sC_1 & 0 & 0\\ 0 & -G_2 & sC_2 & 0\\ G_6 & -G_4 & -G_5 & G_3\end{bmatrix}$	−	+	+
IV	$Y=\begin{bmatrix}0 & 0 & 0 & 0\\ -G_1 & sC_1 & 0 & 0\\ 0 & G_2 & sC_2 & 0\\ G_6 & G_4 & -G_5 & G_3\end{bmatrix}$	−	−	+

Table III. Circuit equations of the three stages of the type B-KHN.

Class	Summer stage	Integrator 1	Integrator 2
I	$G_6V_1-G_4V_2+G_5V_3+G_3V_4=0$	$G_1V_1+sC_1V_2=0$	$G_2V_2+sC_2V_3=0$
II	$G_6V_1+G_4V_2+G_5V_3+G_3V_4=0$	$G_1V_1-sC_1V_2=0$	$G_2V_2-sC_2V_3=0$
III	$-G_6V_1+G_4V_2+G_5V_3+G_3V_4=0$	$G_1V_1+sC_1V_2=0$	$G_2V_2-sC_2V_3=0$
IV	$-G_6V_1-G_4V_2+G_5V_3+G_3V_4=0$	$G_1V_1-sC_1V_2=0$	$G_2V_2+sC_2V_3=0$

The fourth row in Table I includes the above equation of the desirable KHN circuit related to Figure 1(a) with same signs. As classified before in [12] the circuit equations of the other three classes of Type A are also given in Table I.

In class II the two integrators are both non-inverting, whereas in class III the first integrator is inverting and the second integrator is non-inverting. In class IV, the first integrator is non-inverting and the second integrator is inverting.

The NAM equations of the four classes of type A-KHN circuit together with the signs of the three different output voltages are given in Table II.

DOI: 10.1002/cta

Table IV. The admittance matrix of the type B-KHN circuits.

Class	Admittance matrix Y	Polarity HP	Polarity BP	Polarity LP
I	$Y=\begin{bmatrix} 0 & 0 & 0 & 0 \\ G_1 & sC_1 & 0 & 0 \\ 0 & G_2 & sC_2 & 0 \\ G_6 & -G_4 & G_5 & G_3 \end{bmatrix}$	−	+	−
II	$Y=\begin{bmatrix} 0 & 0 & 0 & 0 \\ -G_1 & sC_1 & 0 & 0 \\ 0 & -G_2 & sC_2 & 0 \\ G_6 & G_4 & G_5 & G_3 \end{bmatrix}$	−	−	−
III	$Y=\begin{bmatrix} 0 & 0 & 0 & 0 \\ G_1 & sC_1 & 0 & 0 \\ 0 & -G_2 & sC_2 & 0 \\ -G_6 & G_4 & G_5 & G_3 \end{bmatrix}$	+	−	−
IV	$Y=\begin{bmatrix} 0 & 0 & 0 & 0 \\ -G_1 & sC_1 & 0 & 0 \\ 0 & G_2 & sC_2 & 0 \\ -G_6 & -G_4 & G_5 & G_3 \end{bmatrix}$	+	+	−

For the type B class I circuit, which is obtained from the inverted KHN circuit of Figure 1(b), the circuit equations are given in Table III, which also includes the other three classes of type B-KHN circuit. The NAM equations of the four classes of type B-KHN circuit together with the signs of the three different output voltages are given in Table IV.

4. GENERATION OF TYPE A-KHN CIRCUITS BY NAM EXPANSION

The generation of the four classes of the type A-KHN circuits is considered in this section. To limit the paper length, only one circuit for each class will be given in this section. Additional circuits will be given in Section 7. The straight brackets used are for nullators and norators as was introduced in [17–19]. The curved brackets are for a VM and a CM as was used in [20–22].

4.1. Generation of class-I

The Y matrix of type A class I KHN circuit is given by:

$$Y=\begin{bmatrix} 0 & 0 & 0 & 0 \\ G_1 & sC_1 & 0 & 0 \\ 0 & G_2 & sC_2 & 0 \\ -G_6 & G_4 & -G_5 & G_3 \end{bmatrix} \tag{6}$$

The diagonal elements are realizable by grounded capacitors C_1 and C_2 at nodes 2 and 3 and a grounded conductance G_3 at node 4. The two minus signs in the positions 4, 1 and 4, 3 indicates that the use of nullators and norators only cannot provide a practical realization with grounded

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passive elements. This illustrates the importance of the mirror elements [12] in achieving NAM expansion and obtaining physically realizable grounded passive element KHN circuits.

A blank fifth row and column are added to Equation (6) and then a nullator is connected between nodes 1 and 5 to move G_1 to the fifth column.

$$Y = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & sC_1 & 0 & 0 & G_1 \\ 0 & G_2 & sC_2 & 0 & 0 \\ -G_6 & G_4 & -G_5 & G_3 & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix} \tag{7}$$

A norator is connected between nodes 2 and 5 to move G_1 to the diagonal position 5, 5.

$$Y = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & sC_1 & 0 & 0 & 0 \\ 0 & G_2 & sC_2 & 0 & 0 \\ -G_6 & G_4 & -G_5 & G_3 & 0 \\ 0 & 0 & 0 & 0 & G_1 \end{bmatrix} \tag{8}$$

A blank six- row and column are added to Equation (8) and then a nullator is connected between nodes 2 and 6 to move G_2 to column six.

$$Y = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & sC_1 & 0 & 0 & 0 & 0 \\ 0 & 0 & sC_2 & 0 & 0 & G_2 \\ -G_6 & G_4 & -G_5 & G_3 & 0 & 0 \\ 0 & 0 & 0 & 0 & G_1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \tag{9}$$

A second norator is connected between nodes 3 and 6 to move G_2 to the diagonal position 6, 6.

$$Y = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & sC_1 & 0 & 0 & 0 & 0 \\ 0 & 0 & sC_2 & 0 & 0 & 0 \\ -G_6 & G_4 & -G_5 & G_3 & 0 & 0 \\ 0 & 0 & 0 & 0 & G_1 & 0 \\ 0 & 0 & 0 & 0 & 0 & G_2 \end{bmatrix} \tag{10}$$

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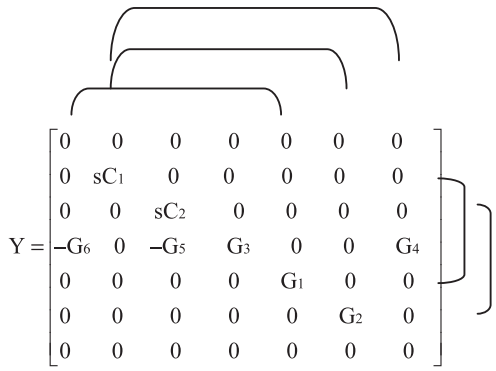
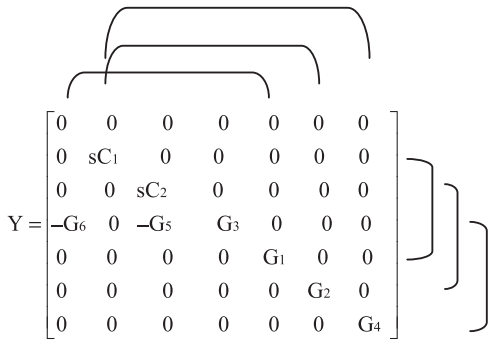
A blank seventh-row and column are added to Equation (10) and then a nullator is connected between nodes 2 and 7 to move G_4 to column seven.



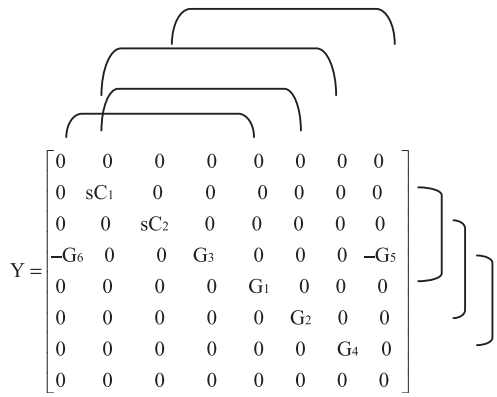
$$Y = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & sC_1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & sC_2 & 0 & 0 & 0 & 0 \\ -G_6 & 0 & -G_5 & G_3 & 0 & 0 & G_4 \\ 0 & 0 & 0 & 0 & G_1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & G_2 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \tag{11}$$

A third norator is connected between nodes 4 and 7 to move G_4 to the diagonal position 7, 7.



$$Y = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & sC_1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & sC_2 & 0 & 0 & 0 & 0 \\ -G_6 & 0 & -G_5 & G_3 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & G_1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & G_2 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & G_4 \end{bmatrix} \tag{12}$$

A blank eighth-row and column are added to Equation (12) and then a nullator is connected between nodes 3 and 8 to move $-G_5$ to column eight as follows:



$$Y = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & sC_1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & sC_2 & 0 & 0 & 0 & 0 & 0 \\ -G_6 & 0 & 0 & G_3 & 0 & 0 & 0 & -G_5 \\ 0 & 0 & 0 & 0 & G_1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & G_2 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & G_4 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \tag{13}$$

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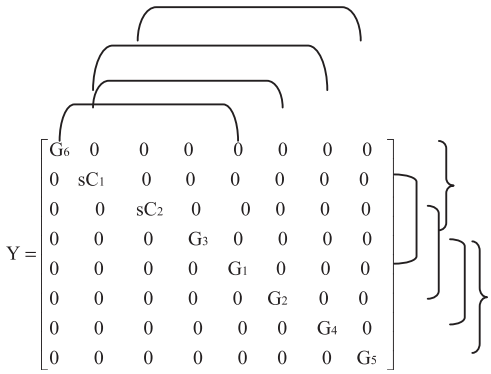
A CM is connected between nodes 4 and 8 to move $-G_5$ to be G_5 at the diagonal position 8, 8. A second CM is also connected between nodes 4 and 1 to move $-G_6$ to be G_6 at the position 1, 1 as follows:



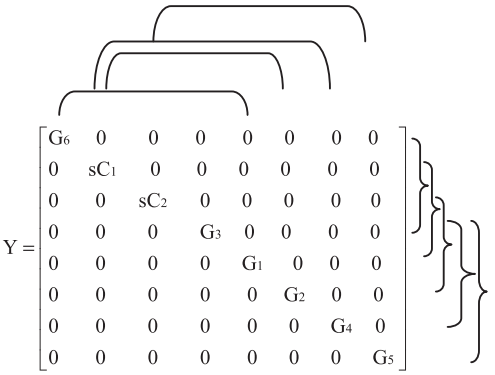
$$Y = \begin{bmatrix} G_6 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & sC_1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & sC_2 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & G_3 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & G_1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & G_2 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & G_4 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & G_5 \end{bmatrix} \tag{14}$$

The above equation is realizable by four nullators, three norators and two CM as shown in Figure 3(a). For a physically realizable circuit it is necessary to have one more nullator so that the number of nullators equal to the number of norators plus number of CM [6]. To achieve the desirable very high input impedance, a nullator is added between node 4 (which is the input node in the original KHN) and the new input node 9. The technique of expanding a node to two nodes by adding a nullator is well known and was used before in [23].

4.2. Generation of class-II

The *Y* matrix of type A-class II KHN circuit is given in Table I.

The *Y* matrix can be expanded to an 8×8 matrix with diagonal elements by successive additions of pathological elements to obtain the desirable NAM given by:



$$Y = \begin{bmatrix} G_6 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & sC_1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & sC_2 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & G_3 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & G_1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & G_2 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & G_4 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & G_5 \end{bmatrix} \tag{15}$$

The above equation is realizable by four nullators and five CM as shown in Figure 3(b). For a physically realizable circuit it is necessary to have one more nullator so that the number of nullators equal to the number of CM [6]. To achieve the desirable very high input impedance, a nullator is added between node 4 and the new input node 9. The circuit in this case is realizable using five, CCII+.

4.3. Generation of classes III and IV

The *Y* matrix of type A-class III and class IV KHN circuits are given in Table I.

Following similar NAM expansion steps as in the previous sections the final *Y* matrix is obtained.

A class III circuit is shown in Figure 3(c) and is realizable using three CCII+ and two CCII−.

A class IV circuit is shown in Figure 3(d) and is realizable using two CCII+ and three CCII−.

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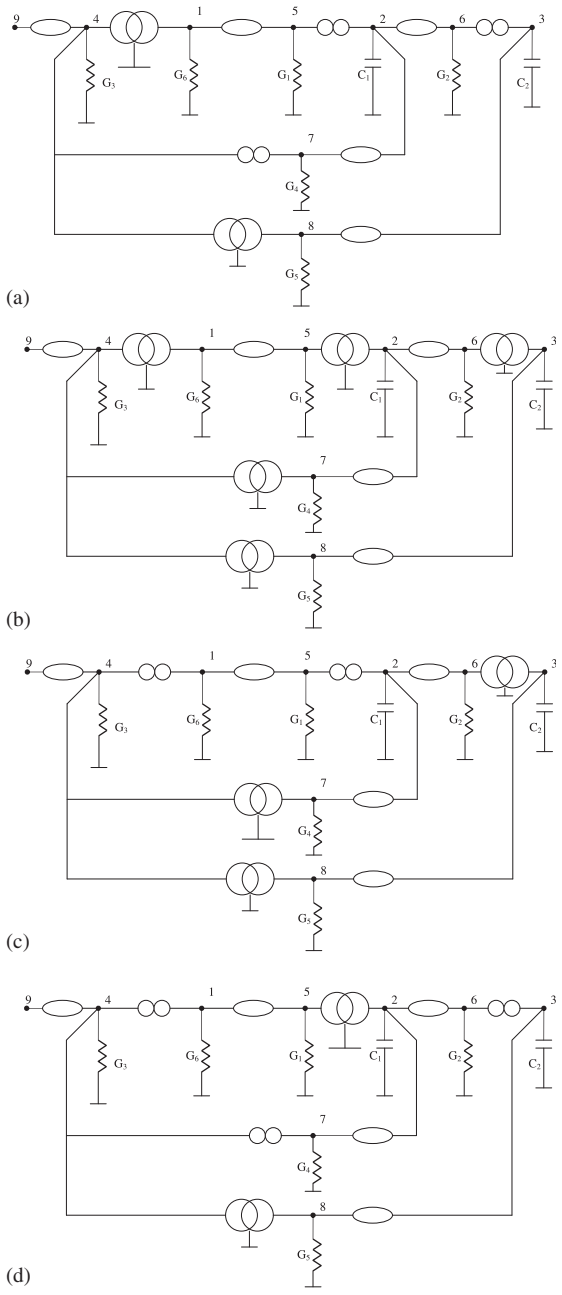

Figure 3. (a) Realization of a KHN circuit type A-class I; (b) realization of a KHN circuit type A-class II; (c) realization of a KHN circuit type A-class III; and (d) realization of a KHN circuit type A-class IV.

5. GENERATION OF TYPE B-KHN CIRCUITS BY NAM EXPANSION

The generation of the four classes of the type B-KHN circuit is considered in this section. To limit the paper length only one equation for one class-B type 1 circuit will be given and the other three classes are discussed very briefly in this section. Additional interesting circuits will be given in Section 7.

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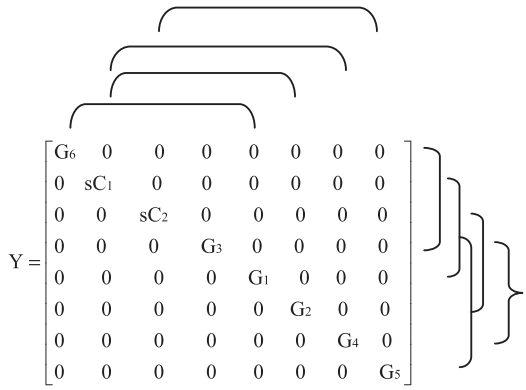
5.1. Generation of class-I

The Y matrix of type B-class I KHN circuit is given by:

$$Y = \begin{bmatrix} 0 & 0 & 0 & 0 \\ G_1 & sC_1 & 0 & 0 \\ 0 & G_2 & sC_2 & 0 \\ G_6 & -G_4 & G_5 & G_3 \end{bmatrix} \tag{16}$$

The diagonal elements are realizable by grounded capacitors C_1 and C_2 at nodes 2 and 3 respectively and a grounded conductance G_3 at node 4. The minus sign in the positions 4, 2 indicates that the use of nullators and norators only cannot provide a practical realization with grounded passive elements.

Following similar steps as in the previous sections, the desirable NAM is obtained as:



$$Y = \begin{bmatrix} G_6 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & sC_1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & sC_2 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & G_3 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & G_1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & G_2 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & G_4 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & G_5 \end{bmatrix} \tag{17}$$

To achieve the desirable very high input impedance, a nullator is added between node 4 and the new input node 9. The circuit in this case is realizable using one CCII+ and four CCII−.

5.2. Generation of classes-II, III and IV

The Y matrix of type B-class II KHN circuit is given in the second row of Table IV.

Following similar steps as in the previous sections

The class II circuit is shown in Figure 4(b) and is realizable using two, CCII+ and three CCII−.

The Y matrix of type B-class III KHN circuit is given in the third row of Table IV. Following similar steps as in the previous sections

The class III circuit is shown in Figure 4(c) and is realizable using, two CCII+ and three CCII−.

The Y matrix of type B-class IV KHN circuit is given in the fourth row of Table IV. Following similar steps as in the previous sections

The class IV circuit is shown in Figure 4(d) and is realizable using three CCII+ and two CCII−.

6. DESIGN EQUATIONS FOR KHN CIRCUIT

The realizations given in the previous sections include one circuit for each class realizable by five CCII with different Z polarities [10]. The circuit shown in Figure 5 represents a practical circuit realization of the type A-class II given in Figure 3(b).

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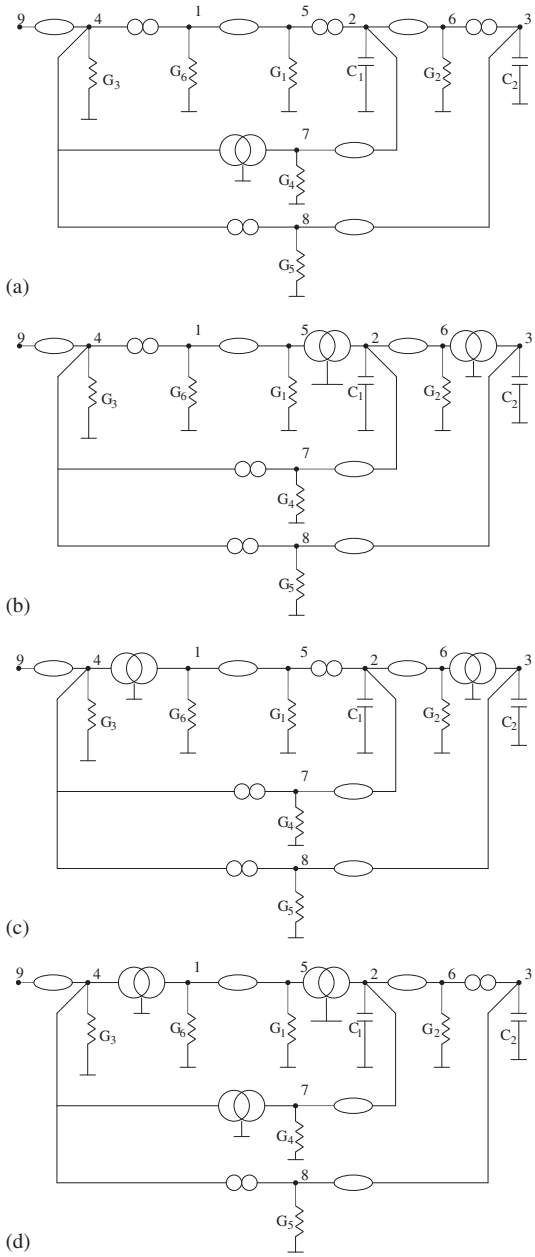

Figure 4. (a) Realization of a KHN circuit type B-class I; (b) realization of a KHN circuit type B-class II; (c) realization of a KHN circuit type B-class III; (d) realization of a KHN circuit type B-class IV.

For each of the realizable KHN circuits the three basic circuit equations are given by:

$$\frac{V_1}{V_{IN}} = \pm \frac{\dfrac{s^2 C_1 C_2 G_3}{G_6}}{s^2 C_1 C_2 + \dfrac{s C_2 G_1 G_4}{G_6} + \dfrac{G_1 G_2 G_5}{G_6}} \tag{18}$$

$$\frac{V_2}{V_{IN}} = \pm \frac{\dfrac{s C_2 G_1 G_3}{G_6}}{s^2 C_1 C_2 + \dfrac{s C_2 G_1 G_4}{G_6} + \dfrac{G_1 G_2 G_5}{G_6}} \tag{19}$$

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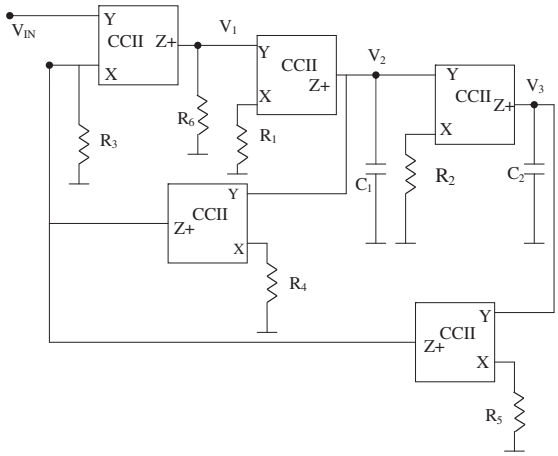

Figure 5. CCII+ realization of type A-class II circuit of Figure 3(b).

$$\frac{V_3}{V_{IN}} = \pm \frac{\dfrac{G_1 G_2 G_3}{G_6}}{s^2 C_1 C_2 + \dfrac{s C_2 G_1 G_4}{G_6} + \dfrac{G_1 G_2 G_5}{G_6}} \tag{20}$$

The sign of the transfer function will depend on the type and class of circuit. From the above equations, ω_O and Q are given by:

$$\omega_O = \sqrt{\frac{G_1 G_2 G_5}{C_1 C_2 G_6}} \tag{21}$$

$$Q = \frac{1}{G_4}\sqrt{\frac{C_1 G_2 G_5 G_6}{C_2 G_1}} \tag{22}$$

For specified ω_O and Q the recommended design equations are given by:
Taking $C_1 = C_2 = C$, $G_1 = G_2 = G$ and $G_5 = G_6$

$$G = \omega_O C, \quad G_4 = \frac{G_5}{Q} \tag{23}$$

It is seen that G_4 controls Q without affecting ω_O. The gain is controlled by G_3 without affecting ω_O or Q.

For HP filter and for a specified high frequency gain H the design value of G_3 is given by:

$$G_3 = H G_6 \tag{24a}$$

For BP filter and for a specified center frequency gain H the design value of G_3 is given by:

$$G_3 = H G_4 \tag{24b}$$

For LP filter and for a specified DC gain H the design value of G_3 is given by Equation (24a).

7. ADDITIONAL REALIZATIONS USING ICCII

7.1. Type A-class I

Additional circuits for type A-class I circuits can be generated using NAM expansion and using VM for transferring negative conductance's from column to anther column. For example, consider

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Equation (12) and then add blank eighth- row and column and then a VM is connected between nodes 3 and 8 to move $-G_5$ to column eight and it becomes G_5 as follows:

$$Y = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & sC_1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & sC_2 & 0 & 0 & 0 & 0 & 0 \\ -G_6 & 0 & 0 & G_3 & 0 & 0 & 0 & G_5 \\ 0 & 0 & 0 & 0 & G_1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & G_2 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & G_4 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \tag{25}$$

A norator is connected between nodes 4 and 8 to move G_5 to the diagonal position 8, 8. A CM is also connected between nodes 4 and 1 to move $-G_6$ to be G_6 at the position 1, 1 as follows:

$$Y = \begin{bmatrix} G_6 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & sC_1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & sC_2 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & G_3 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & G_1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & G_2 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & G_4 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & G_5 \end{bmatrix} \tag{26}$$

After adding a nullator between node 4 and 9 to achieve the desirable high input impedance, the above equation is realizable by four nullators, one VM, four norators and one CM as shown in Figure 6(a).

It should be noted that when using a nullator between nodes 4 and 9 to provide very high input impedance, the total number of circuits for each class is 16 circuits. Therefore, the total number of circuits for each type (which includes four classes) will be 64 circuits resulting in a total of 128 circuits for both types A and B.

If a VM is used instead of the nullator between nodes 4 and 9 a similar number of circuits can be obtained. It should be noted that when a VM is used at the input between nodes 4 and 9 the polarity of the voltage V_4 is related to V_{IN} by a negative sign, which must be taken into consideration in the first step when the 4×4 NAM equation is formulated before the start of the expansion of the NAM equation to obtain the desirable KHN circuit with the desirable polarities of HP, BP and LP. To illustrate the above statements, two more circuits are considered next.

7.2. Type A- class I with VM at input

To realize a type A-class I KHN circuit having a non-inverting HP, an inverting BP and a non-inverting LP and since a VM will be used at the input between nodes 4 and 9, the sign of V_4 must

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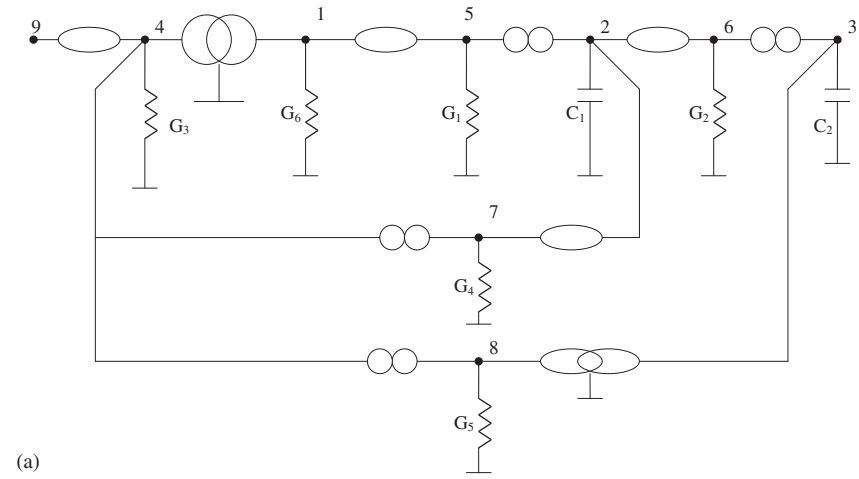
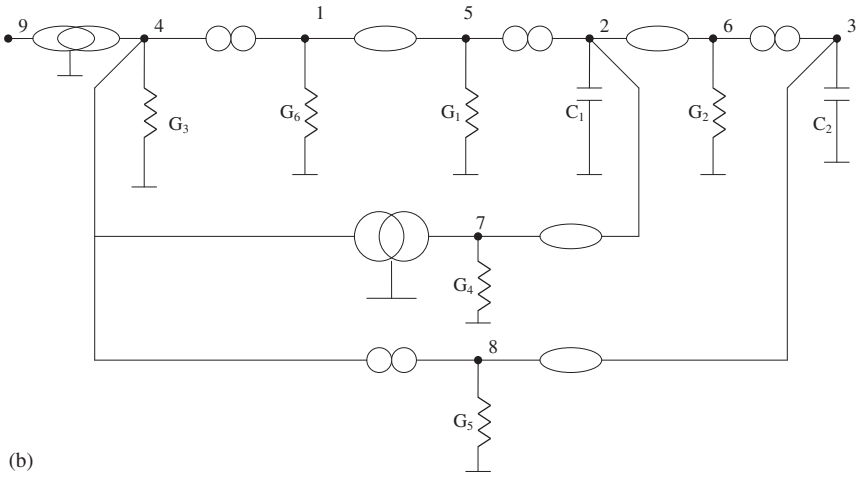
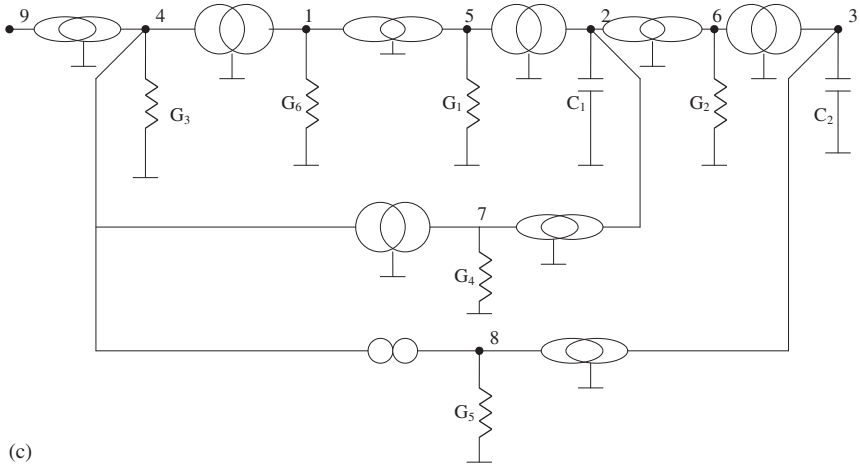


(a)



(b)



(c)

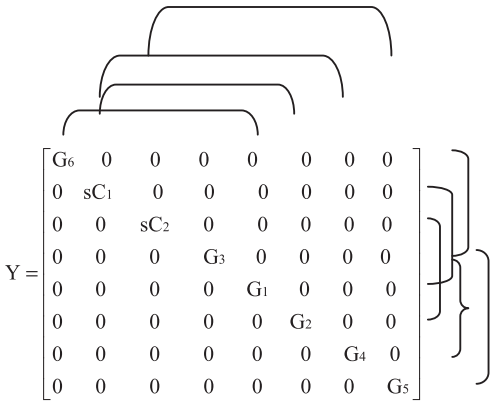
Figure 6. (a) Alternative realization of KHN circuit type A-Class I; (b) realization of KHN circuit using one ICCII−, one CCII+ and three CCII−; (c) four ICCII+ and one ICCII− realization of a KHN circuit.

DOI: 10.1002/cta

be changed in the summation equation given in Table I. Thus, the NAM equation to start with is that given by:

$$Y = \begin{bmatrix} 0 & 0 & 0 & 0 \\ G_1 & sC_1 & 0 & 0 \\ 0 & G_2 & sC_2 & 0 \\ G_6 & -G_4 & G_5 & G_3 \end{bmatrix} \tag{27}$$

Following successive steps using nullators, norators and CM the following equation is obtained.



(28)

Adding a VM between nodes 4 and 9, the KHN circuit is shown in Figure 6(b), which uses one ICCII−, one CCII+ and three CCII−.

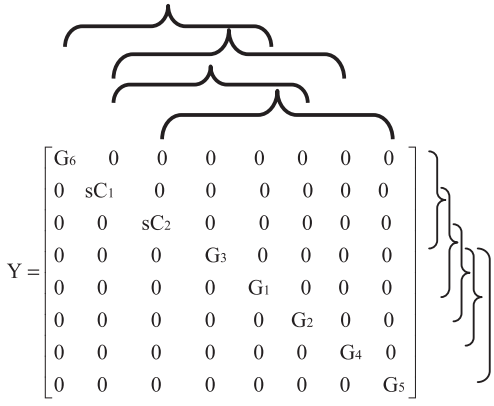
7.3. Type B-class I with VM at input

The realization of an ICCII KHN circuit is considered in this section.

In this case a VM is to be used between nodes 4 and 9 to provide the desirable high input impedance. To realize type B-class I KHN circuit having an inverting HP, non-inverting BP and inverting LP responses and taking into consideration that a VM will be used at the input, in this case the starting point will be the NAM given by:

$$Y = \begin{bmatrix} 0 & 0 & 0 & 0 \\ G_1 & sC_1 & 0 & 0 \\ 0 & G_2 & sC_2 & 0 \\ -G_6 & G_4 & -G_5 & G_3 \end{bmatrix} \tag{29}$$

Following successive steps using VM and no nullators, the following equation is obtained.



(30)

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Adding a VM between nodes 4 and 9, the circuit shown in Figure 6(c), which uses four ICCII+ and one ICCII−, is obtained [11].

Many other circuits can be generated following similar steps.

8. PARASITIC ELEMENT EFFECTS

All the KHN circuits reported here have the same topology. The parasitic resistances R_{X2}, R_{X3}, R_{X4} and R_{X5} can be compensated by subtracting their values from the design values of the resistance R_1, R_2, R_4 and R_5 respectively. The parasitic capacitances C_{Z1} and C_{Z2} can be compensated by subtracting their values from the design values of the capacitances C_1 and C_2 respectively.

The only parasitic elements that are affecting the circuit operation are R_{X1}, C_{Z1}, C_{Z4} and C_{Z5}. Taking these parasitic elements into consideration, it can be proved that the actual value of V_1 is related to its ideal value by the following error function:

$$\frac{V_1(\text{actual})}{V_1} = \frac{1}{(1+s(C_{Z4}+C_{Z5})R_{X1})(1+sC_{Z1}R_6)}$$

$$\frac{V_1(\text{actual})}{V_1} \cong \frac{1}{(1+s(C_{Z4}+C_{Z5})R_{X1}+sC_{Z1}R_6)}$$

$$\cong \frac{1}{(1+sC_{Z1}R_6)} \tag{31}$$

From the above equation the frequency limitation is seen. Equation of the family of KHN circuits is determined by C_{Z1} R_6, which can be reduced by using a large value of R_6.

9. SIMULATION RESULTS AND DISCUSSION

Although the main paper objective is to provide novel approach for the generation of current conveyor-based KHN circuits using NAM expansion, it may be of interest to show simulations of some of the reported KHN circuits. For a fair comparison among the different circuits, the same CMOS generalized conveyor circuit shown in Figure 7 [7, 8] is used in the simulations.

The transistor aspect ratio for the generalized conveyor circuit shown in Figure 7 is given in Table V based on the 0.5μm CMOS model from MOSIS. The supply voltages used are ±1.5 V and $V_{B1} = -0.52$ V and $V_{B2} = 0.33$ V.

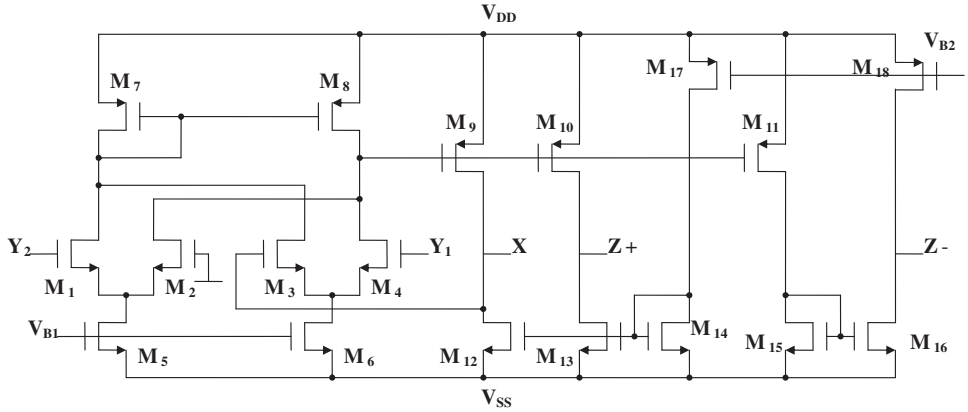

Figure 7. CMOS generalized CCII and ICCII circuit [7, 8].

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Table V. Dimensions of the MOS transistors of Figure 7.

MOS Transistors	$W(\mu m)/L(\mu m)$
M_1, M_2, M_3 and M_4	2.5/1
M_5 and M_6	8/1
M_{12}, M_{13}, M_{14}, M_{15} and M_{16}	20/2.5
M_7 and M_8	10/1
M_9, M_{10}, M_{11}, M_{17} and M_{18}	40/2

Seven different KHN circuits are simulated using the CMOS circuit of Figure 7 which realizes:

(i) CCII+ with Y_2 and $Z-$ grounded.
(ii) CCII− with Y_2 and $Z+$ grounded.
(iii) ICCII+ with Y_1 and $Z-$ grounded.
(iv) ICCII− with Y_1 and $Z+$ grounded.

Figure 8(a) represents the magnitude and phase characteristics together with the ideal response of the BP output of the circuit of Figure 3(a) designed to have a center frequency of 1 MHz, gain of 10 at the center frequency and $Q=10$.

The circuit design parameters taken are $C_1=C_2=10\,\text{pF}$, $R_1=R_2=15.9\,\text{k}\Omega$, $R_5=R_6=10\,\text{k}\Omega$, $R_4=100\,\text{k}\Omega$ and $R_3=10\,\text{k}\Omega$.

It is seen that the simulation results agree with the ideal responses. The total power dissipation is 4.89479 mW.

Figure 8(b) represents the magnitude and phase characteristics together with the ideal response of the BP output of the circuit of Figure 3(b) designed with the same values as above. It is seen that the simulation results agree with the ideal responses. The total power dissipation is 4.92025 mW.

Figure 8(c) presents the magnitude and phase characteristics together with the ideal response of the BP output of the circuit of Figure 3(c) designed with the same values as above. It is seen that the simulation results agree with the ideal responses. The total power dissipation is 4.90141 mW.

Figure 8(d) represents the magnitude and phase characteristics together with the ideal response of the BP output of the circuit of Figure 3(d) designed with the same values as above. It is seen that the simulation results agree with the ideal responses. The total power dissipation is 4.91105 mW.

Figure 9(a) represents the magnitude and phase characteristics together with the ideal response of the BP output of the circuit of Figure 4(a) designed with the same values as above. It is seen that the simulation results agree with the ideal responses. The total power dissipation is 4.87753 mW.

Figure 9(b) represents the magnitude and phase characteristics together with the ideal response of the band-pass output of the circuit of Figure 6(b) designed with the same values as above. It is seen that the simulation results agree with the ideal responses. The total power dissipation is 4.87753 mW

For fair comparison the same generalized conveyor circuit was used and it is seen that all of the simulated circuits operate nearly as ideal and the power dissipation is almost identical in all of them.

Figure 10(a) represents a new floating KHN circuit, which belongs to type B class II and it uses three CCII− and two ICCII− and has three inverting output responses.

Figure 10(b) represents the magnitude and phase characteristics together with the ideal response of the inverting LP output of the circuit of Figure 10(a) designed to have a maximally flat magnitude response, Q equal to 0.707, cutoff frequency of 1 MHz and unity DC gain.

The circuit design parameters taken are $C_1=C_2=10\,\text{pF}$, $R_1=R_2=15.9\,\text{k}\Omega$, $R_5=R_6=10\,\text{k}\Omega$, $R_4=7.07\,\text{k}\Omega$ and $R_3=10\,\text{k}\Omega$.

It is seen that the simulation results are close to the ideal responses.

It is worth noting that if a different CMOS current conveyor circuit is used, the results obtained may be slightly different, but in this case the evaluation will be for the CMOS conveyor circuit not to the KHN filter circuit.

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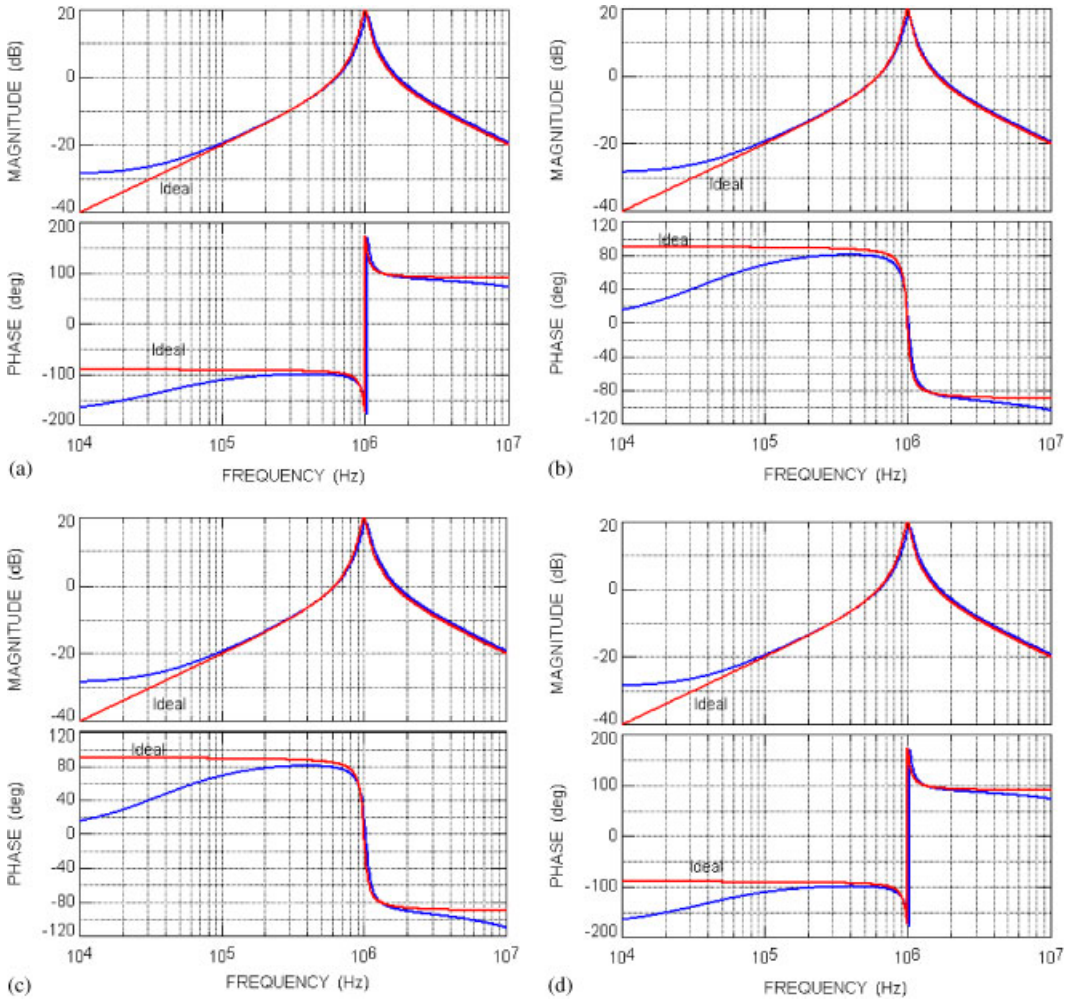

Figure 8. (a) BP frequency response of KHN of Figure 3(a); (b) BP frequency response of KHN of Figure 3(b); (c) BP frequency response of KHN of Figure 3(c); and (d) BP frequency response of KHN of Figure 3(d).

It is seen that several KHN circuits are available for the designer. The one to use depends on the types of CCII or ICCII one is interested to use and the desirable polarity for HP, BP and LP interested to achieve.

It should be noted that in generating alternative Op Amp KHN circuits from Figure 1(a) by alternative pairing of nullators and norators, eight different circuits in topology are obtained. Taking the effect of the single pole model of the Op Amp into consideration, only one circuit is found to have zero Q sensitivity as given in [24].

Here the situation is different: we are not altering the pairing of pathological elements and all 256 have same topology and have the same non-ideal effects caused by parasitic elements as explained in Section 8.

10. CONCLUSIONS

NAM expansion is used to generate a family of grounded passive component KHN circuits. The generated KHN circuits have independent control on the selectivity factor and the radian frequency

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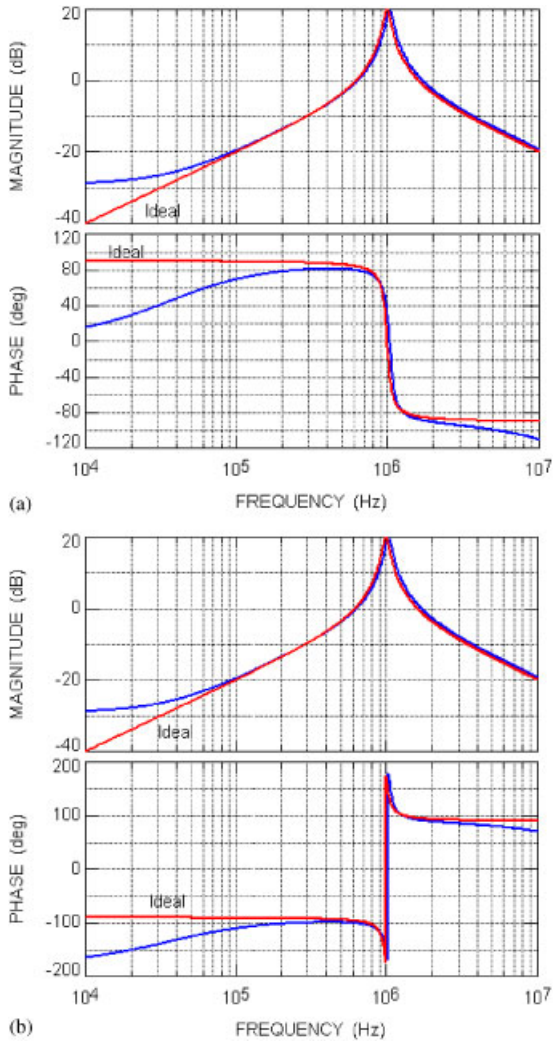

Figure 9. (a) BP frequency response of KHN of Figure 4(a) and (b) band-pass frequency response of KHN of Figure 6(b).

as in the original KHN, besides they have independent control on the gain, which is not possible in the original KHN circuit. The NAM expansion is based on using nullor elements and pathological VM and CM as well. The two types of the KHN circuit are considered, each type includes four classes. Using a nullator at the input to provide the desirable high input impedance it is found that there are 16 different KHN circuit for each class; therefore, there are a total of 64 circuits that belong to each type. Using a VM at the input to provide the desirable high input impedance it is found that there are also 16 different KHN circuits that belong to each class. It is worth noting that the summer stage equations given in Tables I and III and the corresponding NAM equations in Tables II and IV are based on the assumption that a nullator is used at the input to provide the desirable high input impedance. If a VM is used instead of the nullator at the input, the equations should be modified. Of course more circuits can be generated by alternative pairing of nullor elements and mirror elements. Among the generated circuits there are eight circuits that have floating property and they cannot be obtained using CCII alone. This demonstrates the advantage of combining CCII and ICCII in KHN realizations.

It should be noted that the generation of Op Amp-based KHN circuits by alternative pairing of nullators and norators resulting in eight alternative KHN circuits, one of them was given in [24].

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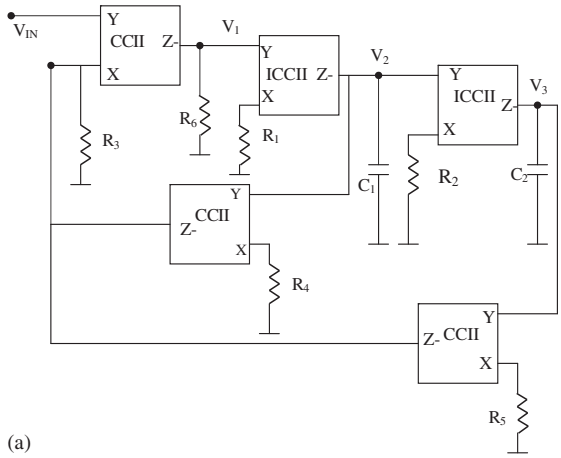
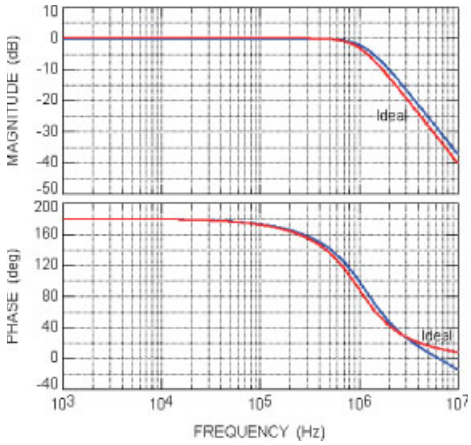


(a)



(b)

Figure 10. (a) A three CCII−, two ICCII− floating KHN circuit and (b) LP frequency response of KHN of Figure 10(a).

It is also worth noting that a general synthesis technique of active-RC filters was given in [25] as well as matrix generation methods of Gm-C filters were given in [26–28].

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