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A New Approach to Obtain Alternative Active Building Blocks Realizations based on their Ideal Representations

Ein neues Vorgehen zur Realisierung alternativer aktiver Schaltungen, das auf idealen Ersatzdarstellungen beruht

Abstract
This paper describes a systematic approach to obtain alternative realizations for a particular active building block based on its simple ideal representation. The proposed approach relies on the properties of two categories of ideal elements; the well-known nullor elements and the mirror elements, which are basically used to model the active devices featuring voltage or current inverting properties. These ideal elements are used to obtain ideally equivalent nullor-mirror representations for a particular active device. The described approach results in alternative representations which give the designer a choice of circuits that may be used to build the active device with the possibility of enhancing its characteristics. As an example, the proposed approach is used to generate alternative realizations for the negative type of the second-generation current conveyor (CCII–). Most of the CCII– realizations result in high performance in terms of impedance level, accuracy and frequency response. PSpice simulations that demonstrate the performance of the different realizations are also given.

Übersicht
Dieser Beitrag beschreibt das systematische Vorgehen, Alternativen zu einer bestimmten aktiven Grundschaltung zu realisieren, die auf deren einfacher idealisierter Ersatzdarstellung beruht. Der Vorschalg baut auf zwei Kategorien von idealen Elementen auf: den gut bekannten Nullor- und den Minor-Elementen, die grundsätzlich verwendet werden, um aktive Schaltungen zu modellieren, die die Eigenschaft haben, Spannung oder Strom zu invertieren. Diese idealen Elemente werden verwendet, um ideale äquivalente Nullor-Minor-Ersatzdarstellungen für eine bestimmte aktive Schaltung zu erhalten.
Die beschriebene Verfahrensweise führt zu alternativen Darstellungen, die dem Schaltungsentwickler eine Auswahl von Schaltungen anbieten, die zum Aufbau der aktiven Schaltungen verwendet werden können mit der Möglichkeit, deren Eigenschaften zu verbessern.
Als Beispiel wird die vorgeschlagene Methode verwendet, um alternative Realisierungen des invertierenden Stromspiegels (ideale invertierende stromgesteuerte Stromquelle CCII) zu generieren. Die meisten CCII-Realisierungen führen zu qualitativ hochwertigen Ergebnissen hinsichtlich Impendanzniveau, Genauigkeit und Frequenzcharakteristik.
Pspice-Simulationen, die die Leistungsfähigkeit der verschiedenen Realisierungsmöglichkeiten demonstreiren, werden ebenfalls angegeben.

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Für die Dokumentation
Nullor / Stromspiegel / Stromübertrager

1. Introduction

In the process of designing active circuits it is useful to follow systematic methodologies to obtain new circuits. This is helpful in developing analog tools for automatic circuit design. The nullor elements [1, 2] have been found useful in solving circuit analysis and design problems and many authors have investigated the use of nullor-based methods or computational algorithms for the synthesis of analog circuits [3–7]. The attractive feature of the two nullor elements (the nullator and the norator) is their ability to model active circuits independently of the particular realization of the active devices with the possibility of generating a number of equivalent idealized circuits from which the best practical ones can thereafter be selected [8, 9]. Despite the ability of nullators and norators to represent many active building blocks, they fail to represent the positive type second-generation current conveyor (CCII+) proposed in [10]. Other elements like resistors are combined with the nullators and norators in order to obtain the nullor representation of the CCII+ [11]. In order to avoid the use of the resistors in the nullor representation of any building block, two elements are defined and given names: the current mirror and the voltage mirror [12]. These elements are basically used to represent active devices with current or voltage reversing properties.

The objective of this paper is to present a systematic approach to obtain alternative realizations for a particular active building block. This is achieved by generating ideally equivalent nullor-mirror representations for the building block from its simple ideal representation. The generated representations are realized in different ways according to the pairing of the nullors and the mirrors and to the building block used in the realizations.

The proposed approach has a great importance in interrelating different active building blocks since it describes how a given building block can be realized using other building blocks. This can be helpful to profit from the characteristics of high-performance active devices by using them to realize other devices. Besides the theoretical interest in the proposed approach, it can be of great importance when there is a need to replace a particular component by another one, which is commercially available. For example, in practice the negative type second-generation current conveyor (CCII–) is realized using two units of the CCII+, which is commercially available [13].

The paper begins by summarizing the definitions of the nullors and mirrors. The proposed approach is used to obtain alternative realizations for the CCII–. A classification of the CCII–realizations is given and their characteristics are discussed. Most of the realizations are found to have high performance in terms of input impedance, bandwidth and voltage and current tracking accuracy. Though this paper focuses on the CCII–, the same procedure can be used to obtain alternative representations for other building blocks.

2. The Nullor and Mirror Elements

The set of nullor elements comprises the nullator and the norator [2]. The nullator is a one-port network element defined by $V = I = 0$ and its symbol is shown in **Fig. 1(a)**. It is a bilateral and lossless one-port. On the other hand, the norator is a one-port network element defined by arbitrary V and I and its symbol is shown in **Fig. 1(b)**.

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(a) (b)

Fig. 1: The symbolic representations of the nullator and the norator

(a) (b)

Fig. 2: The symbolic representations of the voltage mirror and the current mirror

The two mirror elements are the voltage mirror and the current mirror [12] and their symbols are shown in **Figs. 2(a)** and **2(b)** *respectively. The voltage mirror is a loss-less two port network element* used to represent a voltage reversing action and is defined by:

$$V_1 = -V_2 \qquad (1a)$$

$$I_1 = I_2 = 0. \qquad (1b)$$

The current mirror is a two port network element used to represent a current reversing action and is defined by:

V_1 and V_2 which are arbitrary.

$I_1 = I_2$, and they are also arbitrary. (2)

3. The Proposed Approach

Generally, any active building block can be ideally represented by a combination of the four ideal elements (the nullors and the mirrors). Moreover, in a physically realizable circuit all the voltages and currents are always uniquely and definitely determined. This in turn implies that in the ideal representation of a physically realizable circuit the nullator (or the voltage mirror) and the norator (or the current mirror) must occur in a pair. Hence, the simplest ideal representation of a given active device can be formed of one pair of ideal elements. The first step in order to obtain alternative building block realizations is to modify its simple nullor-mirror representation such that the modified representations have an increased number of ideal elements. Then, the modified representations can be realized in different ways according to the pairing of the ideal elements. The generation of the modified ideally equivalent representation from the simple building block ideal representation is based on the following nullor-mirror properties:

i. Each of the four ideal elements can be replaced by a set of three ideal elements and sometimes with two additional matched MOS transistors biased with the same gate voltage and operated in the ohmic region. For example, two cascaded current mirrors and a nullator parallel to one of the two current mirrors can replace a norator. **Figs. 3** through **6** show the equivalent representations of the nullator, norator, voltage mirror and current mirror respectively.
ii. The open-circuit can be represented by a nullator in series with a norator or a current mirror as shown in **Figs. 7(a)** and **7(b)** or by a voltage mirror in series with a norator or a current mirror as shown in **Figs. 7(c)** and **7(d)**.
iii. The short-circuit can be represented by a nullator in parallel with a norator as shown in **Fig. 8**.

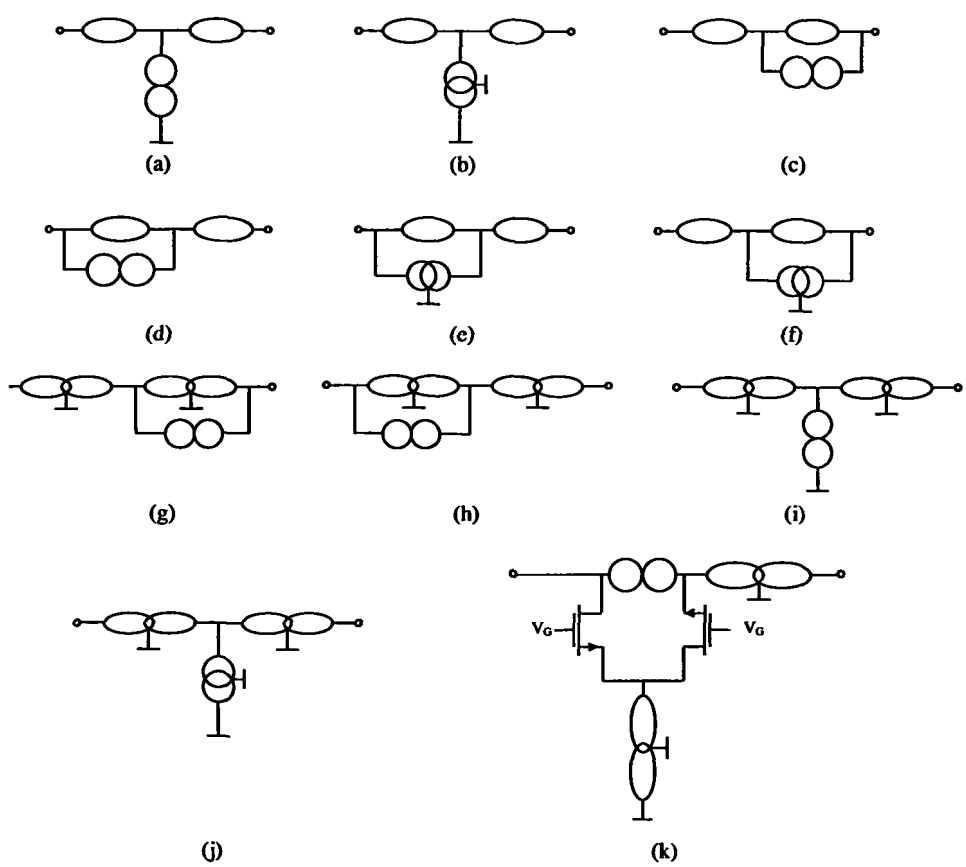


Fig. 3: The nullator equivalent representations

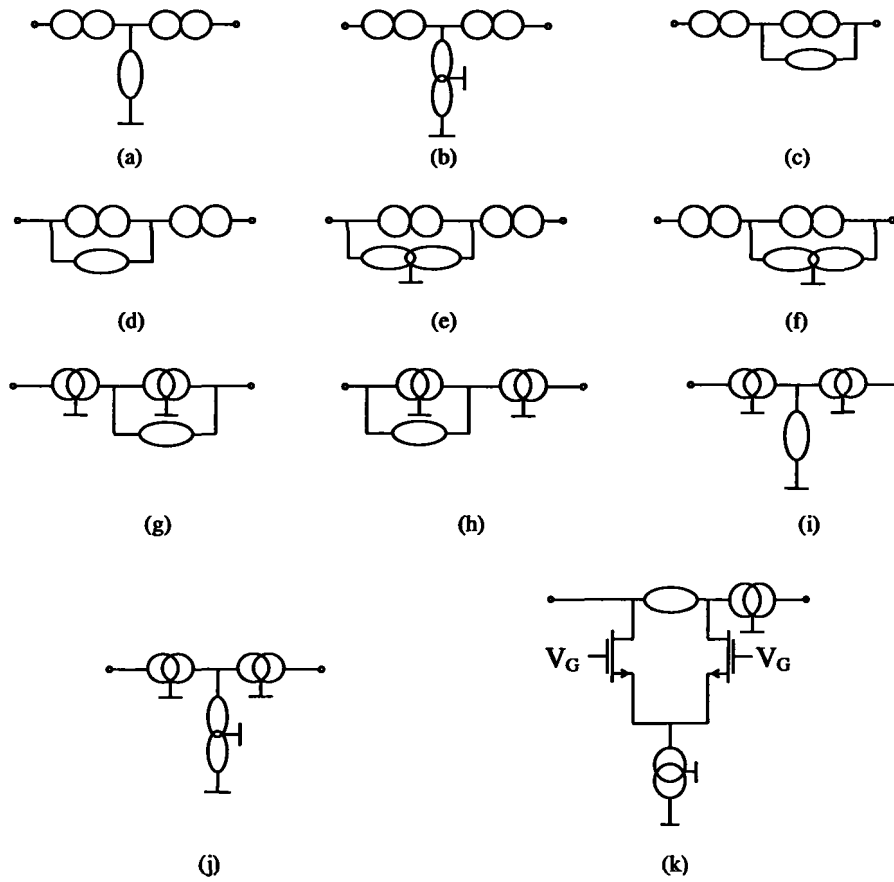


Fig. 4: The norator equivalent representations

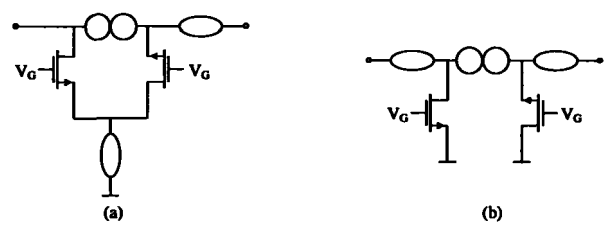


Fig. 5: The voltage mirror equivalent representations

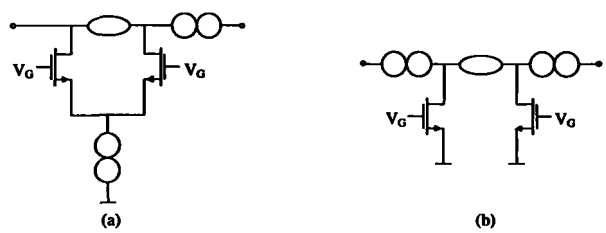


Fig. 6: The current mirror equivalent representations

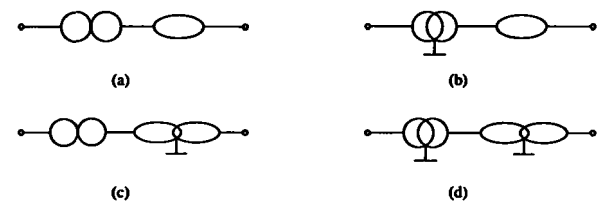


Fig. 7: The open-circuit equivalent representations

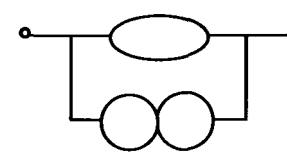


Fig. 8: The short-circuit equivalent representation

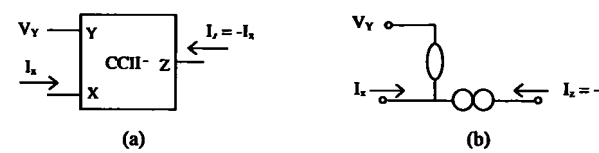


Fig. 9: The CCII–; (a) symbolic representation; (b) nullor representation

It is worth noting that additional equivalent representations for the four ideal elements, the open circuit and the short-circuit can be obtained by recursively applying the above-mentioned three modifications to the representations shown in Figs. 3 through 8.

4. Generation of CCII– Alternative Realizations

The CCII– shown in **Fig. 9(a)** is basically a combined voltage follower and negative type current follower. The simple nullor representation of the CCII– consists of a nullator connected to a norator as shown in **Fig. 9(b)**. The procedure described in section 3 can be used in order to obtain the complete set of the CCII– ideal equivalent representations by replacing the norator, the nullator, any short circuit or open circuit in Fig. 9(b) by their equivalent representations. However, in this paper and for simplicity, the

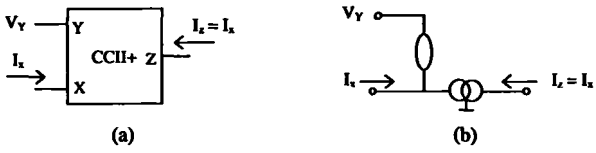


Fig. 10: The CCII+; (a) symbolic representation; (b) nullor-mirror representation

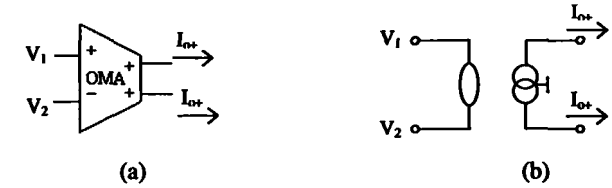
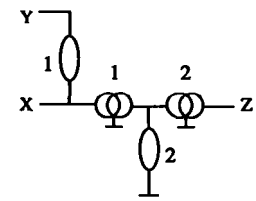
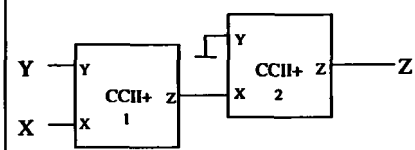
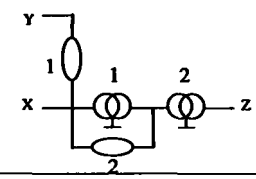
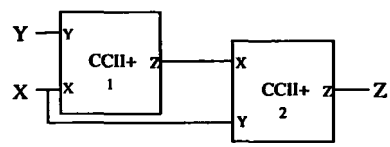
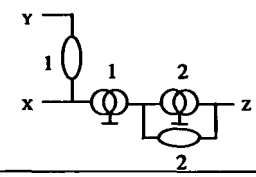
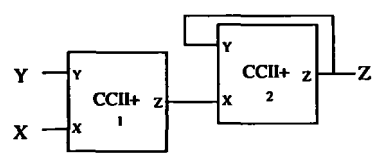
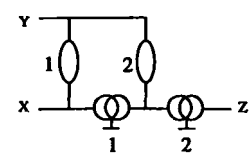
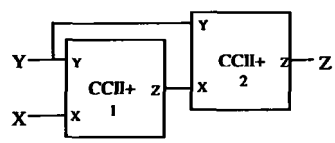
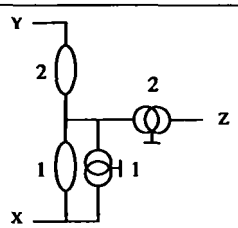
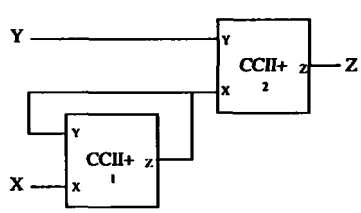
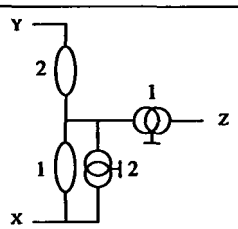
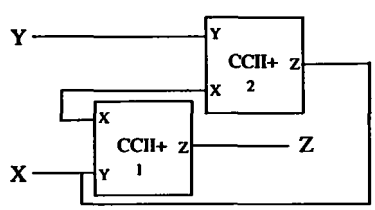


Fig. 11: The OMA; (a) symbolic representation; (b) nullor-mirror representation

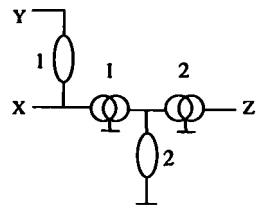
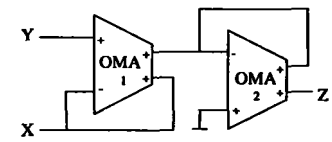
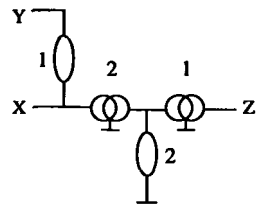
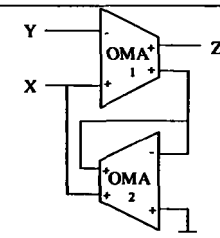
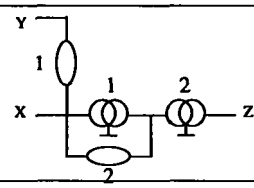
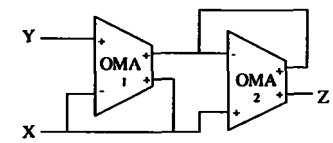
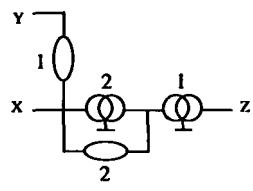
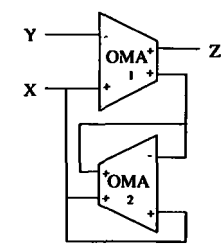
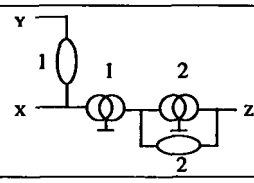
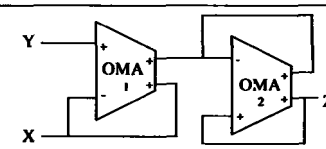
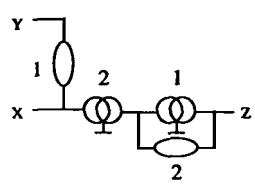
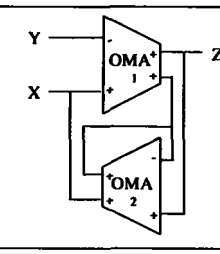
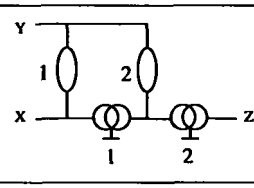
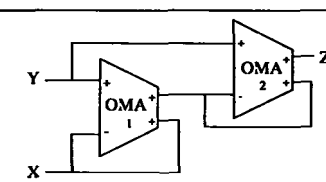
Table 1: The CCII– equivalent nullor-mirror representations and their CCII+ based realizations

No.	CCII- nullor-mirror representation	CCII+ based CCII- realization
1		
2		
3		
4		
5		
6		

ideal elements used in the CCII– ideally equivalent nullor-mirror representations will be restricted to the nullator and the current-mirror. As shown in **Figs. 10** and **11**, the nullator-(current-mirror) pair can be realized using the CCII+ [10] or the operational mirrored amplifier (OMA) [14], which is basically an operational transconductor amplifier with double output currents. As shown in **Tables 1** and **2**, six different CCII– ideally equivalent nullor-mirror representations are obtained. These representations are realized in different ways according to the pairing of the two ideal elements, resulting in six CCII+ based realizations and twelve OMA based realizations as shown in Tables 1 and 2 respectively.

Although the CCII– realizations shown in Tables 1 and 2 are ideally equivalent, they have different characteristics that can be evaluated by considering the actual behavior of the basic block used in the realizations. The main parameters used to evaluate the CCII– realizations are the output current transfer gain (A_i), the output current offset (I_{Zoff}), the input impedance seen at the X terminal (R_X), the voltage transfer gain (A_v) and the voltage offset

Table 2: The CCII- equivalent nullor-mirror representations and their OMA based realizations

No.	CCII- nullor-mirror representation	OMA based CCII- realization
1		
2		
3		
4		
5		
6		
7		

(V_{Xoff}). The actual behavior of the CCII- is described using the following equations:

$$I_Y = 0 \tag{3a}$$

$$V_X = A_v V_Y + I_X R_X + V_{Xoff} \tag{3b}$$

$$I_Z = A_i I_X + I_{Zoff}. \tag{3c}$$

While the ideal behavior of the CCII- is described by:

$$A_v = -A_i = 1 \tag{4a}$$

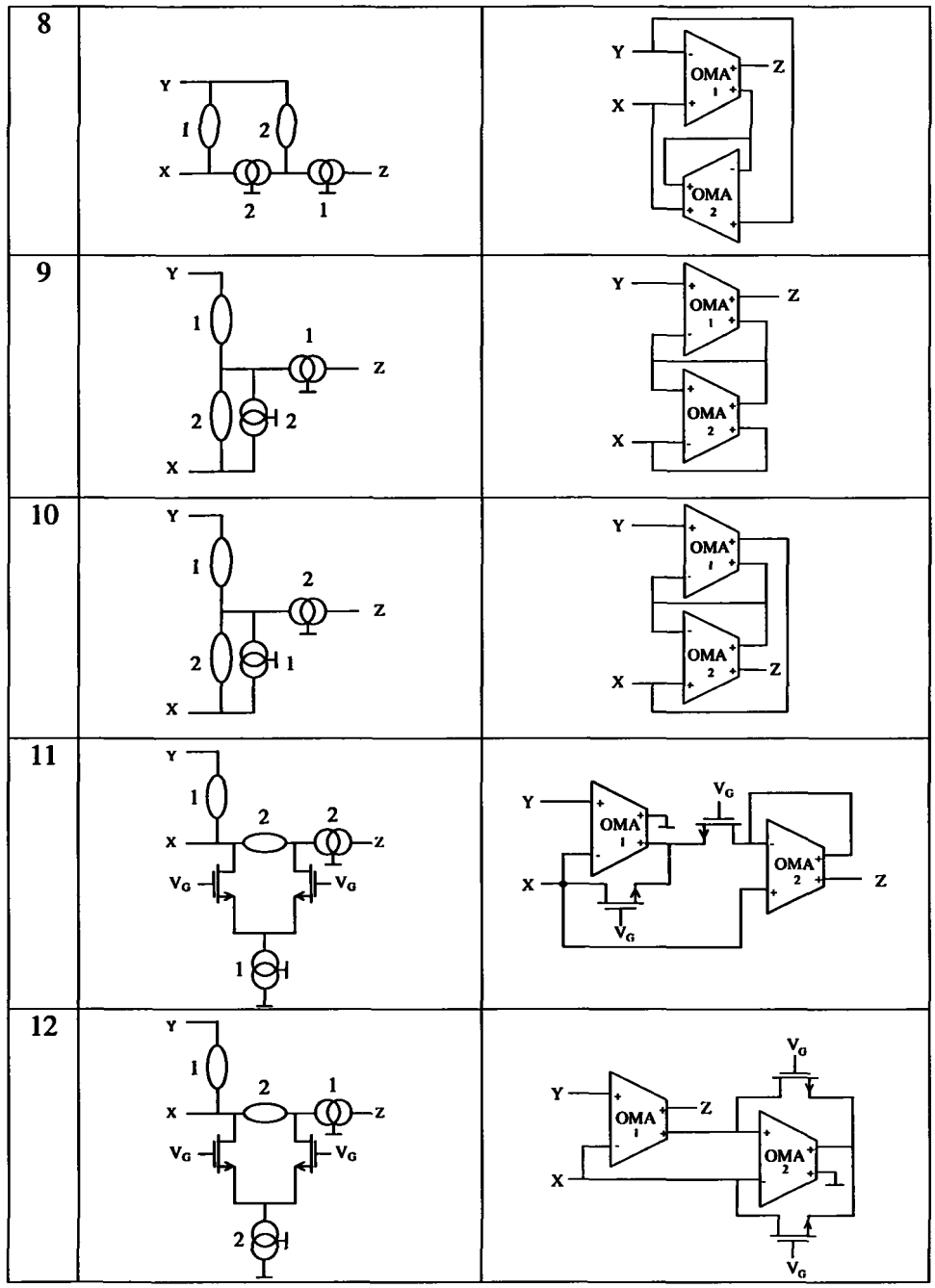
$$R_X = 0 \tag{4b}$$

$$V_{Xoff} = 0 \tag{4c}$$

$$I_{Zoff} = 0. \tag{4d}$$

In the evaluation of the CCII- realizations, the terms voltage magnitude error (E_v) and current magnitude error (E_i) will be used to represent the deviation of the gains magnitudes from unity, i.e., ($E_v = 1 - |A_v|$ and $E_i = 1 - |A_i|$). The terms Φ_v and Φ_i are used to represent the phase errors of the voltage and current transfer gains respectively.

The CCII- realizations are classified into two classes according to the building block used.



4.1. The CCII- Class I Realizations

This class consists of the CCII+ based CCII- realizations shown in Table 1. The practical parameters of these realizations are evaluated in terms of the CCII+ parameters. Eqn. (3) is used to describe the actual behavior of the CCII+. The conditions for ideal CCII+ behavior are the same as those given in (4), except that A_i is equal to unity in the case of the CCII+.

The realizations no. 1 through 4 in Table 1 represent the conventional approach of realizing the CCII- using two cascaded CCII+s [15-16]. In these realizations, the input impedance (R_X), the voltage transfer gain (A_v) and offset (V_{Xoff}) are the same as those of the CCII+ used.

The realization no. 5 in Table 1 was introduced in [15] and it features a reduced R_X, which is given by:

$$R_X = R_{X1} - R_{X2} \tag{5}$$

where R_{X1} are R_{X2} are the input impedances of the two CCII+ used in the realization.

In each of the CCII+ based realizations no. 1 through 5, the current transfer gain, current offset, current magnitude and phase errors of the CCII- are given by:

$$A_i(s) = -A_{i1}(s)A_{i2}(s) \tag{6}$$

$$I_{zoff} = I_{zoff2} - A_{i2}I_{zoff1} \tag{7}$$

$$E_i = 1 - |A_i| = E_{i1} + E_{i2}(1 - E_{i1}) \tag{8}$$

$$\Phi_i = \Phi_{i1} + \Phi_{i2} \tag{9}$$

Equation (6) is used to determine the bandwidth of the CCII- in terms of the CCII+ bandwidth. If the CCII+ used has a single dominant pole, then the bandwidth of the CCII- realizations no. 1 through 5 in Table 1 will be lower than that of the CCII+ used. Moreover, the cascading of the two CCII+s results in cur-

rent magnitude and phase errors higher than that of the CCII+ used, as given by (8) and (9).

From (7), if the CCII+ used in the realizations no. 1 through 5 in Table 1 has a constant current offset and a unity current gain, the resulting CCII- current offset will be canceled. However, in simple CMOS realizations of the CCII+ [17], the mismatch between the output current mirrors transistors and the channel length modulation effect result in an output current offset dependent on the output current level as well as the voltage difference between the X and Z terminals of the CCII+. The attractive feature of the realizations no. 2 to 5 in Table 1, is that the voltage difference between the X and the Z terminals of one of the two CCII+ is made equal to zero by changing the connection of Y terminal of the second CCII+. Hence, cancelling the corresponding offset current resulting from the channel length modulation effect.

Referring to realization no. 6 in Table 1, the short circuit current transfer gain, current offset and current magnitude and phase errors of the CCII- are given by:

$$A_i(s) = \frac{-A_{i1}(s)}{A_{i2}(s) + \dfrac{R_{X1}+R_{X2}}{Z_{o2}}} \tag{10}$$

$$I_{zoff} = I_{zoff1} + A_{i1} I_{zoff2} \tag{11}$$

$$E_i = \frac{E_{i1} - E_{i2}}{\left|1 + \dfrac{R_{X1}+R_{X2}}{A_{i2}(s) Z_{o2}}\right|} \tag{12}$$

$$\Phi_i = \Phi_{i1} - \Phi_{i2} - \arg\left(1 + \frac{R_{X1}+R_{X2}}{A_{i2}(s) Z_{o2}}\right) \tag{13}$$

where Z_{o2} is the output impedance seen at the Z terminal of the second CCII+ in the realization no. 6 in Table 1.

By Comparing (10) through (13) with (6) through (9), and assuming that the input impedance at the X terminal R_x is much smaller than the output impedance at the Z terminal Z_o, it can be shown that the realization no. 6 in Table 1 features enhancement in the current transfer gain bandwidth, current magnitude and phase errors. On the other hand, the current offset of this realization is greater than that obtained in the case of the CCII+ based realizations no. 1 through 5.

The realization no. 6 in Table 1 also features high performance in terms of voltage transfer gain, voltage offset, and voltage magnitude and phase errors as given by the following equations:

$$A_v(s) = \frac{A_{v2}(s)}{A_{v1}(s) + \dfrac{R_{X1}+R_{X2}}{A_{i2}(s) Z_{o2}}} \tag{14}$$

$$V_{Xoff} = V_{Xoff2} - V_{Xoff1} \tag{15}$$

$$E_v = \frac{E_{v2} - E_{v1}}{\left|1 + \dfrac{R_{X1}+R_{X2}}{A_{v1}(s) A_{i2}(s) Z_{o2}}\right|} \tag{16}$$

$$\Phi_v = \Phi_{v2} - \Phi_{v1} - \arg\left(1 + \frac{R_{X1}+R_{X2}}{A_{v1}(s) A_{i2}(s) Z_{o2}}\right) \tag{17}$$

The input impedance at the X terminal of the realization no. 6 in Table 1 is given by:

$$R_X = \frac{R_{X1}+R_{X2}}{A_{v1} A_{i2}} // Z_{o2} \tag{18}$$

PSpice Simulations were performed in order to compare between the CCII+ based realizations. The CCII+ is simulated using the CMOS realization given in [17] and shown in **Fig. 12.** The simulation results are shown in **Table 2.** The current transfer

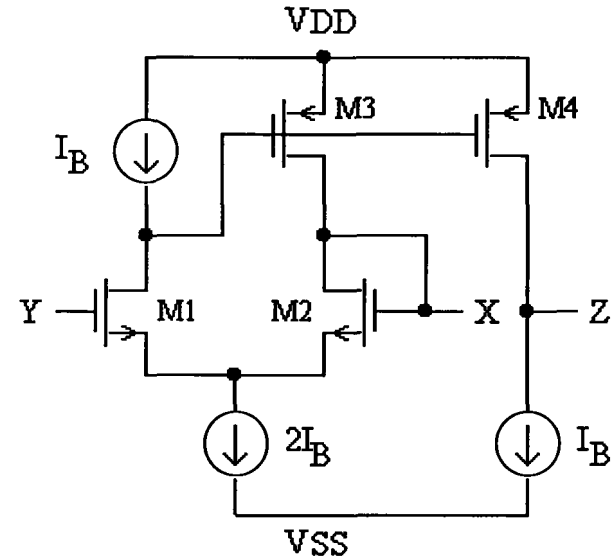


Fig. 12: The CMOS realization of the CCII+ given in [17]

characteristics between the X and Z terminals of the CCII- realizations were simulated with the Y terminal grounded and a load 1 kΩ connected to the output Z terminal. **Fig. 13** shows the frequency response of the current transfer gains of the six CCII- realizations shown in Table 1 respectively. The voltage transfer simulations were carried out with a load of 20 kΩ connected to the X terminal of each CCII- realization and their results are given in **Table 3.**

Table 3: Simulation results for the CCII+ based CCII- realizations

CCII+ based realization No.	R_x (Ω)	I_z f_{3dB} (MHz)	I_{zoff} (nA)	A_i (mdB)	V_X f_{3dB} (MHz)	V_{Xoff} (mVolt)	A_v (mdB)
1	50	32.5	0.1	-274	86	0.2	-60
2	50	31	0.5	-266	86	0.2	-60
2	50	34.7	0.1	-274	86	0.2	-60
3	50	32.5	0.1	-274	86	0.2	-60
4	2.2	39	-0.17	-262	60.9	0.4	-78
5	101	122	-1.1	-5	98	-0.05	-40

The CCII+ based realizations no. 1 through 4 in Table 1 are found to have the smallest current offset. The voltage characteristics and input impedance R_X of these realizations are similar to those of the CCII+ used. On the other hand, the output current bandwidth in these realizations is lower than that of the CCII+ used due the cascading of the two CCII+s. Although the realization no. 5 in Table 1 results in the smallest R_X, its transfer voltage characteristics feature lower bandwidth, higher voltage offset and higher gain errors. The realization no. 6 in Table 1 resulted in voltage and current bandwidths higher than those of the CCII+ used. This realization also features voltage offset cancellation. However, it resulted in the highest R_X and I_{Zoff}.

4.2. The CCII- Class II Realizations

This class consists of the OMA based CCII- realizations shown in Table 2. Simulations were carried out for these realizations using the CMOS realization of the operational transconductor given in [18] and after adding a multiple output current as shown in **Fig. 14.** In each of the realizations no. 11 and 12 in Table 2, two

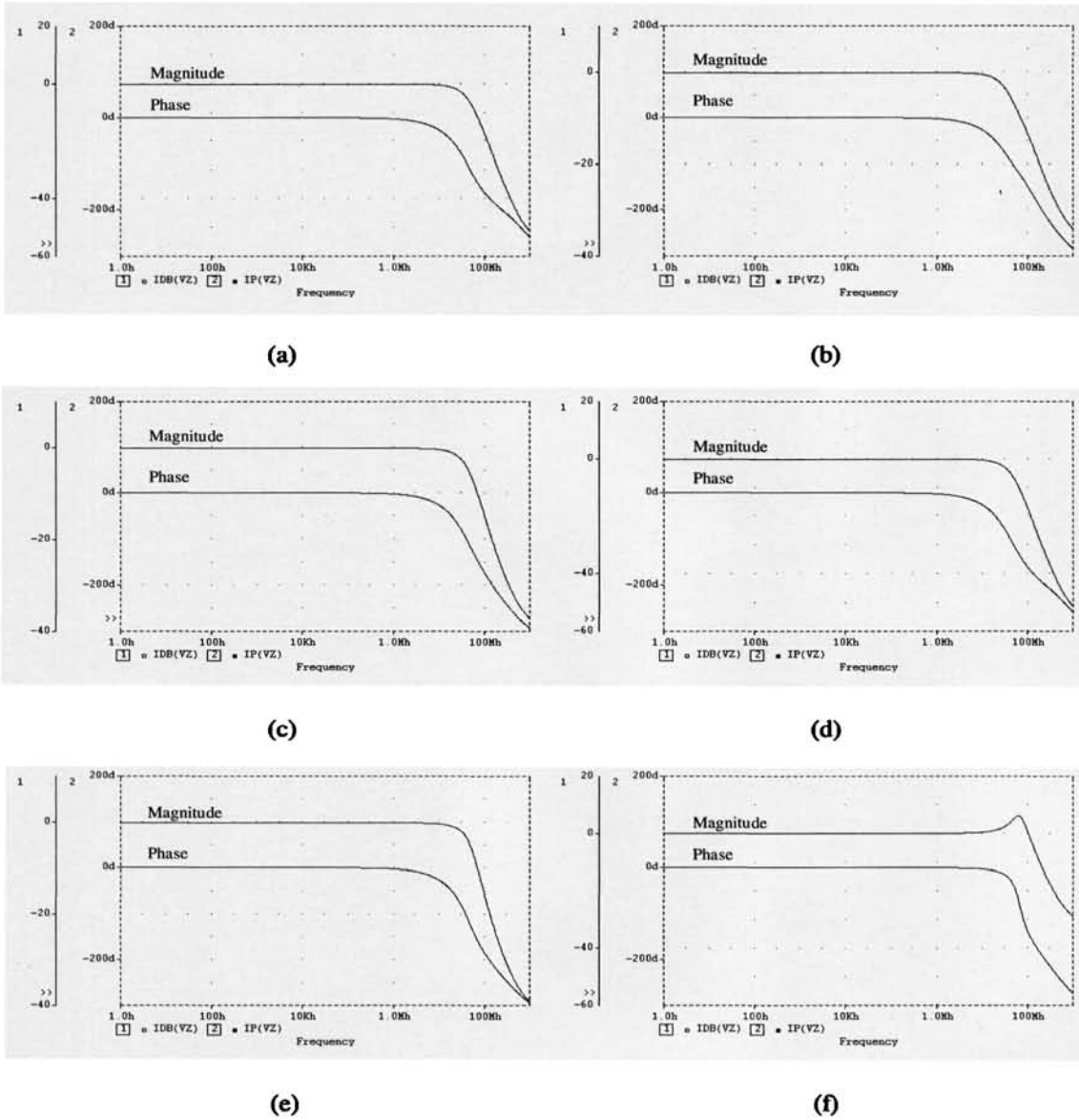


Fig. 13: The frequency response of the current transfer gains of the CCII– class I realizations

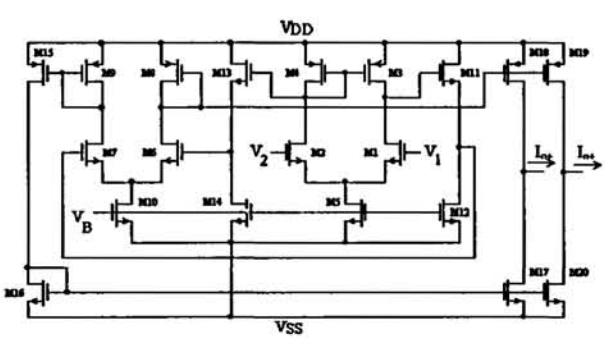


Fig. 14: The CMOS realization of the OMA

matched MOS transistors biased with the same gate voltage are used. The aspect ratio (W μm/ L μm) was equal to 1.2/1.2 for the two MOS transistors and V_G is set to 4 V. The simulation results for this class are given in **Table 4**. The resulted CCII– parameters depend on the characteristics of the used OMA. In most of the realizations, the R_X value is a linear combination of the OMA reciprocal transconductance gain. The realization no. 9 in Table 2 has the smallest R_X, which is given by

$$R_X = \frac{1}{G_2} - \frac{1}{G_1} \qquad (19)$$

Table 4: Simulation results for the OMA based CCII– realizations

OMA based realization No.	R_z (Ω)	I_z f_{3dB} (MHz)	A_i (μdB)	V_X f_{3dB} (MHz)	V_{Xoff} (μVolt)	A_v (mdB)
1	4.15	169	4.65	197	-0.2	-18
2	4.15	248	-2	177	0.2	-28
3	4.15	163.5	1.5	200	-0.2	-18
4	4.15	265	-5.17	174	0.2	-18
5	4.15	156.2	4.65	197	-0.2	-18
6	4.15	279	-2	177	0.2	-18
7	4.15	169	4.65	195	-0.2	-18
8	4.15	243.5	-2	182	0.2	-18
9	0.054	156.5	3.1	205	-0.4	-0.24
10	8.3	211	0	160	0	-35
11	8.3	154	4700	160	-0.2	-35
12	4.15	115	8430	170	-0.2	18

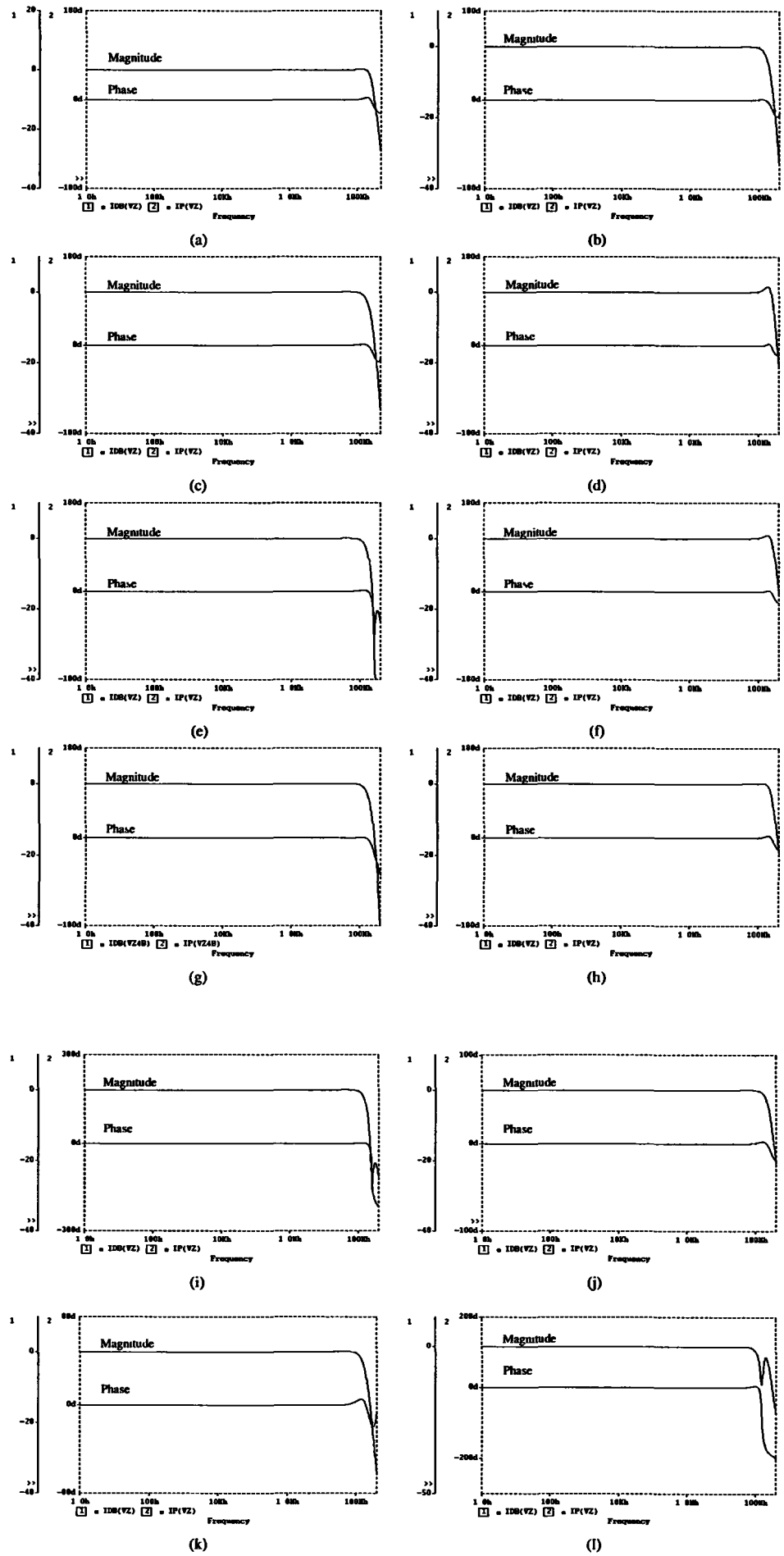


Fig. 15: The frequency response corresponding to the OMA based CCII– realizations

where G_1 is the open loop transconductance gain of the i^{th} OMA.

In the realization no. 9 in Table 2, G_2 and G_1 were equal to 0.241 s and 0.244 s respectively resulting in R_x approximately equal to 54 mΩ.

The realizations of this class feature accurate current transfer characteristics in terms of offset and gain errors due to the used closed loop configurations. The voltage transfer characteristics were simulated with a load of 1 kΩ connected to the X terminal of each CCII- realization. As given in Table 4, small voltage offsets were obtained. The realizations no. 1, 3, 5, 7 and 9 in Table 2 have transfer voltage bandwidths greater than 190 MHz. The current transfer characteristics were simulated with the Z terminal grounded, resulting in zero current offsets. **Fig. 15** shows the frequency response of the short circuit current transfer gain for the different OMA based CCII- realizations shown in Table 2. The realization no. 6 has the widest transfer current bandwidth.

5. Conclusion

The nullor and mirror elements properties are used to generate ideally equivalent building block representations. These representations can be implemented in different ways according to the grouping of the ideal elements used. The generation of CCII+ based and OMA based CCII- realizations is presented. It is demonstrated that the characteristics of the CCII- realizations depend on the actual behavior of the building block used in a particular realization. Many CCII- realizations feature high performance in terms of frequency response, voltage and current offsets, gain error and input impedance. In these realizations, the characteristics of the CCII- are improved compared to the building block used. Hence, in this case, the building block used to realize the CCII- need not to be optimized since the performance can be enhanced by using two units of the same building block. For example, in many OMA based realizations, the input impedance reduction can be achieved even if the transconductance gain of the OMA used is reduced. Although this paper is directed toward realizing the CCII-, the same nullor and mirror element properties can be used to generate equivalent realizations of other building blocks.

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