Int. J. Electron. Commun. (AEÜ) 64 (2010) 971–977

Contents lists available at ScienceDirect

Int. J. Electron. Commun. (AEÜ)

journal homepage: www.elsevier.de/aeue

Generation of CCII and ICCII based Wien oscillators using nodal admittance matrix expansion

Ahmed M. Soliman

Electronics and Communication Engineering Department, Faculty of Engineering, Cairo University, Egypt

ARTICLE INFO

Article history:
Received 16 July 2009
Accepted 22 August 2009

Keywords:
Nodal admittance matrix synthesis
Nullator
Norator
Pathological current and voltage mirrors
Oscillators

ABSTRACT

This paper introduces a new generation method of the grounded capacitor Wien oscillator circuits using current conveyors (CCII) or inverting current conveyors (ICCII) or combination of both of them. The nodal admittance matrix (NAM) of the single Op Amp Wien oscillator is taken as the starting point in the new approach of systematic synthesis of equivalent oscillators. The synthesis procedure is based on the generalized systematic synthesis framework using NAM expansion. The resulting derived 32 oscillators include many novel oscillators, using current conveyors or inverting current conveyors or both. Comparison between the generated oscillators based on the effect of parasitic elements on the oscillator performance is discussed.

1. Introduction

The first systematic synthesis of canonic oscillators using controlled sources was given in [1]. Most of the reported oscillators employ two floating capacitors except the circuits that belong to Wien oscillators employ one grounded capacitor and one floating capacitor. In [2] the design of single Op Amp single resistance controlled oscillators was given. Eight canonic circuits using five or six resistors each were given in [2], the two capacitors used are floating in all reported circuits except one which has one grounded capacitor and the other is floating. Due to the advantage of using grounded capacitors [3]. A systematic synthesis method was given in [4] to generate a set of tunable active RC oscillators each using two finite gain voltage controlled voltage sources, three resistors and two grounded capacitors.

Four alternative forms of the Wien bridge oscillator using a single Op Amp were given in [5], only one of them employ two grounded capacitors and is shown in Fig. 1.

After the introduction of the second generation current conveyor (CCII) [6], the first Wien oscillator with one grounded capacitor and one floating capacitor and using two CCII− was reported in [7].

A generation method for realizing grounded capacitors Wien oscillators using two CCII+ was introduced in [8].

The objective of this paper is to apply nodal admittance matrix (NAM) expansion to generate 32 oscillator circuits from the Wien circuit of Fig. 1 using CCII or inverting CCII (ICCII) [9] or combination of both.

2. Pathological elements

Recently, a symbolic framework for systematic synthesis of linear active circuits based on nodal admittance matrix (NAM) expansion was presented in [10–13]. The matrix expansion process begins by introducing blank rows and columns, representing new internal nodes, in the admittance matrix. Then, nullators and norators are used to move the resulting admittance matrix elements to their final locations, properly describing either floating or grounded passive elements. Thus, the final NAM is obtained including finite elements representing passive circuit components and unbounded elements, so called infinity-variables, representing nullators and norators. In this framework, nullators and norators [14] ideally describe active elements in the circuit are used. The nullator and norator are pathological or singular elements that possess ideal characteristics and are specified according to the constraints they impose on their terminal voltages and currents. For the nullator $V=I=0$, while the norator imposes no constraints on its voltage and current. A nullator–norator pair constitutes a universal active two-port network element called the nullor [14] and hence, nullator and norator are also called nullor elements. The attractive feature of the two nullor elements is their ability to model active circuits. Despite the ability of nullor elements to describe many active building blocks, they fail to represent devices like the CCII+ proposed in [6]. Other passive elements like resistors are combined with nullators and norators in order to obtain the nullor representation of the CCII+ [7]. In order to avoid the use of passive elements in the nullor representation of any building block, additional pathological elements called mirror elements were introduced in [15,16] to describe the voltage and current

E-mail address: asoliman@ieee.org

1434-8411/$ - see front matter © 2009 Elsevier GmbH. All rights reserved.
doi:10.1016/j.aeue.2009.08.003

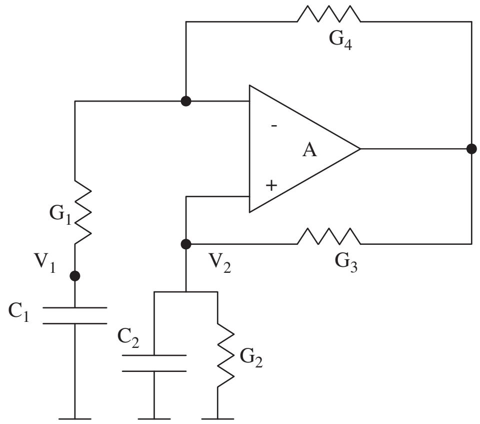

Fig. 1. Grounded capacitor Wien oscillator using Op Amp.

reversing actions. The voltage mirror (VM) is a lossless two-port network element used to represent an ideal voltage reversing action and it is described by

$$V_1 = -V_2 \tag{1a}$$

$$I_1 = I_2 = 0 \tag{1b}$$

The current mirror (CM) is a two-port network element used to represent an ideal current reversing action and it is described by

$$V_1 \text{ and } V_2 \text{ are arbitrary} \tag{1c}$$

$$I_1 = I_2 \text{and they are also arbitrary} \tag{1d}$$

Very recently the systematic synthesis method based on admittance matrix expansion using nullor elements [10–13] has been extended to accommodate mirror elements. This results in a generalized framework encompassing all pathological elements for ideal description of active elements [17–19]. Accordingly, more alternative realizations are possible and a wide range of active devices can be used in the synthesis procedure.

In this paper, the conventional systematic synthesis framework using admittance matrix expansion presented in [10–13] and [17–19] to synthesize oscillator circuits is presented.

3. Formulation of the NAM equation

The basic Op Amp oscillator circuit considered in this paper is the grounded capacitor Wien oscillator shown in Fig. 1 [5] having independent control on the condition of oscillation by varying a floating resistor. The state equations are descried by the following matrix equation:

$$\begin{bmatrix} C_1\frac{dv_1}{dt} \\ C_2\frac{dv_2}{dt} \end{bmatrix} = \begin{bmatrix} -G_1 & G_1 \\ -\frac{G_1G_3}{G_4} & -G_2+\frac{G_1G_3}{G_4} \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \end{bmatrix} \tag{2}$$

Taking the grounded capacitors as external circuit elements the NAM equation of the Op Amp circuit with the four resistors is given by

$$Y = \begin{bmatrix} G_1 & -G_1 \\ \frac{G_1G_3}{G_4} & G_2-\frac{G_1G_3}{G_4} \end{bmatrix} \tag{3}$$

The condition of oscillation is given by

$$\frac{R_1}{R_2}+\frac{C_2}{C_1}=\frac{R_4}{R_3} \tag{4a}$$

The condition of oscillation can be controlled by varying R_3 or R_4 without affecting the radian frequency of oscillation which is given by

$$\omega_O = \sqrt{\frac{G_1G_2}{C_1C_2}} \tag{4b}$$

4. Generation of type-A oscillators

Starting from Eq. (3) a family of four oscillators is generated in the following section. The condition of oscillation in the newly generated oscillators is controlled by a grounded resistor instead of a floating resistor in the circuit of Fig. 1.

4.1. Generation of type-A pathological circuit 1

Apply pivotal expansion [12] to the basic NAM Eq. (3) therefore

$$Y = \begin{bmatrix} G_1 & -G_1 & 0 \\ 0 & G_2 & -G_3 \\ G_1 & -G_1 & G_4 \end{bmatrix} \tag{5}$$

Adding a blank fourth row and fourth column, it is desirable to move $-G_1$ and $-G_1$ from the second column to the fourth column (since node 2 is connected to the grounded G_2 in parallel with the external C_2 and node 3 is connected to the grounded G_4). This is carried out using a nullator connected between nodes 2 and 4 as follows:

$$Y= \begin{bmatrix} G_1 & 0 & 0 & -G_1 \\ 0 & G_2 & -G_3 & 0 \\ G_1 & 0 & G_4 & -G_1 \\ 0 & 0 & 0 & 0 \end{bmatrix} \tag{6}$$

It is desirable to move G_1 and $-G_1$ from the third row to the fourth row with inverted signs so that a floating G_1 is to be realized between nodes 1 and 4. This is achieved using a CM connected between nodes 3 and 4 as follows:

$$Y= \begin{bmatrix} G_1 & 0 & 0 & -G_1 \\ 0 & G_2 & -G_3 & 0 \\ 0 & 0 & G_4 & 0 \\ -G_1 & 0 & 0 & G_1 \end{bmatrix} \tag{7}$$

Adding a fifth blank row and column, it is desirable to move $-G_3$ to the diagonal position 5, 5. This is carried out using a nullator connected between nodes 3 and 5 and a CM connected between nodes 2 and 5 as follows:

$$Y= \begin{bmatrix} G_1 & 0 & 0 & -G_1 & 0 \\ 0 & G_2 & 0 & 0 & 0 \\ 0 & 0 & G_4 & 0 & 0 \\ -G_1 & 0 & 0 & G_1 & 0 \\ 0 & 0 & 0 & 0 & G_3 \end{bmatrix} \tag{8}$$

Adding the capacitors C_1 and C_2 at nodes 1 and 2, respectively, the above equation is realized as shown in Fig. 2(a).

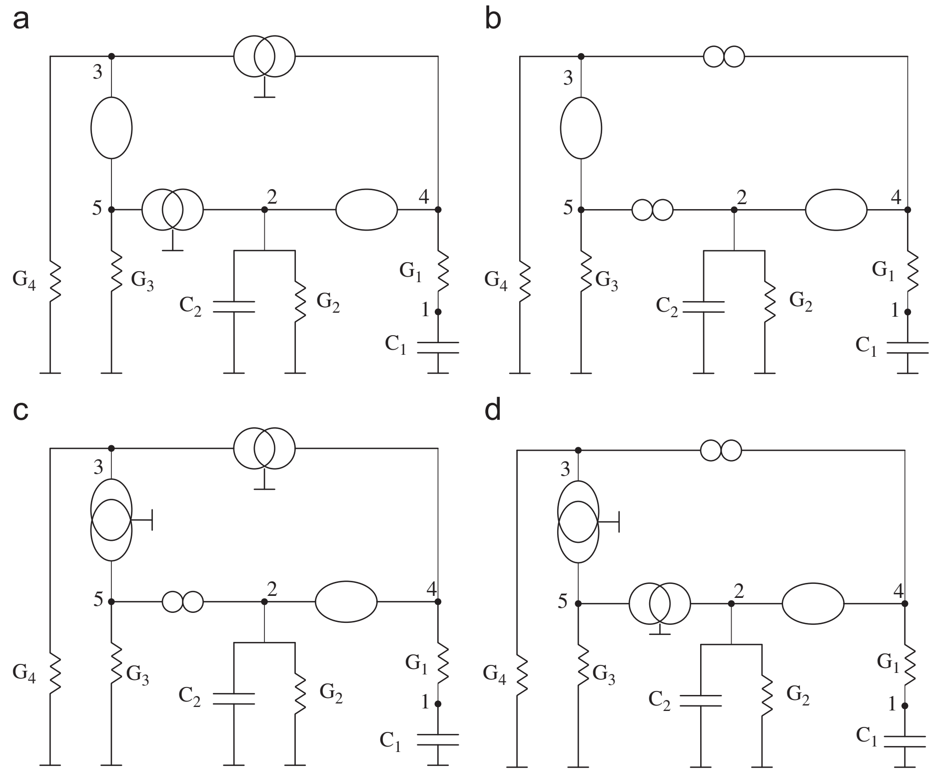

Fig. 2. Four alternative realizations of type A oscillators: (a) realization A-1, (b) realization A-2, (c) realization A-3, and (d) realization A-4.

4.2. Generation of type-A pathological circuit 2

Apply pivotal expansion to the basic NAM Eq. (3) in an alternative form from that given by Eq. (5) therefore

$$Y = \begin{bmatrix} G_1 & -G_1 & 0 \\ 0 & G_2 & G_3 \\ -G_1 & G_1 & G_4 \end{bmatrix} \tag{9}$$

Adding a blank fourth row and fourth column, it is desirable to move $-G_1$ and G_1 from the second column to the fourth column. This is carried out using a nullator connected between nodes 2 and 4 as follows:

$$Y = \begin{bmatrix} G_1 & 0 & 0 & -G_1 \\ 0 & G_2 & G_3 & 0 \\ -G_1 & 0 & G_4 & G_1 \\ 0 & 0 & 0 & 0 \end{bmatrix} \tag{10}$$

It is desirable to move $-G_1$ and G_1 from the third row to the fourth row so that a floating G_1 is to be realized between nodes 1 and 4. This is achieved using a norator connected between nodes 3 and 4 as follows:

$$Y = \begin{bmatrix} G_1 & 0 & 0 & -G_1 \\ 0 & G_2 & G_3 & 0 \\ 0 & 0 & G_4 & 0 \\ -G_1 & 0 & 0 & G_1 \end{bmatrix} \tag{11}$$

Adding a fifth blank row and column, it is desirable to move G_3 to the diagonal position 5, 5. This is carried out using a nullator connected between nodes 3 and 5 and a norator connected between nodes 2 and 5 as follows:

$$Y = \begin{bmatrix} G_1 & 0 & 0 & -G_1 & 0 \\ 0 & G_2 & 0 & 0 & 0 \\ 0 & 0 & G_4 & 0 & 0 \\ -G_1 & 0 & 0 & G_1 & 0 \\ 0 & 0 & 0 & 0 & G_3 \end{bmatrix} \tag{12}$$

Adding the capacitors C_1 and C_2 at nodes 1 and 2, respectively, the above equation is realized as shown in Fig. 2(b).

4.3. Generation of type-A pathological circuit 3

Starting from Eq. (7) and adding a fifth blank row and column, it is desirable to move $-G_3$ to the diagonal position 5, 5. This is carried out using a VM connected between nodes 3 and 5 and a norator connected between nodes 2 and 5 as follows:

$$Y = \begin{bmatrix} G_1 & 0 & 0 & -G_1 & 0 \\ 0 & G_2 & 0 & 0 & 0 \\ 0 & 0 & G_4 & 0 & 0 \\ -G_1 & 0 & 0 & G_1 & 0 \\ 0 & 0 & 0 & 0 & G_3 \end{bmatrix} \tag{13}$$

Adding the capacitors C_1 and C_2 at nodes 1 and 2, respectively, the above equation is realized as shown in Fig. 2(c).

4.4. Generation of type-A pathological circuit 4

Starting from Eq. (11) and adding a fifth blank row and column, it is desirable to move G_3 to the diagonal position 5, 5. This is carried out using a VM connected between nodes 3 and 5 and a CM connected between nodes 2 and 5 as follows:

$$Y=\begin{bmatrix} G_1 & 0 & 0 & -G_1 & 0 \\ 0 & G_2 & 0 & 0 & 0 \\ 0 & 0 & G_4 & 0 & 0 \\ -G_1 & 0 & 0 & G_1 & 0 \\ 0 & 0 & 0 & 0 & G_3 \end{bmatrix} \tag{14}$$

Adding the capacitors C_1 and C_2 at nodes 1 and 2, respectively, the above equation is realized as shown in Fig. 2(d).

5. Generation of type-B oscillators

The following NAM equation which also results in Eqs. (4a) and (4b) is used as the key equation in the realizations of the following four equivalent oscillator circuits and classified as type-B:

$$Y=\begin{bmatrix} G_1 & G_1 \\ -\dfrac{G_1G_3}{G_4} & G_2-\dfrac{G_1G_3}{G_4} \end{bmatrix} \tag{15}$$

It should be noted that the above equation is obtained from Eq. (3) by interchanging the signs of the elements in the 1, 2 and 2, 1 positions. This will not affect the condition of oscillation or the frequency of oscillation.

The above equation, however, cannot be realized as an Op Amp Wien oscillator.

5.1. Generation of type-B pathological circuit 1

Apply pivotal expansion to the basic NAM Eq. (15) therefore

$$Y=\begin{bmatrix} G_1 & G_1 & 0 \\ 0 & G_2 & -G_3 \\ -G_1 & -G_1 & G_4 \end{bmatrix} \tag{16}$$

Adding a blank fourth row and fourth column, it is desirable to move G_1 and $-G_1$ from the second column to the fourth column to become $-G_1$ and G_1, respectively. This is carried out using a VM connected between nodes 2 and 4 as follows:

$$Y=\begin{bmatrix} G_1 & 0 & 0 & -G_1 \\ 0 & G_2 & -G_3 & 0 \\ -G_1 & 0 & G_4 & G_1 \\ 0 & 0 & 0 & 0 \end{bmatrix} \tag{17}$$

It is desirable to move $-G_1$ and G_1 from the third row to the fourth row so that a floating G_1 is to be realized between nodes 1 and 4. This is achieved using a norator connected between nodes 3 and 4 as follows:

$$Y=\begin{bmatrix} G_1 & 0 & 0 & -G_1 \\ 0 & G_2 & -G_3 & 0 \\ 0 & 0 & G_4 & 0 \\ -G_1 & 0 & 0 & G_1 \end{bmatrix} \tag{18}$$

Adding a fifth blank row and column, it is desirable to move $-G_3$ to the diagonal position 5, 5. This is carried out using a VM connected between nodes 3 and 5 and a norator connected between nodes 2 and 5 as follows:

$$Y=\begin{bmatrix} G_1 & 0 & 0 & -G_1 & 0 \\ 0 & G_2 & 0 & 0 & 0 \\ 0 & 0 & G_4 & 0 & 0 \\ -G_1 & 0 & 0 & G_1 & 0 \\ 0 & 0 & 0 & 0 & G_3 \end{bmatrix} \tag{19}$$

Adding the capacitors C_1 and C_2 at nodes 1 and 2, respectively, the above equation is realized as shown in Fig. 3(a).

5.2. Generation of type-B pathological circuit 2

Apply pivotal expansion to the basic NAM Eq. (15) therefore

$$Y=\begin{bmatrix} G_1 & G_1 & 0 \\ 0 & G_2 & G_3 \\ G_1 & G_1 & G_4 \end{bmatrix} \tag{20}$$

Adding a blank fourth row and fourth column, it is desirable to move G_1 and G_1 from the second column to the fourth column to become $-G_1$ and $-G_1$, respectively. This is carried out using a VM connected between nodes 2 and 4 as follows:

$$Y=\begin{bmatrix} G_1 & 0 & 0 & -G_1 \\ 0 & G_2 & G_3 & 0 \\ G_1 & 0 & G_4 & -G_1 \\ 0 & 0 & 0 & 0 \end{bmatrix} \tag{21}$$

It is desirable to move G_1 and $-G_1$ from the third row to the fourth row with opposite signs so that a floating G_1 is to be realized between nodes 1 and 4. This is achieved using a CM connected between nodes 3 and 4 as follows:

$$Y=\begin{bmatrix} G_1 & 0 & 0 & -G_1 \\ 0 & G_2 & G_3 & 0 \\ 0 & 0 & G_4 & 0 \\ -G_1 & 0 & 0 & G_1 \end{bmatrix} \tag{22}$$

Adding a fifth blank row and column, it is desirable to move G_3 to the diagonal position 5, 5. This is carried out using a VM connected between nodes 3 and 5 and a CM connected between nodes 2 and 5 as follows:

$$Y=\begin{bmatrix} G_1 & 0 & 0 & -G_1 & 0 \\ 0 & G_2 & 0 & 0 & 0 \\ 0 & 0 & G_4 & 0 & 0 \\ -G_1 & 0 & 0 & G_1 & 0 \\ 0 & 0 & 0 & 0 & G_3 \end{bmatrix} \tag{23}$$

Adding the capacitors C_1 and C_2 at nodes 1 and 2, respectively, the above equation is realized as shown in Fig. 3(b).

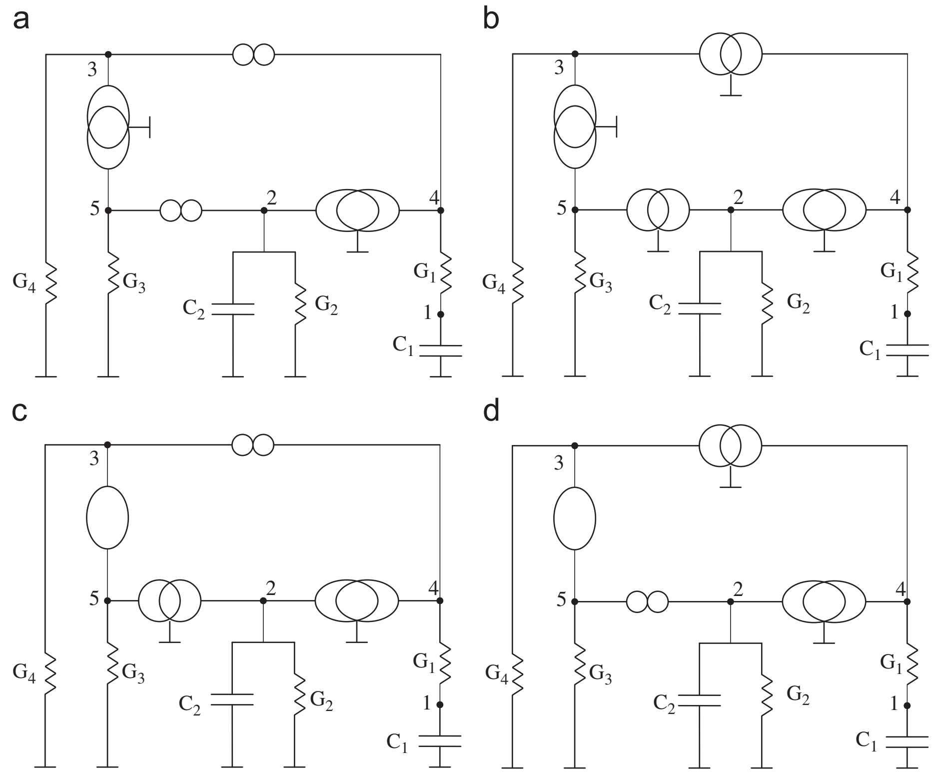

Fig. 3. Four alternative realizations of type B oscillators: (a) realization B-1, (b) realization B-2, (c) realization B-3, and (d) realization B-4.

5.3. Generation of type-B pathological circuit 3

Starting from Eq. (16) and following successive steps the following NAM is obtained:

$$Y=\begin{bmatrix} G_1 & 0 & 0 & -G_1 & 0 \\ 0 & G_2 & 0 & 0 & 0 \\ 0 & 0 & G_4 & 0 & 0 \\ -G_1 & 0 & 0 & G_1 & 0 \\ 0 & 0 & 0 & 0 & G_3 \end{bmatrix} \quad (24)$$

Adding the capacitors C_1 and C_2 at nodes 1 and 2, respectively, the above equation is realized as shown in Fig. 3(c).

5.4. Generation of type-B pathological circuit 4

Starting from Eq. (20) and following successive steps the following NAM is obtained:

$$Y=\begin{bmatrix} G_1 & 0 & 0 & -G_1 & 0 \\ 0 & G_2 & 0 & 0 & 0 \\ 0 & 0 & G_4 & 0 & 0 \\ -G_1 & 0 & 0 & G_1 & 0 \\ 0 & 0 & 0 & 0 & G_3 \end{bmatrix} \quad (25)$$

Adding the capacitors C_1 and C_2 at nodes 1 and 2, respectively, the above equation is realized as shown in Fig. 3(d).

6. The CCII and ICCII oscillator circuits

The eight generated circuits based on the use of pathological elements and shown in Figs. 2 and 3 can lead to the following four

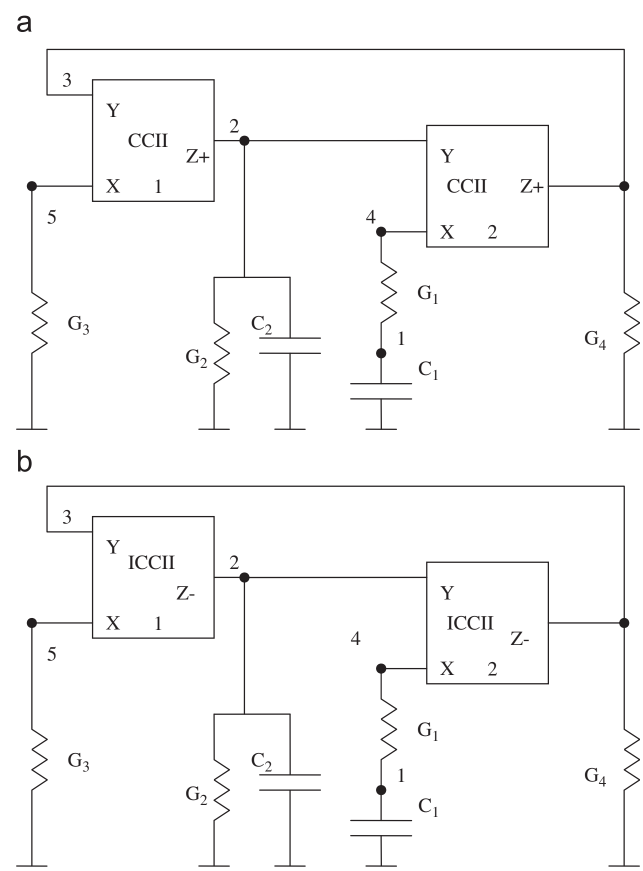

Fig. 4. (a) Realization of class-I type A circuit from Fig. 2(a) and (b) realization of class I type B circuit from Fig. 3(a).

classes of circuits based on alternative pairing of the pathological elements.

6.1. Class I oscillator circuits

This class includes eight CCII and ICCII circuits obtained from Figs. 2 and 3 by taking nodes 3, 5, 2 to represent *Y*, *X* and *Z* terminals of conveyor 1 and nodes 2, 4, 3 to represent *Y*, *X* and *Z* terminals of conveyor 2. For example the circuit of Fig. 2(a) is realized by two, CCII+ as shown in Fig. 4(a) and the circuit of Fig. 3(a) is realized by two ICCII− as shown in Fig. 4(b). Similarly the other six CCII and ICCII circuits can be obtained from Figs. 2b, c, d, and Figs. 3b, c, d, and are not included here to limit the paper length.

It is seen that the parasitic resistance R_{X1} can be compensated by subtracting its value from the design value of R_3. The parasitic resistance R_{X2} can be compensated by subtracting its value from the design value of R_1. The parasitic capacitance C_{z1} can be compensated by subtracting its value from the design value of C_2.

The only parasitic element which affects the circuit is C_{Z2} as it acts in parallel with R_4 and it has a very minor effect. It can be shown that the effect of the parasitic capacitance C_{Z2} can be minimized by taking $C_{Z2}\,R_4$ much less than C_1R_1 and C_2R_2.

6.2. Class II oscillator circuits

This class includes eight CCII and ICCII circuits obtained from Figs. 3 and 4 by taking nodes 4, 2, 5 to represent *Y*, *X* and *Z* terminals of conveyor 1 and nodes 5, 3, 4 to represent *Y*, *X* and *Z* terminals of conveyor 2. For example the circuit of Fig. 3(a) is realized by two CCII+ as shown in Fig. 5(a) and the circuit of Fig. 4(a) is realized by two ICCII− as shown in Fig. 5(b). Similarly the other six CCII and ICCII circuits can be obtained from Figs. 2b, c, d, and Figs. 3b, c, d.

It is seen that the only parasitic element that can be compensated is parasitic resistance R_{X2} by subtracting its value from the design value of R_4. The three other parasitic elements namely R_{X1}, C_{Z1} and C_{Z2} are affecting the circuit operation.

It should be noted that pairing the pathological elements resulting in class II circuits is more sensitive to parasitic element effects than the alternative pairing resulting in class I circuits.

6.3. Class III oscillator circuits

The third class of oscillator circuits is generated from class I by applying the adjoint network theorem [20–23]. Although the adjoint network theorem is intended to convert voltage mode to current mode circuits it is also applicable to oscillator circuits. Applying the adjoint network theorem to class I oscillators by replacing the nullator by a norator and the current mirror by a voltage mirror and vice versa [9] the circuits of class III are obtained. For example using the above transformation rule Fig. 6(a) is obtained as the adjoint of Fig. 2(a). Fig. 6(b) is obtained from Fig. 6(a) by taking nodes 2, 5, 3 to represent *Y*, *X* and *Z* terminals of the first ICCII− and nodes 3, 4, 2 to represent *Y*, *X* and *Z* terminals of the second ICCII−.

It is seen that the parasitic resistance R_{X1} can be compensated by subtracting its value from the design value of R_3. The parasitic resistance R_{X2} can be compensated by subtracting its value from

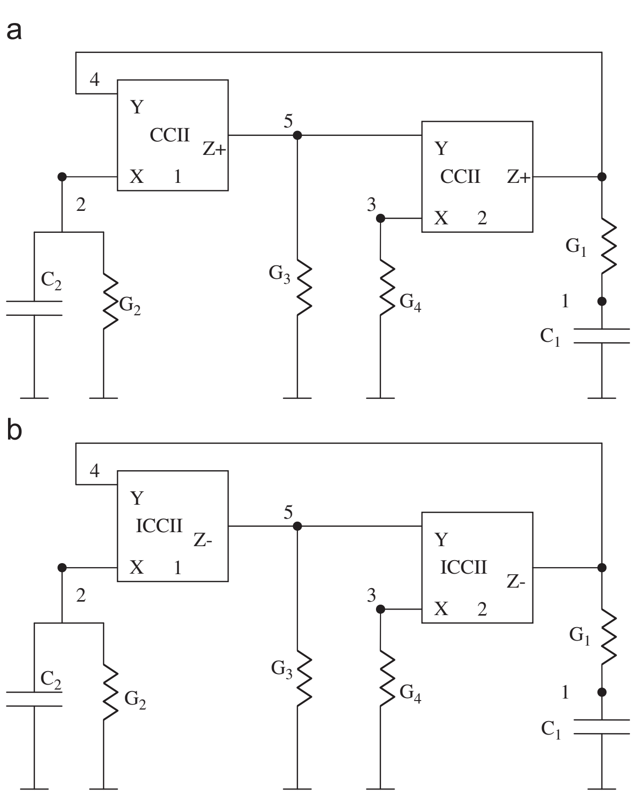

Fig. 5. (a) Realization of class II type A circuit from Fig. 2(a) and (b) realization of class II type B circuit from Fig. 3(a).

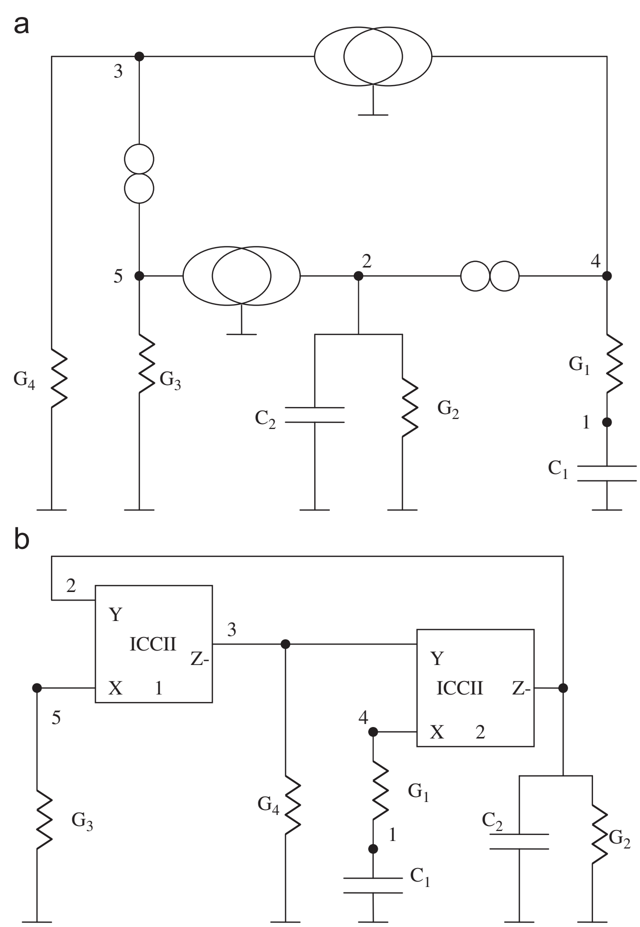

Fig. 6. (a) Adjoint circuit to the circuit of Fig. 2(a) and (b) realization of class III type A circuit from Fig. 6(a).

the design value of R_1. The parasitic capacitance C_{z2} can be compensated by subtracting its value from the design value of C_2.

The only parasitic element which affects the circuit is C_{Z1} as it acts in parallel with R_4.

6.4. Class IV oscillator circuits

The fourth class of oscillator circuits is generated from class II by applying the adjoint network theorem or from class III by alternative pairing of pathological elements.

7. Conclusions

A new generation method of the grounded capacitor Wien oscillator circuits using CCII or ICCII or combination of both of them is introduced. The NAM of the single Op Amp Wien oscillator is taken as the starting point in the new approach of systematic synthesis of equivalent oscillators. The synthesis procedure is based on the generalized systematic synthesis framework using NAM expansion.

Four classes are defined and each class includes eight circuits. The resulting derived 32 oscillators include many novel oscillators, using various types of current conveyors and inverting current conveyors. Comparison between the generated oscillators based on the effect of parasitic elements on the oscillator performance indicated that classes I and III are affected only by one parasitic capacitance and are superior to classes II and IV affected by the two parasitic capacitances and one parasitic resistance R_X.

It should also be noted that a two CCII− and a two CCII+ circuits with similar topology was published in [24] and [25], respectively; however, no generation method was given in both of them. The two CCII+ circuits reported in [8] are generated from the Op Amp Wien oscillators but using alternative generation method different from the NAM expansion generation procedure given in this paper. Finally it should be noted that the circuit of Fig. 4(a) is identical to Fig. 4(b) in [8] except a third capacitor is used in [8] to provide independent control on the radian frequency of operation.

References

[1] Bhattacharyya BB, Sundaramurthy M, Swamy MNS. Systematic generation of canonic sinusoidal RC active oscillators. IEE Proceedings 1981;128:114–26.
[2] Boutin N. On the identification and design of single amplifier single resistance controlled oscillators. IEEE Transactions on Circuits and Systems 1984;31:1046–9.
[3] Bhushan M, Newcomb RW. Grounding of capacitors in integrated circuits. Electronics Letters 1967;3:148–9.
[4] Bhattacharyya BB, Sundaramurthy M, Swamy MNS. Realization of tunable RC-active oscillators using grounded capacitors and voltage amplifiers. International Journal of Circuit Theory and Applications 1980;8:355–71.
[5] Boutin N. Two new single op-amp RC Bridget T oscillator circuits. IEE Proceedings 1983;130:222–4.
[6] Sedra AS, Smith KC. A second generation current conveyor and its applications. IEEE Transactions on Circuit Theory 1970;17:132–4.
[7] Svoboda JA. Current conveyors operational amplifiers and nullors. IEE Proceedings 1989;136:317–22.
[8] Soliman AM. Novel generation method of current mode Wien type oscillators using current conveyors. International Journal of Electronics 1998;85:737–47.
[9] Awad IA, Soliman AM. Inverting second generation current conveyors: the missing building blocks, CMOS realizations and applications. International Journal of Electronics 1999;86:413–32.
[10] Haigh DG, Clarke TJW, Radmore PM. Symbolic framework for linear active circuits based on port equivalence using limit variables. IEEE Transactions on Circuits and Systems I 2006;53:2011–24.
[11] Haigh DG. A method of transformation from symbolic transfer function to active-RC circuit by admittance matrix expansion. IEEE Transactions on Circuits and Systems I 2006;53:2715–28.
[12] Haigh DG, Tan FQ, Papavassiliou C. Systematic synthesis of active-RC circuit building-blocks. Analog Integrated Circuits and Signal Processing 2005;43:297–15.
[13] Haigh DG, Radmore PM. Admittance matrix models for the nullor using limit variables and their application to circuit design. IEEE Transactions on Circuits and Systems I 2006;53:2214–23.
[14] Carlin HJ. Singular network elements. IEEE Transactions on Circuit Theory 1964;11:67–72.
[15] Awad IA, Soliman AM. On the voltage mirrors and the current mirrors. Analog Integrated Circuits and Signal Processing 2002;32:79–81.
[16] Awad IA, Soliman AM. A new approach to obtain alternative active building blocks realizations based on their ideal representations. Frequenz 2000;54:290–9.
[17] Saad RA, Soliman AM. Generation, modeling, and analysis of CCII-Based gyrators using the generalized symbolic framework for linear active circuits (p n/a). International Journal of Circuit Theory and Applications 2008;36:289–309.
[18] Saad RA, Soliman AM. Use of mirror elements in the active device synthesis by admittance matrix expansion. IEEE Transactions on Circuits and Systems I 2008;55:2726–35.
[19] Saad RA, Soliman AM. A new approach for using the pathological mirror elements in the ideal representation of active devices. International Journal of Circuit Theory and Application 2008, online doi:10.1002/cta.534.
[20] Director SW, Rohrer RA. The generalized adjoint network and network sensitivities. IEEE Transactions on Circuit Theory 1969;16:318–23.
[21] Bhattacharyya BB, Swamy MNS. Network transposition and its application in synthesis. IEEE Transactions on Circuit Theory 1971;18:394–7.
[22] Roberts GW, Sedra AS. All current-mode selective circuits. Electronics Letters 1989;25:759–61.
[23] Carlosena A, Moschytz GS. Nullators and norators in voltage to current mode transformations. International Journal of Circuit Theory and Applications 1993;21:421–4.
[24] Abuelmatti MT, Al-Ghumaiz AA, Khan MH. Novel CCII – single element controlled oscillators employing grounded resistance and capacitors. International Journal of Electronics 1995;78:1107–12.
[25] Ben Salem S, Fakhfakh M, Masmoudi D, Loulou M, Loumeau P, Masmoudi N. A high performance CMOS CCII and high frequency applications. Analog Integrated Circuits and Signal Processing 2006;49:71–8.

Ahmed M. Soliman was born in Cairo, Egypt, on November 22, 1943. He received the B.Sc. degree with honors from Cairo University, Cairo, Egypt, in 1964, the M.S. and Ph.D. degrees from the University of Pittsburgh, Pittsburgh, PA, U.S.A., in 1967 and 1970, respectively, all in electrical engineering.

He is currently Professor, Electronics and Communications Engineering Department, Cairo University, Egypt.

From September 1997 to September 2003, Dr. Soliman served as Professor and Chairman Electronics and Communications Engineering Department, Cairo University, Egypt.

From 1985 to 1987, Dr. Soliman served as Professor and Chairman of the Electrical Engineering Department, United Arab Emirates University, and from 1987 to 1991 he was the Associate Dean of Engineering at the same University.

He has held visiting academic appointments at San Francisco State University, Florida Atlantic University and the American University in Cairo.

He was a visiting scholar at Bochum University, Germany (Summer 1985) and with the Technical University of Wien, Austria (Summer 1987).

In 1977, Dr. Soliman was decorated with the First Class Science Medal, from the President of Egypt, for his services to the field of engineering and engineering education.

Dr. Soliman is a Member of the Editorial Board of the IET Proceedings Circuits, Devices and Systems.

Dr. Soliman is a Member of the Editorial Board of Research Letters in Electronics.

Dr. Soliman is a Member of the Editorial Board of Analog Integrated Circuits and Signal Processing.

Dr. Soliman is also a Member of the Editorial Board of Scientific Research and Essays.

Dr. Soliman served as Associate Editor of the IEEE Transactions on Circuits and Systems I (Analog Circuits and Filters) from December 2001 to December 2003 and is an Associate Editor of the Journal of Circuits, Systems and Signal Processing from January 2004 till now.