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CMOS-CCII Realizations Based on the Differential Amplifier: A Review

CMOS-CCII-Schaltungsrealisierungen mit Differentialverstärkern, ein Überblick

Abstract
An analysis of five CMOS realizations of the current conveyor of the second generation type (CCII) all based on the Long Tail differential Pair (LTP) is presented and PSpice simulations are compared. The different advantages observed in these realizations are discussed. It is also shown that the fifth realization, which is proposed in this paper, offers an improvement in the bandwidth extent, which makes it suitable to operate in high frequency applications.

Übersicht
Eine Analyse von fünf CMOS-Schaltungsrealisierungen des Stromübertragers der zweiten Generation (CCII), alle basierend auf einer Differentialverstärkerschaltung (LTP) wird vorgestellt. Ihre PSpice-Simulationsergebnisse werden verglichen. Die hierbei sichtbaren unterschiedlichen Vorteile werden diskutiert. Es wird ferner gezeigt, daß die fünfte in dieser Arbeit vorgeschlagene Realisierung eine größere Bandbreite und damit Anwendungen in der Hochfrequenztechnik bietet.

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Für die Dokumentation
CMOS-Analogschaltungen / Stromübertrager

1. Introduction

Since its conception, the second generation current conveyor (CCII) has proven to be an exceptionally versatile current mode building block that can be implemented as several functional circuits, a current amplifier, current integrator, and current summer [1-12]. The CCII is a three-port network with a describing matrix of the form

$$\begin{bmatrix} V_X \\ I_Y \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 \\ 0 & 0 & 0 \\ K & 0 & 0 \end{bmatrix} \begin{bmatrix} I_X \\ V_Y \\ V_Z \end{bmatrix} \quad (1)$$

K determines the polarity of the conveyor, for,
$K = 1$, the conveyor is a CCII+, and for
$K = -1$, the conveyor is a CCII-

Throughout this paper, the abbreviation CCII will be used instead of CCII+ for simplicity. Several CMOS realizations of the CCII have been reported in the literature [2-8]. Recently, current-mode circuits have received a great interest since they are suitable to operate under low voltage supplies since the current mode substitutes current swings for voltage swings in signal propagation.

Key performance features of current-mode signal processing are wideband capability and a wide dynamic range under low power operation. To exploit such potentials of current-mode signal processing, the CCII derived from the first generation current conveyor reported in [2] is based on the translinear loop and has prototyped many innovative designs that are simple and offer an excellent current following action over a wide bandwidth. However, it suffers from gain inaccuracy due to area mismatch between the input and the output transistors of the current mirror. Besides, the voltage following action is inaccurate and there is a DC offset. To overcome these problems, a very promising technique to implement CCII consists of a feedback-stabilized voltage follower has been proposed [3]. This technique employs a high open loop amplification in order to reduce the DC offset and the input resistance of the CCII. Several accurate implementations in the literature have followed this op-amp based architecture [4-6].

The purpose of this paper is to examine a group of different CMOS CCII circuits based on this technique and to compare their performances. All these circuits are based on the use of the Long Tail differential Pair (LTP) as the source of transconductance gain due its high frequency response and its immunity to some second-order effects that might reflect on the offset voltage like the body-effect. The comparison is made on the basis that for all structures the MOS models are identical, the aspect ratios for equivalent transistors are equal, the power supplies are the same and all devices are matched. The principle of operation for each CCII circuit will be described, these are designated: the first CMOS CCII realization reported by Surakampontorn et al. [3], the second realization reported by Liu et al. [4], the third realization reported by Palmisano and Palumbo [5], the fourth realization reported by Ismail and Soliman CCII [6] and finally a new proposed CCII optimized to operate in high frequency applications. Frequency compensation techniques [13] are not used in these circuits in order to obtain a fair comparison between different topologies since they can be applied to any one of them.

2. Circuit Description

2.1. First CMOS CCII realization

The CMOS realization of the CCII proposed in [3] is shown in **Fig. 1**. The structure is based on the differential pair transistors M1 and M2. It is assumed that M1-M2, M4-M5, M7-M8 and M9-M10 are well matched, and that all transistors are operating in the

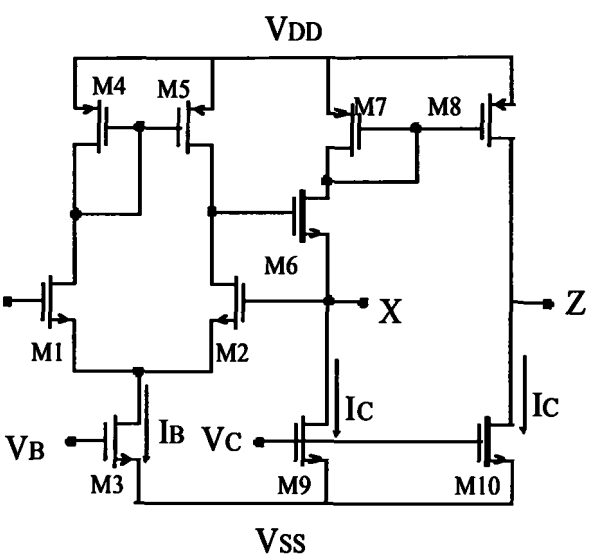

Fig. 1: First CCII realization (Surakampontorn et al. CCII [3])

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saturation region. Transistor M6 is connected as a source follower implying a negative feedback action on the differential pair. Consequently, due to this high open loop gain, the voltage at X follows successfully the voltage at Y and the resistance seen at X is very small. However, in a practical realization, several non-idealities contribute to errors from the ideal performance. The major factors that will be considered are the finite transconductance value of the transistor g_m, and the channel length modulation effect introduced as a finite drain to source transconductance g_{ds} of the MOS transistors.

Accordingly, the voltage transfer function from the node Y to the node X is obtained as:

$$A_v = \frac{V_X}{V_Y} \approx \frac{2g_{m1}}{\left(2g_{m1} + g_{d2} + g_{d5}\right)} \tag{2}$$

and the resistance seen at the node X when the nodes Y and Z are grounded is given by:

$$r_x \approx \frac{\left(g_{d2} + g_{d5}\right)}{g_{m6}\left(2g_{m1} + g_{d2} + g_{d5}\right)}. \tag{3}$$

Since the current is conveyed from the node X to the node Z through simple current mirrors, it is clear that the resistance seen at the node Z is given by:

$$r_Z \approx \frac{1}{\left(g_{d8} + g_{d10}\right)}. \tag{4}$$

From (3) and (4), it follows that r_X is very small and V_X follows exactly V_Y despite the low number of transistors. However, the circuit suffers from low current driving capability and limited input voltage range especially under reduced supply voltages.

Concerning the high frequency response, the major high frequency limitation is due to the stray capacitances at the nodes X and Z. When studying the case of CCII-based voltage amplifier, i.e. two grounded resistances are connected to the nodes X and Z respectively, one can note that, considering only the gate-source capacitances of the transistors M2 and M6 in the voltage follower section of the CCII, one dominant pole w_p and one dominant zero w_z are obtained such that

$$w_z = \frac{g_{m2}g_{m6}}{C_2(g_{d2} + g_{d4}) + C_6 g_{m2}} \tag{5}$$

$$w_p = \frac{g_{m2}g_{m6}}{\left(C_2 + C_6\right)(g_{d2} + g_{d4}) + C_6 g_{m2}} \tag{6}$$

where C_2 and C_6 are the gate-to-source capacitances of the transistors M2 and M6 respectively. It is clear that, in this feedback-stabilized voltage follower, these frequencies are quite high and will not be the major high frequency limitation [3]. This is clear due to the high Gain Bandwidth product delivered by the op-amp like architecture [14]. However, when studying the current-follower section between X and Z, the time constant due to the PMOS current mirror M7-M8 is of remarkable value and the dominant pole w_{p2} is given by

$$w_{p2} = \frac{g_{m7}}{\left(C_7 + C_8\right)} \tag{7}$$

where C_7 and C_8 are the gate-to-source capacitances of the transistors M7 and M8 respectively. Surely, this pole is the high frequency limitation of the circuit specially that in CMOS technology, the value of g_m is relatively low and gate-to-source capacitances are high when compared to bipolar technologies putting a limitation on the wideband capabilities of such architectures implemented in CMOS. In order to obtain a common figure of merit, all the used PMOS transistors in this paper (except those of the final circuit) are taken with equal aspect ratios. By this way it can be assumed that the current following action is almost the same in all these circuits. Consequently, the high frequency pole due to the current following action for each topology will be estimated in terms of g_m and C_{GS}, the transconductance and the gate-to-source capacitance of the PMOS transistors respectively. Therefore the high frequency pole of this topology will be simplified to

$$w_p \approx \frac{g_m}{2C_{GS}}. \tag{8}$$

2.2. Second CMOS CCII realization

The simplified CMOS realization of the CCII+ proposed in [4] is shown in **Fig. 2.** (the cascading has been removed and ordinary current mirrors were used instead of the CCI cells in order to maintain fair tradeoffs for comparison). In this case an inverting output stage (transistor M6 and M8) were used to stabilize the long tail differential pair M1 and M2. One advantage of this stage is that it can give a larger open loop gain in addition to the ordinary buffering action performed by the source follower in section 2.1. To maintain stability, the feedback action was made on the positive input port of the differential pair (Port X in this case).

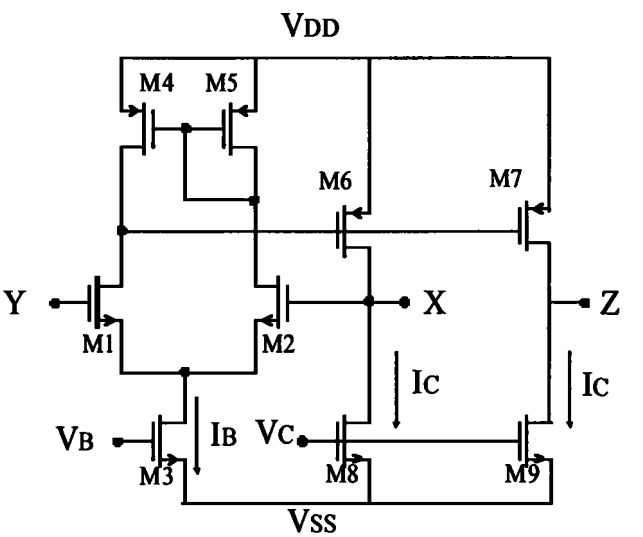

Fig. 2: Second CCII realization (Liu et al. CCII [4])

The voltage transfer function from the node Y to the node X is then obtained as

$$A_v \approx \frac{2g_{m1}g_{m6}}{2g_{m1}g_{m6} + \left(g_{d1} + g_{d4}\right)\left(g_{d6} + g_{d8}\right)} \tag{9}$$

and the resistance seen at the node X is given by

$$r_x \approx \frac{\left(g_{d1} + g_{d4}\right)}{2g_{m1}g_{m6} + \left(g_{d1} + g_{d4}\right)\left(g_{d6} + g_{d8}\right)}. \tag{10}$$

From (9) and (10) it is clear that the voltage follower section of the circuit gives a remarkable performance. Following the same analysis given in the previous section, it can be concluded that r_Z is the same. As for the high frequency pole, it is given by:

$$w_p \approx \frac{g_m}{2C_{GS}} \tag{11}$$

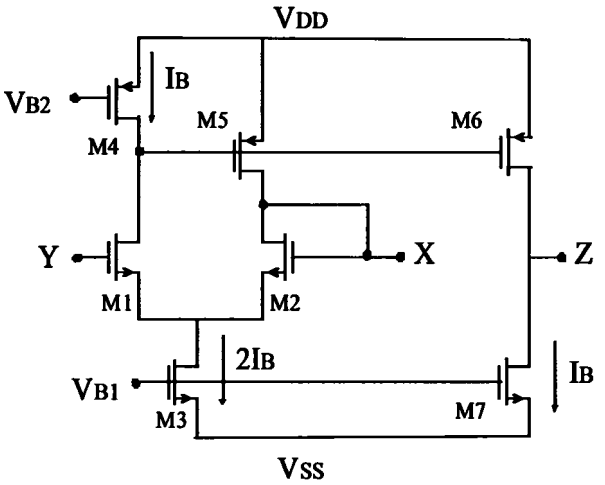

Fig. 3: Third CCII realization (Palmisano and Palumbo CCII [5])

which is the same as that of the circuit of Fig. 1.

2.3. Third CMOS CCII realization

The CMOS realization of the CCII proposed in [5] is shown in **Fig. 3**. Transistors M1-M5 perform a unity-gain amplifier and transistors M6 and M7 implement a common source amplifier. Setting $I_3 = 2I_4$, the negative feedback action on the gate of the transistor M2 makes the gate-source voltages of M1 and M2 equal and always fixed to their quiescent value. Therefore, V_X follows V_Y with success. It is clear that this realization offers a relatively high gain despite the low number of transistors. The voltage transfer function from the node Y to the node X is then obtained as

$$A_v \approx \frac{g_{m1}}{\left(g_{m1}+g_{d2}+g_{d5}\right)} \tag{12}$$

and the resistance seen at the node X is given by

$$r_X \approx \frac{(g_{d1}+2g_{d4})}{g_{m1}g_{m5}+g_{m2}(g_{d1}+g_{d4})}. \tag{13}$$

As for the current-follower section, no change is made from the previous two topologies (the same r_Z and high frequency pole).

2.4. Fourth CMOS CCII realization

The circuit configuration of the CCII reported in [6] is shown in **Fig. 4**. It consists mainly of two matched differential pairs (M1-M3 and M2-M4). It can be easily noted that the transistors (M3-M6) form the first generation current conveyor (CCI) introduced in [2]. So the voltage from the source of the transistor M4 is conveyed to the source of the transistor M3 and the current from the transistor M5 to the transistor M6, thus the voltage V_Y applied to the gate of M1 does not affect the current flowing in M4 since the latter follows the current flowing in M3, and since the sources of transistors M1 and M2 have the same voltage (due to the action of the CCI) and carry the same current (since the currents in M3 and M4 are equal), the voltage at the node Y is conveyed to the node X with success. The current coming from X can be reproduced at Z by the action of the current mirror (M7-M8).

The voltage transfer function is given by

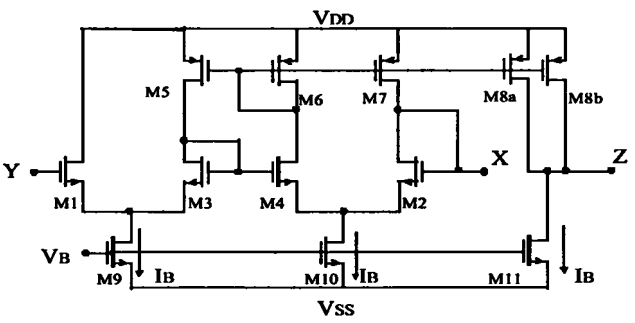

Fig. 4: Fourth CCII realization (Ismail and Soliman CCII [6])

$$A_v \approx \frac{\dfrac{2g_{m1}^2}{(g_{d3}+g_{d5})(g_{d2}+g_{d7})}}{\left(1+2g_{m1}\dfrac{1}{(g_{d2}+g_{d7})}\left(1+g_{m1}\dfrac{1}{(g_{d3}+g_{d5})}\right)\right)}. \tag{14}$$

The resistance r_X at node X is

$$r_X \approx \frac{\left(g_{d3}+g_{d5}\right)}{\left(g_{d2}+g_{d7}\right)\left(g_{d2}+g_{d7}\right)+2g_{m1}(g_{d3}+g_{d5}+g_{m1})}. \tag{15}$$

Obviously, the high open loop gain obtained results in a very small r_X and V_X follows exactly V_Y [4]. However, in this topology, the high frequency pole due to the current following section is most serious due to the extended current mirror used. Therefore, the pole introduced by the PMOS current mirror is approximately given by

$$w_p \approx \frac{g_m}{5C_{GS}} \tag{16}$$

which represents the price paid for an increased open loop gain in the voltage follower section.

2.5. Proposed CCII for high frequency applications

The use of PMOS current mirrors in the current-follower section of the CCII results usually in an inaccurate current following action because of area mismatch and a relatively limited frequency response [7]. As shown in previous sections, the current following accuracy is generally controlled by a careful design of the current mirrors. Usually, this leads to the use of PMOS transistors with long channels and to introduce cascaded transistors. In addition, the current driving capability of these mirrors must be insured by enlarging the aspect ratios of these transistors. Consequently, large gate-to-source capacitances are expected to be seen which reflects a serious high frequency pole limitation. The Floating Current Source (FCS) proposed in [7] gives an elegant solution to replace the PMOS current mirrors in the current following section but only for the CCII- circuits. All the reported circuits implementing the op-amp architecture based CCII+ suffer from this problem. The modified circuit shown in **Fig. 5** overcomes this problem by solving the limitation of the circuit in Fig. 4.

The circuit configuration of the proposed CCII is shown in Fig. 5. All transistors are assumed to be operating in the saturation region. M1-M8 are assumed to be matched. The negative feedback action on the gates of M3-M6 by means of the non-inverting amplifier stage composed of M9 and the current source I_D forces the sum of the currents flowing in M4 and M7 to equal I_B. Another negative feedback action applied from the drain to the gate of transistor M8 forces the two long tail structures M1-M4 and M5-M8 to follow the same differential voltage equivalent to the current driven from the node X. Therefore the voltage at the node Y is repro-

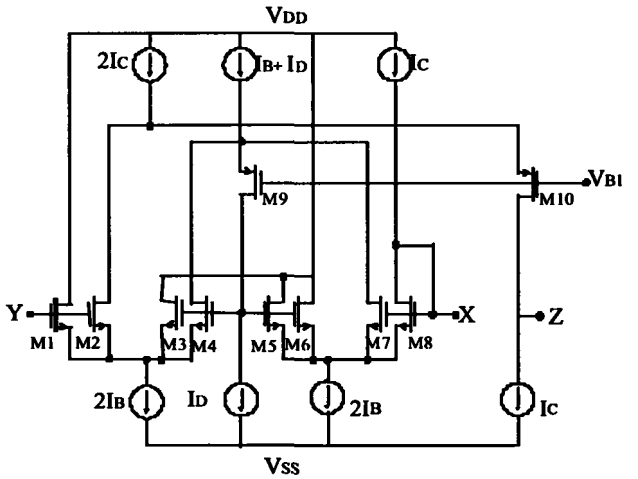

Fig. 5: Proposed CCII for high frequency applications

duced successfully at the node X. The high open loop gain obtained from the use of the two current tail structures with inherent local feedback actions minimizes significantly the input resistance at X as well as the offset voltage between v_Y and v_X [6]. The current flowing from X is reproduced at the node Z without the use of PMOS current mirrors, which improves the current following action between X and Z. This is done easily because the currents flowing in M1, M2, M7 and M8 are all equal. The transistor M10 is used to isolate the drain of M2 from fluctuations of the voltages at Z. It is clear that the current following action is insensitive to the errors in the aspect ratios of M10 which represents a major advantage over the use of conventional current mirrors. Also, it is noted that, in the complete circuit, PMOS current mirrors are completely avoided since the PMOS mirrors gate and drain capacitances usually have a major role in bandwidth degradation. Therefore, the bandwidth extent is expected to be highly improved. Thus, the voltage-following action between Y and X and the current-following action between X and Z are merged together in this special arrangement which makes the obtained bandwidth considerably wide. Consequently, the high frequency pole of the circuit is approximately given by

$$w_p \approx \frac{g_m}{C_{GS}}. \tag{17}$$

Although the analysis shows an improvement in the obtained bandwidth by a factor of two, the effective improvement is even larger. This is due to the fact that the accuracy of the current following action is not related to M10. Therefore, the aspect ratios of M10 can be optimized in order to obtain a considerable increase in the bandwidth.

The major drawback in this topology is the need of several precise current sources, which represents the price paid for this bandwidth improvement. A proposed biasing circuit is shown in **Fig. 6** that delivers the currents $2I_B$ and I_B. Similar circuits can be implemented to obtain the other required current sources in the circuit.

Accordingly, the voltage transfer function from the node Y to the node X is obtained as

$$A_v \approx \frac{\dfrac{2g_{m1}^2}{(g_{d4}+g_{d7})(g_{d8})}}{\left(1+2g_{m1}\dfrac{1}{(g_{d8})}\left(1+g_{m1}\dfrac{1}{(g_{d4}+g_{d7})}\right)\right)} \tag{18}$$

where the value of the output resistance of the current source is assumed infinite in the derivation but is included in the simulations later.

The resistance seen at the node X when the nodes Y and Z are grounded is given by

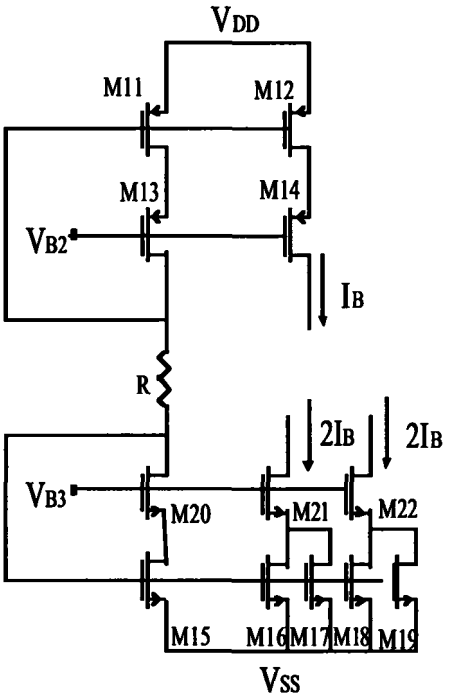

Fig. 6: Proposed precision current source circuit

$$r_X \approx \frac{(g_{d4}+g_{d7})}{(g_{d8})(g_{d4}+g_{d7})+2g_{m1}(g_{d4}+g_{d7}+g_{m1})}. \tag{19}$$

3. PSpice Simulations

The performances of the five current conveyor circuits shown in Figs. 1-5 are simulated using PSpice. Transistors aspect ratios are given in **Tables 1-5** and 0.5 µm MIETEC CMOS process are assumed. Supply voltages used are V_{DD}= -V_{SS}= 1.5 V and I_B is set to 50 µA. For the aspect ratios taken during simulations, the second realization will need to increase its phase margin using compensation techniques [13]. This is because the PMOS current mirrors, in addition to their function in the current following action, are used also to close the feedback loop of the voltage follower section. Therefore, unlike the other realizations, the effect of the large

Table 1: The W/L of the transistors of the circuit shown in Fig. 1

Transistor	Aspect Ratio
M1,M2	60/1
M3	8/1
M4,M5	50/2.5
M6	40/.5
M7,M8	50/2.5
M9,M10	50/2.5

Table 2: The W/L of the transistors of the circuit shown in Fig. 2

Transistor	Aspect Ratio
M1,M2	60/1
M3	8/1
M4,M5	50/2.5
M6,M7	50/2.5
M8,M9	50/2.5

Table 3: The W/L of the transistors of the circuit shown in Fig. 3

Transistor	Aspect Ratio
M1,M2	60/1
M3	8/1
M4	50/2.5
M5,M6	50/2.5
M7	4/1

Table 4: The W/L of the transistors of the circuit shown in Fig. 4

Transistor	Aspect Ratio
M1-M4	60/1
M5-M8b	50/2.5
M9-M11	8/1

Table 5: The W/L of the transistors of the circuit shown in Fig. 5

Transistor	Aspect Ratio
M1-M8	60/1
M9-M10	4/.5

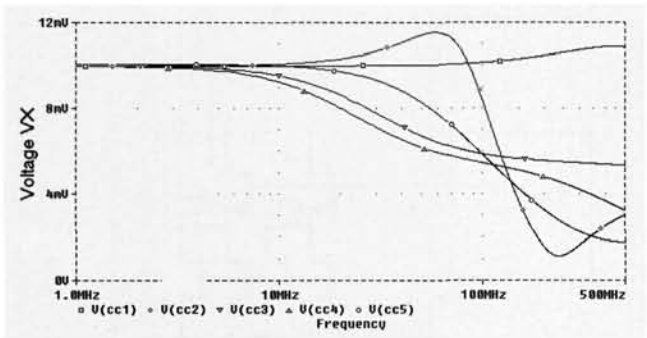

Fig. 7:The frequency characteristics of the voltage transfer gain between Y and X (V_X/V_Y)

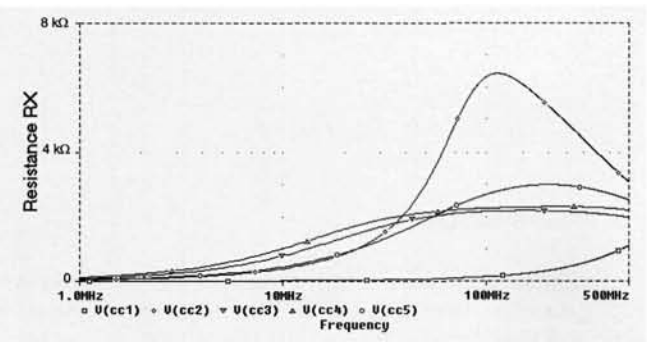

Fig. 8: The input resistance r_x versus frequency

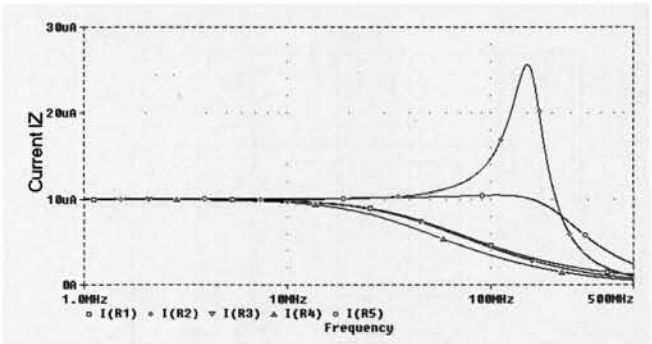

Fig. 9: The frequency characteristics of the transfer gains (I_Z/I_X)

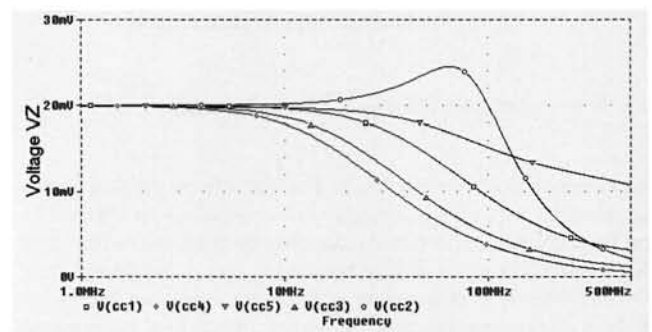

Fig. 10: The frequency characteristics of the voltage transfer gains of the CCII-based voltage amplifiers

Table 6

Current Conveyor	Simulated Open loop Gain (voltage section)	Simulated r_X	Simulated Bandwidth
Surakampontorn et al. CCII [3]	40 dB	2.5 Ω	48 MHz
Liu et al. CCII [4]	65 dB	2 Ω	42 MHz (a compensating capacitance will be needed to increase the phase margin)
Palsimino and Palumbo CCII [5]	44 dB	2.1 Ω	48 MHz.
Ismail and Soliman CCII [6]	47 dB	2.7 Ω	25 MHz
Modified Ismail and Soliman CCII for High Frequency Applications	51 dB	2.1 Ω	140 MHz.

Table 7

Current Conveyor	Simulated Offset Voltage**	Simulated Offset Current***
Surakampontorn et al. CCII [3]	-0. 05 mV	-0.03 μA
Liu et al. CCII [4]	-0. 04 mV	-0 03 μA
Palsimino and Palumbo CCII [5]	-0. 035 mV	-0.03 μA
Ismail and Soliman CCII [6]	-0. 05 mV	-0 03 μA
Modified Ismail and Soliman CCII for High Frequency Applications	+0. 05 mV	+0.02 μA

* Transistors mismatch effect is not taken in account in these simulation results.

** Simulations were taken for the case of 10 mVp-p input voltage.

*** Simulations results were taken for the case of 20 mA input current.

parasitic capacitances introduced by these transistors appear in the voltage follower section and hence need to be compensated. **Fig. 7** shows the voltage transfer characteristics from the node Y to the node X when the node X is terminated by R_x = 5 kΩ and V_Y is 0.5 Vp-p, the five CCII circuits enumerated in the same order of their presentation. **Fig. 8** shows the voltage at the node X when the node Y is grounded and the input current I_X is 10 μA, which represents the resistance r_x seen at the node X. It is shown that the resistance seen from all the configurations are low at low frequency and their behavior differ in high frequency. For all configurations, r_X does not exceed 6.5 kΩ. **Fig. 9** shows the current transfer characteristics from the node X to the node Z when the node Y is grounded and the input current I_X is 10 μA. It is clear that the proposed circuit offers a highly improved current-following action when compared to other configurations. Finally, the frequency characteristics of the voltage gain V_Z/V_Y when the node X is terminated by R_X = 5 kΩ and the node Z is terminated by R_Z =10 kΩ is shown in **Fig. 10**. It is clear that the second realization suffers from a considerable overshoot in its frequency response. The improvement in the proposed CCII current bandwidth due to the absence of the PMOS current mirror is also clearly observed. **Tables 6 and 7** present both theoretical and simulation results comparisons for the given circuits. Also for all the circuits, the THD was better than 55 dB for input signal amplitudes up to 0.6V.

4. Conclusion

Five CMOS Current conveyors based on a feedback-stabilized differential pair-based voltage follower are presented. Their performances have been compared based on PSpice simulation results. It has been thus shown that they are suitable to be used in current-mode analog circuit applications.

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