Journal of Circuits, Systems, and Computers
Vol. 20, No. 2 (2011) 243–262

DOI: 10.1142/S0218126611007232

World Scientific
www.worldscientific.com

ON THE TRANSFORMATION OF GROUNDED INDUCTORS TO FLOATING INDUCTORS USING OFA AND FCCII*

AHMED M. SOLIMAN

Electronics and Communications Engineering Department,
Faculty of Engineering, Cairo University, Egypt
asoliman@ieee.org

Received 21 September 2010
Accepted 11 October 2010

It is well known that a floating inductor circuit is realized from a grounded inductor circuit by replacing the operational amplifier by a floating operational transconductance amplifier. This idea is extended to transform current conveyor grounded inductors to floating inductors by replacing the current conveyor by the recently introduced floating current conveyor. Several examples are considered and simulation results are given to support the theory. Although the paper is partially a review in nature it includes several new realizations of floating inductors.

Keywords: Operational floating amplifier; floating current conveyors; grounded inductors; floating inductors.

1. Introduction

Several active RC realizations for realizing ideal grounded and floating inductors are available in the literature.[1–14] Classification of different active RC circuits simulating floating inductors was given in Ref. 1. The active building block used in Ref. 1 is the conventional operational amplifier (op amp) as well as special amplifiers with floating output ports.[3] The use of op amps in gyrator circuits is of great practical importance because of their wide range of applicability. In Ref. 3 a floating gyrator circuit using two fully floating operational transconductance amplifiers was generated from the Riordan-gyrator circuit which employs two op amps.[2] The operational floating amplifier (OFA)[4] which is also known as a nullor[5] can also be used in realizing floating gyrators.[4]

The valuable classification of floating inductors given in Ref. 1 also included the transformation of the grounded inductors given in Refs. 6 and 8 to floating inductors. Due to the importance of this topic it will be extended in this partially review paper

*This paper was recommended by Regional Editor Piero Malcovati.

to current conveyor (CCII) circuits.[9] In this paper three CCII circuits realizing grounded inductors are transformed to floating inductor circuits using the newly introduced floating current conveyor (FCCII).[15]

2. Floating Building Blocks

The two floating building blocks that are used in this paper are the OFA and the FCCII.

2.1. *The operational floating amplifier (OFA)*

The OFA is shown symbolically in Figs. 1(a) and 1(b) and is defined by Ref. 4:

$$V_{i1} = V_{i2}\,, \quad I_{i1} = I_{i2} = 0\,, \quad I_{O1} = -I_{O2}\,. \tag{1}$$

The above definition is identical to the definition of the nullor[5] with the input represented by a nullator and the output by a norator.

2.2. *The floating current conveyor (FCCII)*

There are two types of FCCII. The first FCCII is a four port building block as shown symbolically in Fig. 2(a) and is defined by the following matrix

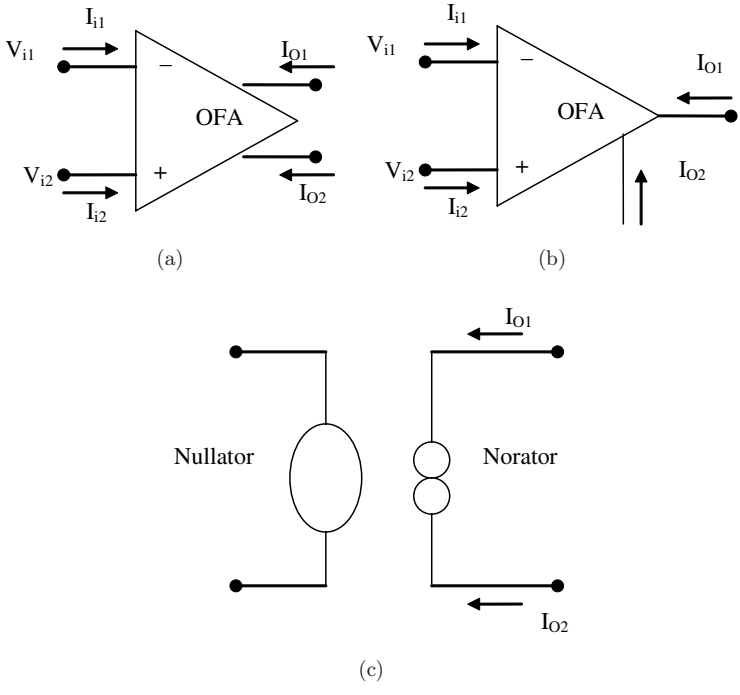
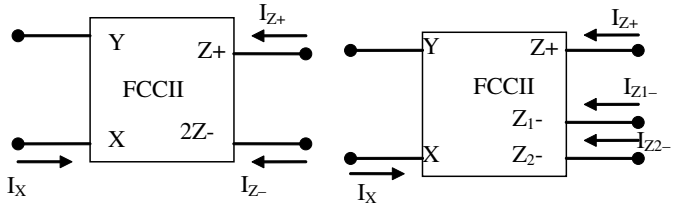


Fig. 1. Symbolic representations of the OFA.



(a) One Z-output. (b) Two Z-outputs.

Fig. 2. Symbolic representations of the FCCII.

equation[15]:

$$\begin{bmatrix} V_X \\ I_Y \\ I_{Z+} \\ I_{2Z-} \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 \\ -2 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_X \\ V_Y \\ V_{Z+} \\ V_{2Z-} \end{bmatrix}. \tag{2}$$

It is seen that this four port-active building block includes the CCII+ as special case with the $2Z$-port grounded. If the two Z output terminals are connected together it realizes a CCII− as special case.

The second FCCII is a five port active building block and is realized with two separate Z-outputs as shown symbolically in Fig. 2(b) and is defined by the following matrix equation:

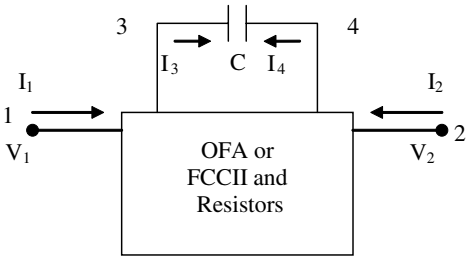
$$\begin{bmatrix} V_X \\ I_Y \\ I_{Z+} \\ I_{Z1-} \\ I_{Z2-} \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 \\ -1 & 0 & 0 & 0 & 0 \\ -1 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_X \\ V_Y \\ V_{Z+} \\ V_{Z1-} \\ V_{Z2-} \end{bmatrix}. \tag{3}$$

The FCCII defined by Eq. (2) can be realized from this FCCII by connecting the two Z-outputs together. On the other hand the FCCII defined by Eq. (3) cannot be realized from the FCCII defined by Eq. (2) and there are applications that require the two Z-terminals to be available as will be seen in the following sections.

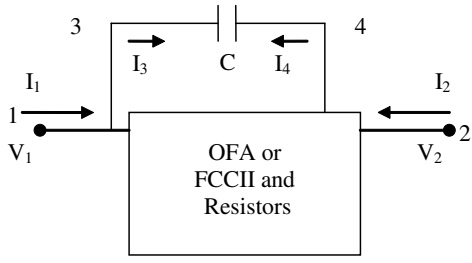
The floating inductors considered in this paper are classified into three generalized configurations as shown in Fig. 3. In the first configuration the capacitor is connected between nodes 3 and 4 and is not sharing any nodes with the input and output ports of the floating inductor. In the second configuration the capacitor node 3 coincides with node 1 of the input. In the third configuration the capacitor node 4 coincides with node 2 of the output.

3. The Floating Inductors Using OFA

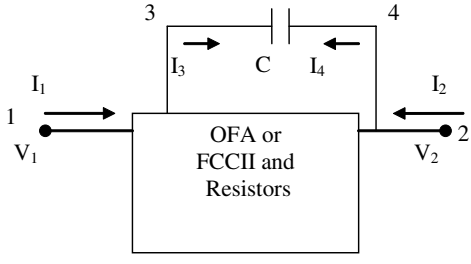
Three well known circuits realizing grounded inductors using op amps are reviewed in this section and are transformed to floating inductor circuits.



(a) Generalized configuration I.



(b) Generalized configuration II.



(c) Generalized configuration III.

Fig. 3. Three alternative configurations of the floating inductor circuit.

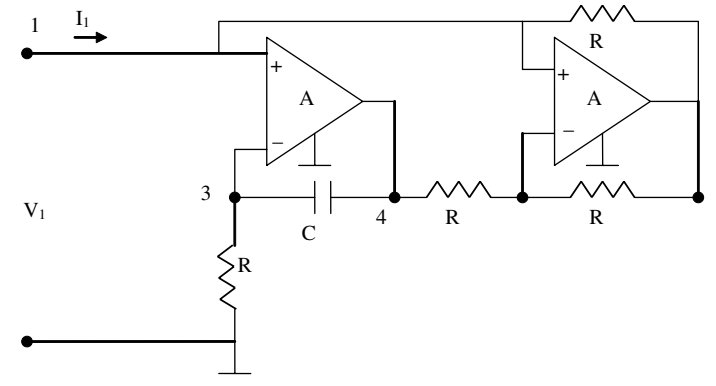
3.1. *Riordan two op amps gyrator circuit*

The Riordan grounded inductor circuit using two Op Amps is shown in Fig. 4(a).[2] A floating inductor circuit was also introduced in Ref. 2 using four op amps, two equal capacitors and seven equal resistors and is based on using two identical grounded inductor circuits connected in cascade resulting in a symmetrical two port circuit. For perfect isolation, the effective inductances of the two circuits must be equal, as any unbalance appears as a parasitic inductance to ground.[2] An alternative method of realizing a floating inductor from Fig. 4(a) and avoiding this matching requirement is to replace the two op amps in Fig. 4(a) by two OFA as shown in Fig. 4(b). The transmission matrix T is given by:

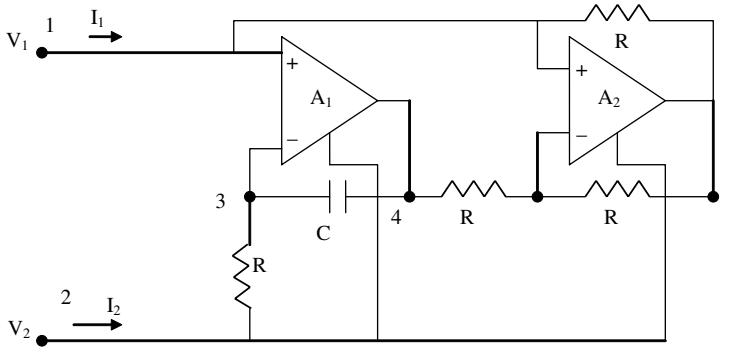
$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} 1 & sCR^2 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} V_2 \\ -I_2 \end{bmatrix}. \tag{4}$$

3.2. *Antoniou two op amps gyrator circuit*

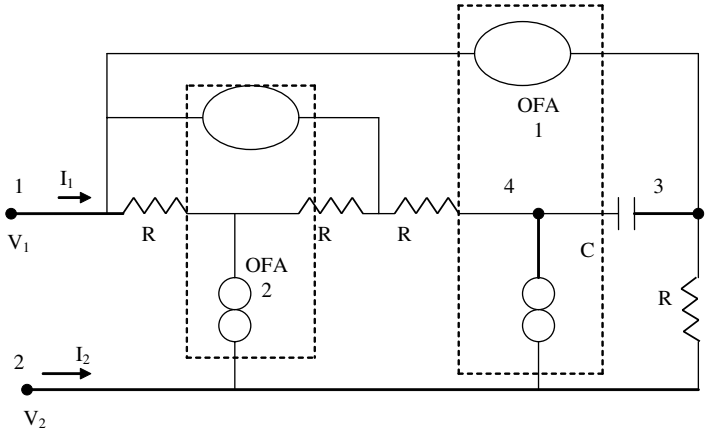
The second grounded inductor circuit considered is the Antoniou circuit using two op amps which is shown in Fig. 5(a).[6] If the resistor at node 4 is removed then the circuit realizes a generalized impedance converter (GIC). It is well known that a floating inductor can be realized from two identical GIC connected in cascade resulting in a symmetrical two port circuit using seven resistors, two capacitors and



(a)

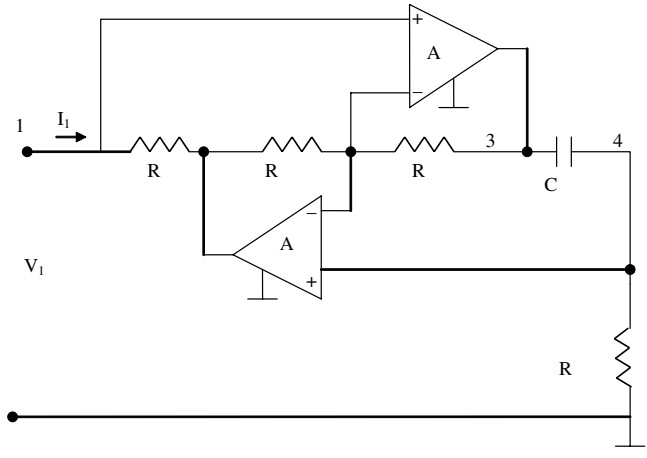


(b)

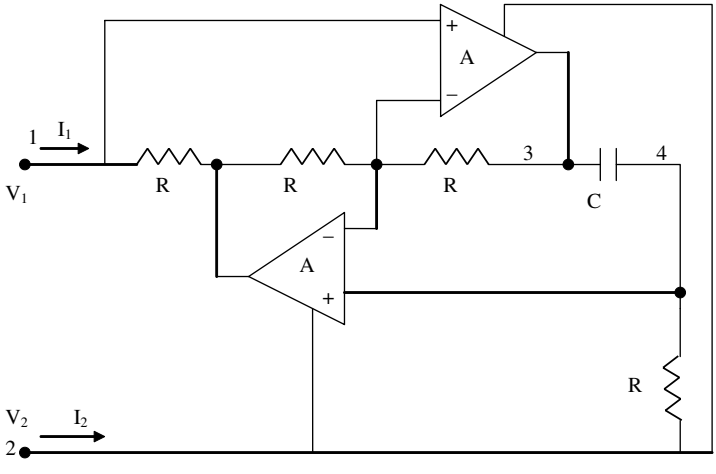


(c)

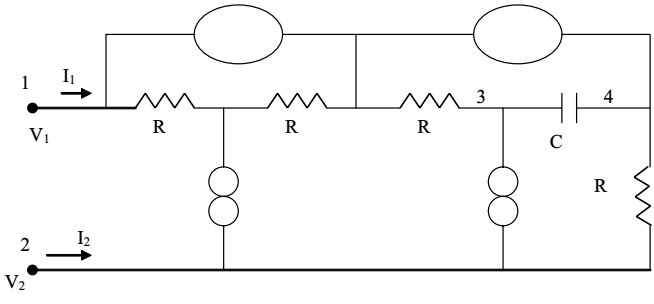
Fig. 4. (a) Riordan grounded inductor circuit using two op amps.[2] (b) Modified Riordan circuit realizing floating L using two OFA. (c) Two nullor realization of Riordan modified circuit.



(a)



(b)



(c)

Fig. 5. (a) Antoniou grounded inductor circuit using two op amps.[6] (b) Modified Antoniou circuit realizing floating L using two OFA. (c) Two nullor realization of Antoniou modified circuit.[7]

four Op Amps. For proper operation of the circuit the two GIC must be matched. Modification of the grounded inductor circuit of Fig. 5(a) to realize a floating inductor was given in Ref. 1 and Fig. 5(b) represents the floating circuit using two OFA. The realized floating inductor is given by CR^2. A two nullor equivalent circuit is shown in Fig. 5(c). This nullor circuit was also given in Fig. 1 of Ref. 7. This circuit belongs also to the configuration I shown in Fig. 3(a).

3.3. *Orchard– Willson single op amp gyrator circuit*

The third circuit to be considered is the single op amp grounded inductor circuit shown in Fig. 6(a) which uses six resistors and one capacitor.[8] This circuit requires matching conditions of the resistor values and a fairly detailed analysis based primarily on the behavior at low frequencies was given in Ref. 8. Maintaining a match of resistances to within a small percentage then for all but the highest quality of simulated inductances, this circuit should be satisfactory as stated in Ref. 8.

Modification of this circuit to realize a floating inductor was given in Ref. 1 and Fig. 6(b) represents the floating circuit using a single OFA. The realized floating inductor is given by $4CR^2$. A single nullor equivalent circuit is shown in Fig. 6(c).

Four alternative new realizations of the modified Orchard−Willson floating inductor circuit can be obtained from the equivalent two nullor circuit shown in Fig. 6(d). Replacing the two norator by two pathological current mirrors (CM) [16] results in Fig. 6(e).The first new realization using two CCII− is shown in Fig. 6(f).

The circuit components of this circuit are summarized in Table 1 together with the equivalent CCII+ circuit obtained from Fig. 6(e). There are two other new pathological circuits that can be obtained from Figs. 6(d) and 6(e) by replacing the two nullators by two voltage mirrors (VM) as shown in Table 1. The group of the circuits considered in this section belongs to configuration II shown in Fig. 3(b).

3.4. *Alternative CCII– floating inductor circuit*

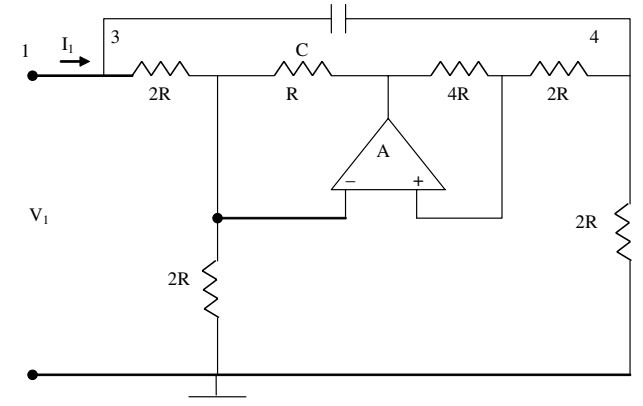
The circuit shown in Fig. 7(a) was introduced in Ref. 11 and was analyzed for non-idealities of the CCII− in Ref. 12. The transmission matrix for this circuit is the same as given by Eq. (4). This circuit belongs to the configuration I shown in Fig. 3(a).

4. The Floating Inductors using FCCII

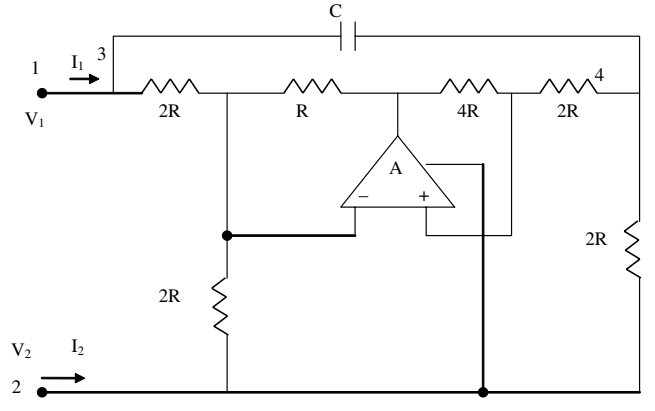
Three CCII circuits realizing grounded inductors are transformed to three new floating inductor circuits using the FCCII.

4.1. *New floating inductor using a single FCCII*

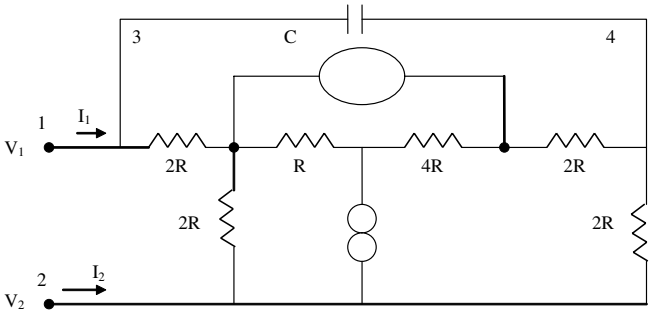
The first grounded inductor circuit using a single CCII+ was introduced in Ref. 10. Although it has the advantage of using a single CCII+ which is commercially



(a)

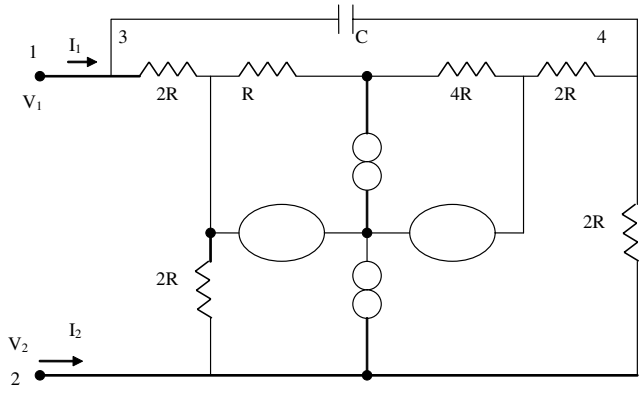


(b)

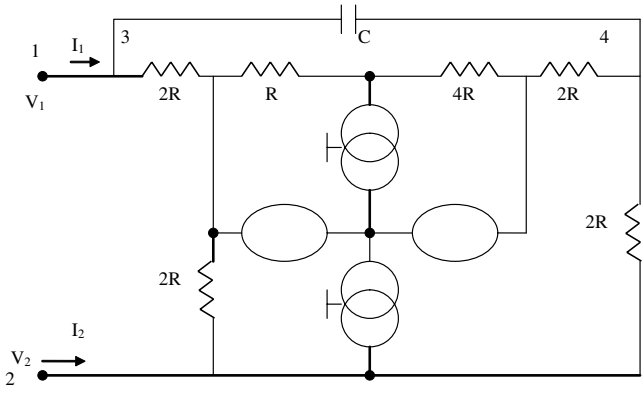


(c)

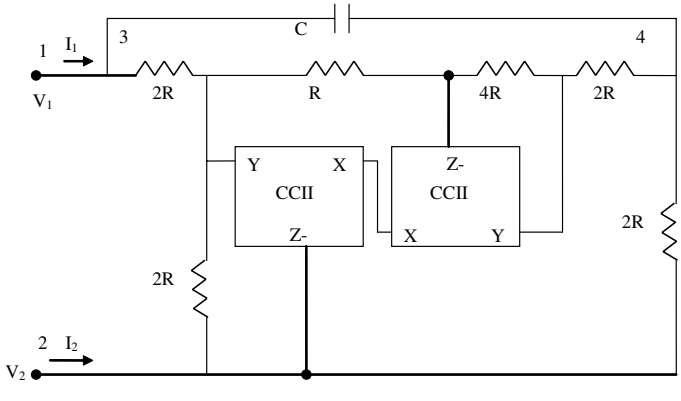
Fig. 6. (a) Orchard–Willson grounded inductor circuit.[8] (b) Modified Orchard–Willson floating inductor circuit.[1] (c) Single nullor realization of modified Orchard–Wilson circuit. (d) Two nullor realization of Fig. 6(b). (e) Equivalent realization to Fig. 6(d). (f) Realization of circuit of Fig. 6(d) using two CCII–.



(d)



(e)

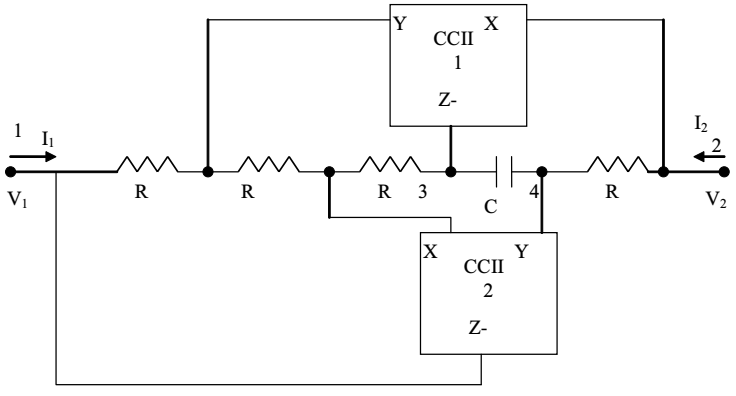


(f)

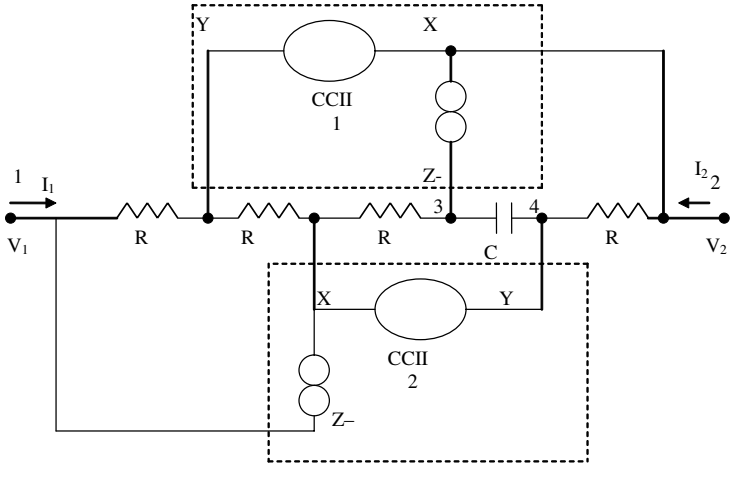
Fig. 6. (*Continued*)

Table 1. Circuit components of different floating inductor circuits.

Circuit figure	R	Nullator	Norator	CM	VM
4(c)	4	2	2	0	0
5(c)	4	2	2	0	0
6(c)	6	1	1	0	0
6(d)	6	2	2	0	0
6(e)	6	2	0	2	0
Eq. to 6(d)	6	0	2	0	2
Eq. to 6(e)	6	0	0	2	2
7(b)	4	2	2	0	0
8(b)	4	1	0	1	0
9(b)	2	2	1	1	0
10(b)	2	4	0	4	0



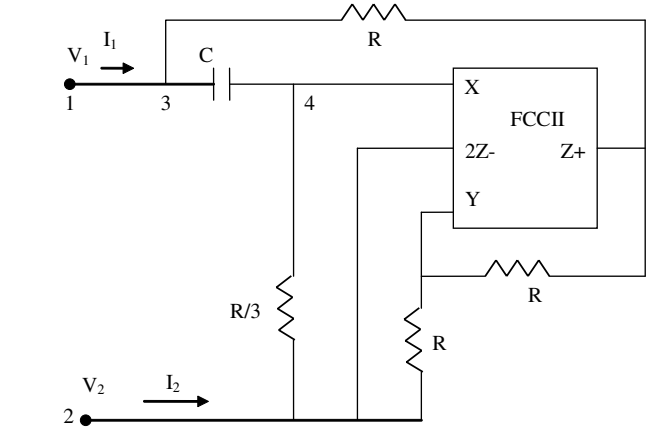
(a)



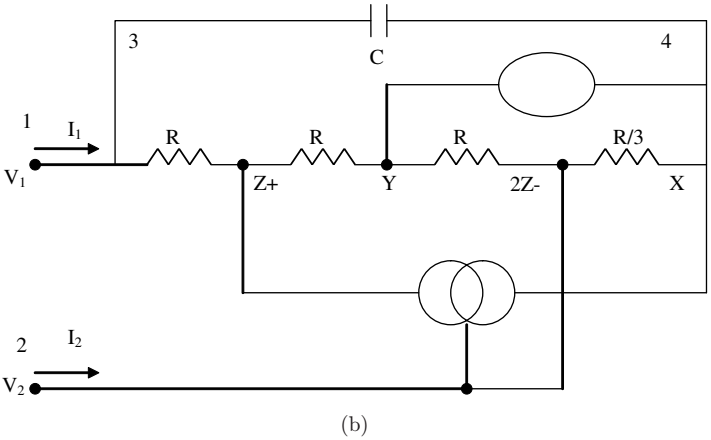
(b)

Fig. 7. (a) Inductor circuit using two CCII–.[11,12] (b) Pathological representation of the inductor of Fig. 7(a).

available, it has matching conditions on the resistor values which limits its practicality. This is similar to the single op amp circuit of Fig. 6(a); it uses however two resistors less than the circuit of Fig. 6(a). The realized floating inductor is given by $0.5CR^2$. Maintaining a match of resistances to within a small percentage, then for all but the highest quality of simulated inductances, this circuit should be satisfactory. A new realization of a floating ideal inductor circuit is obtained by replacing the CCII+ used in the grounded inductor circuit by a FCCII as shown in Fig. 8(a). Again this floating inductor circuit is sensitive to matching conditions of resistor value which limits its practicality. An exact expression for the input impedance of the grounded inductor circuit using CCII+ was given in Ref. 10 and similar mismatch



(a)



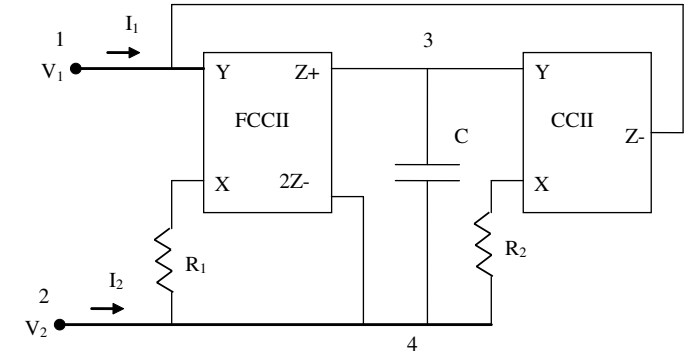
(b)

Fig. 8. (a) Modified floating inductor circuit.[10] (b) Pathological representation of the inductor of Fig. 8(a).

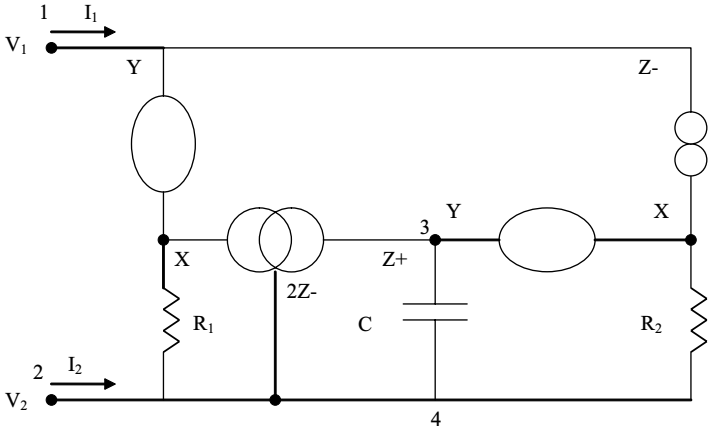
analysis of the floating inductor circuit can be obtained and is not included to limit the paper length. The pathological circuit model is given in Fig. 8(b). The circuit parameters are given in Table 1. This circuit belongs to the configuration II shown in Fig. 3(b).

4.2. *Modified Sedra–Smith two CCII gyrator circuit*

The first gyrator circuit introduced in the literature using CCII+ and CCII− was reported in Ref. 9. Since the CCII− is floating it will be kept in the circuit and the CCII+ is replaced by a FCCII, resulting in the new floating inductor shown in Fig. 9(a). This circuit uses the minimum number of passive elements namely two



(a)



(b)

Fig. 9. (a) Modified Sedra–Smith gyrator using FCCII and CCII−. (b) Pathological representation of the inductor of Fig. 9(a).

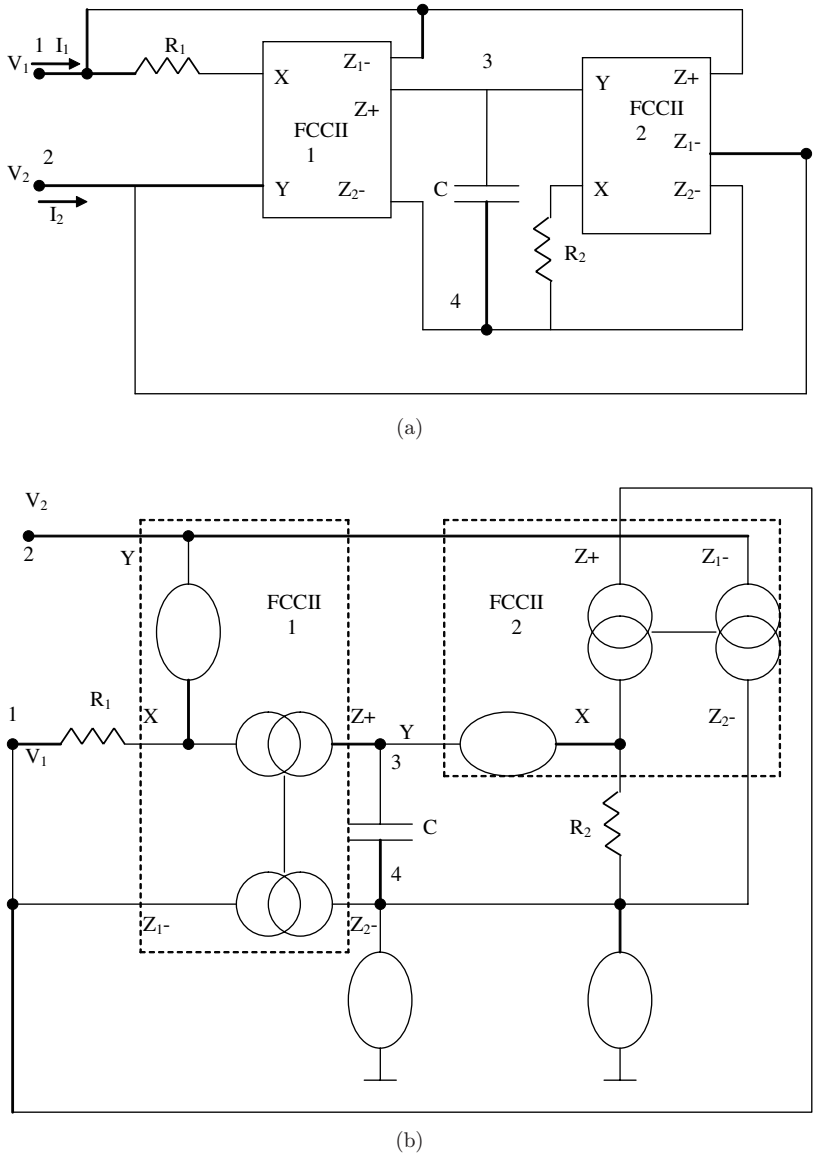


Fig. 10. (a) Modified Ananda Mohan inductor circuit using two FCCII.[13] (b) Pathological representation of the inductor of Fig. 10(a).

resistors and one capacitor to realize an ideal inductor. The realized floating inductor is given by CR^2. The pathological circuit model is given in Fig. 9(b). The circuit parameters are given in Table 1. This circuit belongs to the configuration III in which the capacitor C node 4 coincides with node 2 as defined in Fig. 3(c).

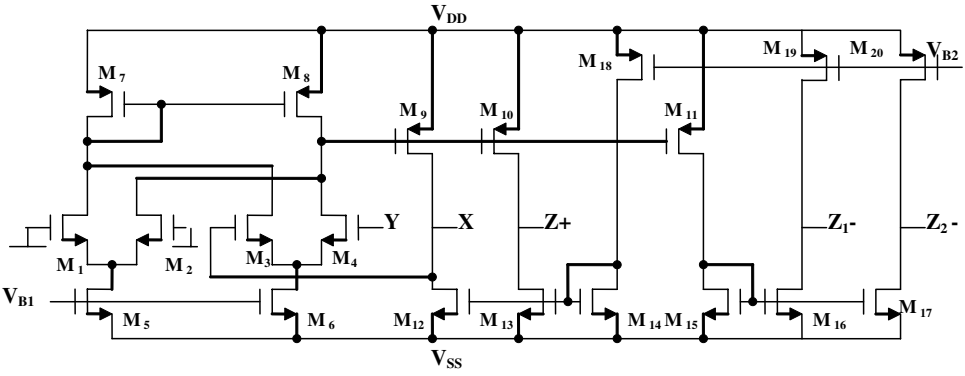


Fig. 11. CMOS circuit of the floating FCCII.

Table 2. Transistor aspect ratios of the FCCII of Fig. 10(b).

MOS Transistors	W(μm)/L(μm)
M_1, M_2, M_3, M_4	8/1
M_5, M_6	8/1
$M_{12}, M_{13}, M_{14}, M_{15}, M_{16}, M_{17}$	20/2.5
M_7, M_8	10/1
$M_9, M_{10}, M_{11}, M_{18}, M_{19}, M_{20}$	40/2

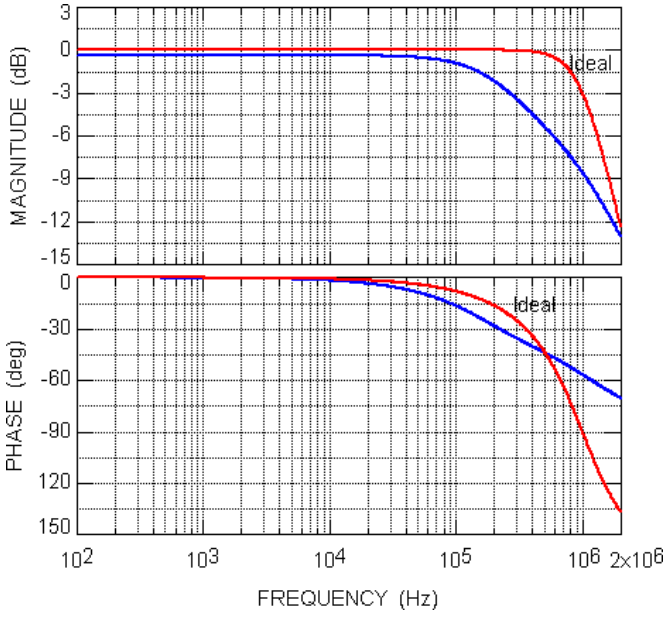
4.3. *Modified Ananda Mohan two CCII grounded inductor circuit*

The grounded inductor circuit introduced in Ref. 13 can also be transformed to a floating inductor circuit by replacing each of the balanced output CCII in Ref. 13 by a FCCII as shown in Fig. 10(a). This circuit uses the minimum number of passive elements namely two resistors and one capacitor to realize an ideal inductor. The realized floating inductor is given by CR^2. The pathological circuit model is given in Fig. 10(b) with two dummy nullator added to provide equal number of CM and nullator.[16] The circuit parameters are given in Table 1. This circuit belongs to the configuration I.

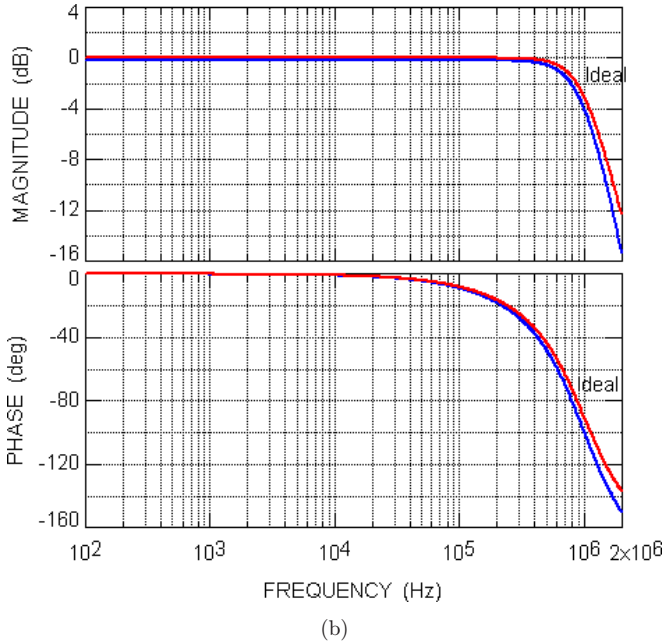
5. Simulation Results

The CMOS circuit realizing the FCCII is obtained directly from the well known differential voltage current conveyor (DVCC)[14] by adding the two MOS transistors M_{17} and M_{20} as shown in Fig. 11. The transistor aspect ratios are given in Table 2 based on the 0.5 μm CMOS model from MOSIS. The supply voltages used are ± 1.5 V, $V_{B1} = -0.52$ V and $V_{B2} = 0.33$ V.

As a first application of the floating reported circuits, a floating inductor of magnitude 0.253 m-H is realized using circuits of Figs. 6(f), 7(a), 8(a), 9(a) and 10(a).



(a)



(b)

Fig. 12. (a) Simulation results of a low-pass filter using L of Fig. 6(f). (b) Simulation results of a low-pass filter using L of Fig. 7(a).

The floating inductor is used to realize a maximally flat second-order low-pass filter ($Q = 0.707$) with cutoff frequency of 1 MHz using a series resistor of $R_S = 2.25\,\text{k}\Omega$ and C_S of 100 pF.

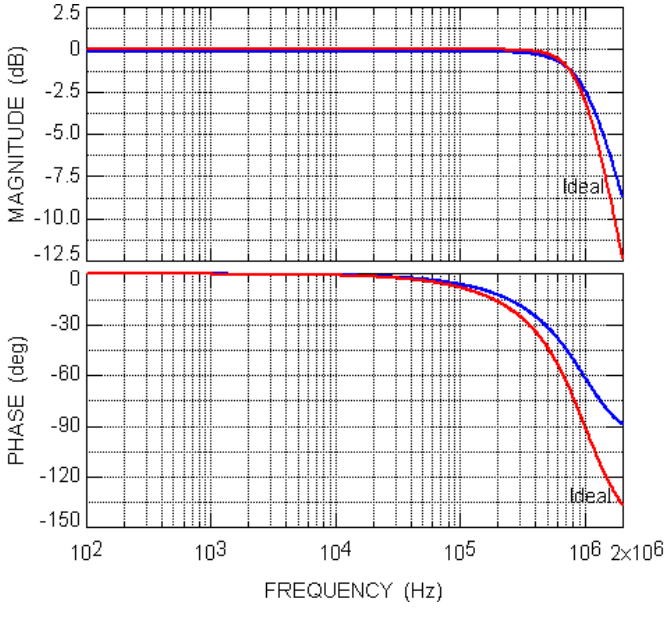
Figure 12(a) represents the simulated magnitude and phase responses together with the ideal responses using the inductor circuit of Fig. 6(f), with two CCII−, $C = 100\,\text{pF}$, $2R = 1.59\,\text{k}\Omega$. The total power dissipation is equal to 2.2669 mW.

Figure 12(b) represents the simulated magnitude and phase responses together with the ideal responses using the inductor circuit of Fig. 7(a), with two CCII−, $C = 100\,\text{pF}, R = 1.59\,\text{k}\Omega$. The total power dissipation is equal to 2.3259 mW.

Figure 13(a) represents the simulated magnitude and phase responses together with the ideal responses using the inductor circuit of Fig. 8(a) using a single FCCII, $C = 200\,\text{pF}, R = 1.59\,\text{k}\Omega$. The total power dissipation is the lowest among all considered circuits and is equal to 1.0429 mW.

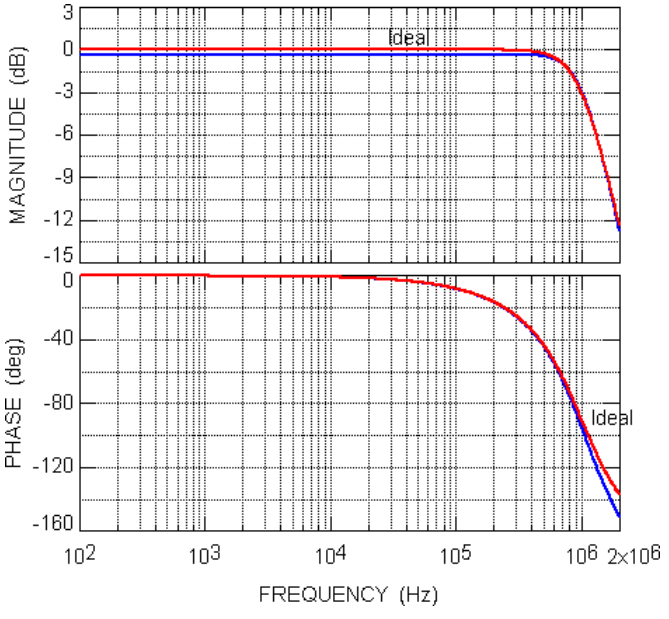
Figure 13(b) represents the simulated magnitude and phase responses together with the ideal responses using the inductor circuit of Fig. 9(a), with $C = 100\,\text{pF}$, $R = 1.59\,\text{k}\Omega$. The total power dissipation is equal to 2.3305 mW.

Figure 13(c) represents the simulated magnitude and phase responses together with the ideal responses using the inductor circuit of Fig. 10(a) with $C = 100\,\text{pF}, R = 1.59\,\text{k}\Omega$. The total power dissipation is equal to 2.1937 mW.

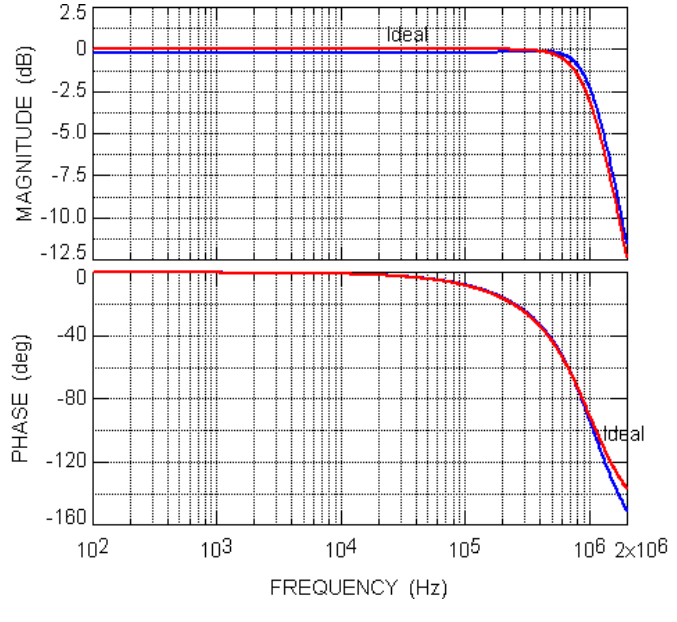


(a)

Fig. 13. (a) Simulated magnitude and phase response of low-pass filter using floating inductor of Fig. 8(a). (b) Simulation results of a low-pass filter using L of Fig. 9(a). (c) Simulation results of a low-pass filter using L of Fig. 10(a).

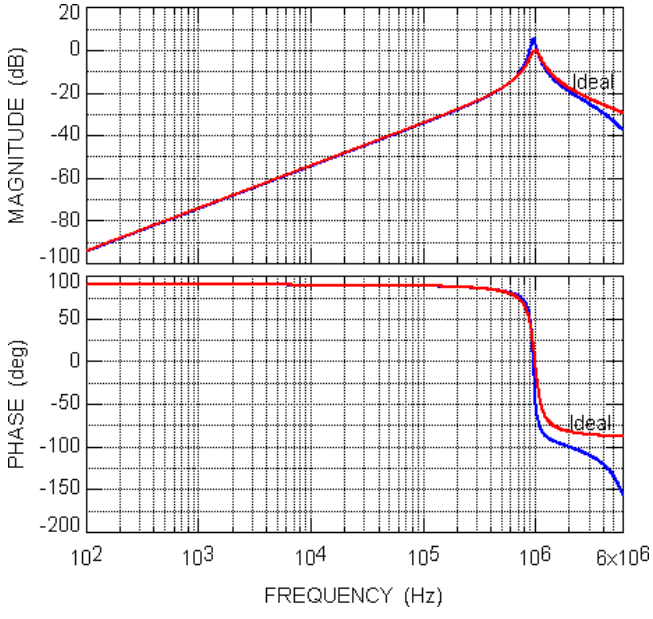


(b)

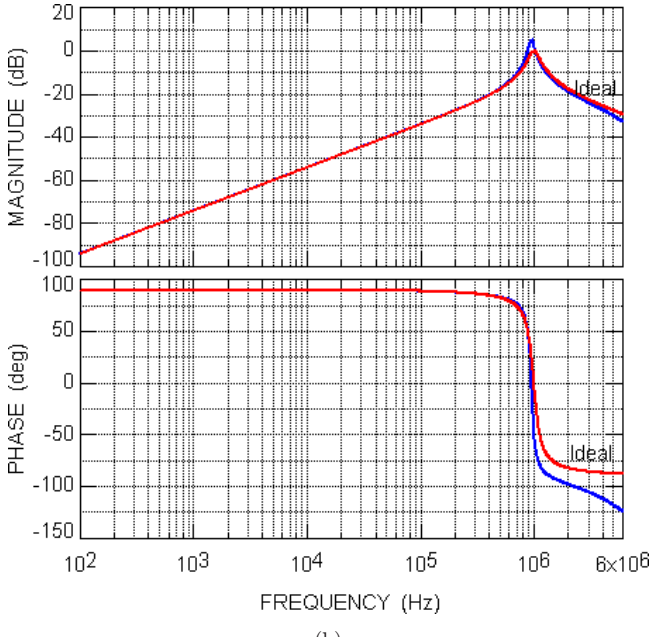


(c)

Fig. 13. (*Continued*)



(a)



(b)

Fig. 14. (a) Simulation results of a band-pass filter using L of Fig. 9(a). (b) Simulation results of a band-pass filter using L of Fig. 10(a).

As a second application a floating inductor of magnitude 0.253 mH is realized, the capacitor $C = 100\,\text{pF}$, equal resistors of $1.59\,\text{k}\Omega$. The floating inductor is used to realize a second-order band-pass filter having a center frequency of 1MHz and $Q = 5$, using a series resistor of $R_S = 318\,\Omega$ and C_S of 100 pF.

Figure 14(a) represents the simulated magnitude and phase responses together with the ideal responses using the inductor of Fig. 10(a). The total power dissipation is equal to 2.2508 mW.

Figure 14(b) represents the simulated magnitude and phase responses together with the ideal responses using the inductor of Fig. 10(a). The total power dissipation is equal to 2.2364 mW.

6. Conclusions

The realization of ideal floating inductors using OFA is reviewed and four new circuits based on Orchard Willson single op amp gyrator are introduced. Three new floating inductor circuits using FCCII are given.

For fair comparison the reported inductor circuits are used in the same low-pass filter and simulated using the same CMOS circuit given in Fig. 11. Pathological circuit models of the proposed new floating inductors are included and the circuit components are given in Table 1. It should be noted that the only two circuits considered in this paper that require resistor matching conditions are the circuits derived from Orchard−Willson circuit [8] and the single FCCII floating inductor circuit. The circuits of Figs. 9(a) and 10(a) employs the minimum number of passive elements, namely two resistors and one capacitor. The simulation results included are very close to the ideal ones except for the circuit of Fig. 6(f); this is due to the parasitic resistances $R_{X1} + R_{X2}$ of the two CCII− acting between the two X terminals.

References

1. M. Silva and W. Saraga, On the classification of active *RC* circuits simulation floating inductors, *Proc. 3rd Int. Symp. Network Theory* (1975), pp. 489−496.
2. R. H. S. Riordan, Simulated inductors using differential amplifiers, *Electron. Lett.* **3** (1967) 50−51.
3. H. R. Trimmel and W. E. Heinlein, Fully floating chain type gyrator circuit using operational trans-conductance amplifiers, *IEEE Trans. Circuits Theor.* **18** (1971) 719−721.
4. J. H. Huijsing, Design and applications of the operational floating amplifier (OFA): The most universal operational amplifier, *Anal. Integr. Circuits Signal Process.* **4** (1993) 115−129.
5. H. J. Carlin, Singular network elements, *IEEE Trans. Circuits Theor.* **11** (1964) 67−72.
6. A. Antoniou, Realization of gyrators using operational amplifiers, and their use in RC-active-network synthesis, *Proc. Inst. Elec. Eng.* **116** (1969) 1838−1850.
7. K. M. Adams and E. Deprettere, On the realization of gyrators by nullors and resistors, *Int. J. Circuits Theor. Appl.* **2** (1974) 287−290.
8. H. J. Orchard and A. Willson, New active gyrator circuit, *Electron. Lett.* **10** (1974) 261−262.

9. A. S. Sedra and K. C. Smith, A second generation current conveyor and its applications, *IEEE Trans. Circuits Theor.* **132** (1970) 132−134.
10. A. M. Soliman, New active gyrator circuit using a single current conveyor, *Proc. IEEE* **66** (1978) 1580−1581.
11. R. Senani, Floating ideal FDNR using only two current conveyors, *Electron. Lett.* **20** (1984) 205−206.
12. J. A. Svoboda, Comparison of RC op amps and RC current conveyor filters, *Int. J. Electron.* **76** (1994) 615−626.
13. P. V. A. Mohan, Grounded capacitor based grounded floating inductance simulation using current conveyors, *Electron. Lett.* **34** (1998) 1037−1038.
14. H. O. Elwan and A. M. Soliman, A novel CMOS differential voltage current conveyor and its applications, *IEE Proc. Circuits, Dev. Syst.* **144** (1997) 195−200.
15. A. M. Soliman and R. A. Saad, On the introduction of new floating current conveyors, *J. Circuits Syst. Comput.* **18** (2009) 1005−1016.
16. I. A. Awad and A. M. Soliman, Inverting second-generation current conveyors: The missing building blocks, CMO realizations and applications, *Int. J. Electron.* **86** (1999) 413−432.