INTERNATIONAL JOURNAL OF CIRCUIT THEORY AND APPLICATIONS
Int. J. Circ. Theor. Appl. 2010; **38**:935–967
Published online 8 June 2009 in Wiley Online Library (wileyonlinelibrary.com). DOI: 10.1002/cta.604

On the systematic synthesis of CCII-based floating simulators

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SUMMARY

This paper is adopting a new approach in the systematic synthesis of CCII-based floating simulators. The synthesis procedure is based on the generalized systematic synthesis framework for active circuits using admittance matrix expansion. The resulting derived floating simulators include circuits that have been reported earlier in the literature in addition to novel floating simulators using various types of CCII. The synthesized floating simulators can be used to realize floating coils, FDNRs, and resistance and capacitance multipliers; according to the types of passive elements employed in the design. The potentials and drawbacks of every one of the synthesized circuits vary according to the design tradeoffs including complexity, number of active devices, number and values of grounded and floating passive elements, matching requirements, and tunability. SPICE simulations are presented to verify the performance of the new circuits obtained by systematic synthesis and hence demonstrate the potentials of the generalized synthesis framework in producing novel circuits with high performance. Copyright © 2009 John Wiley & Sons, Ltd.

Received 10 January 2008; Revised 17 March 2009; Accepted 29 March 2009

KEY WORDS: synthesis; floating simulators; coils; FDNR; current conveyor; nullor; mirror element

1. INTRODUCTION

The floating simulators have always been basic elements in analog signal-processing circuits that are used to overcome the limitations of actual on-chip passive elements (e.g. floating coils and high-valued floating capacitances or resistances). The second generation current conveyor (CCII) [1] is one of the most popular active building-blocks used to realize floating simulator circuits throughout the literature. Several authors have investigated and proposed various simulator circuits for floating coils, FDNRs, and capacitance multipliers using CCIIs. However, in the process of designing active circuits, it is desirable to follow systematic methodologies to obtain novel circuits [2, 3]. This is beneficial in developing analog tools for circuit design automation. In [3], some current-mode floating inductance simulators using current conveyors and transconductance amplifiers have been derived by a systematic approach.

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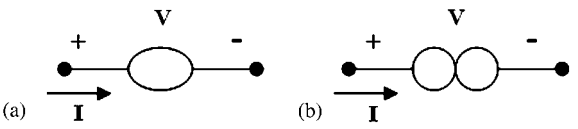

Figure 1. Nullor elements: (a) nullator and (b) norator.

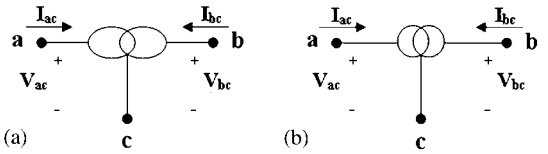

Figure 2. Mirror elements: (a) voltage mirror and (b) current mirror.

Recently, a systematic synthesis framework for linear active-RC circuits has been proposed in [4, 5]. The systematic synthesis approach adopted in this framework employs admittance matrix expansion, such that a $p \times p$ port admittance matrix describing a certain circuit function is expanded to an $n \times n$ nodal admittance matrix (NAM) describing the circuit to be synthesized, where $n > p$. The matrix expansion process begins by applying pivotal expansion [4, 6], which is the reverse operation of the Gaussian elimination, to all matrix elements including products and quotients of admittance terms; until every element in the admittance matrix becomes a single admittance term representing a single circuit element. Then, blank rows and columns, corresponding to internal nodes, are introduced in the resulting matrix, and nullor elements (shown in Figure 1) are used to move matrix elements to their final locations, correctly describing either floating or grounded passive elements. Thus, the final NAM is obtained including finite elements representing passive circuit components and unbounded elements, so-called infinity-variables [4, 5], representing nullor elements. This systematic synthesis framework has been extended in [7, 8] to use NAM representations for mirror elements [9], in addition to nullor elements, in the matrix expansion process and the ideal representation of active devices. Figure 2 shows the schematic representations of the mirror elements. This generalized approach facilitates the extraction of more alternative ideal representations based on all types of pathological elements (nullor elements and mirror elements) and, hence, more circuit realizations for a certain function can be achieved. Moreover, a wide range of active elements can be used in the circuit synthesis.

The admittance matrix transformations in the synthesis framework can be summarized as follows. (a) nullators used to move admittance terms between columns; (b) norators are used to move admittance terms between rows; (c) voltage mirrors used to move admittance terms between columns and reverse their sign; and (d) current mirrors are used to move admittance terms between rows and change their sign. Thus, such elements can be introduced to change the positions of the matrix elements and have an admittance equivalent admittance matrix satisfying the required relationships between the input and output signals. The new admittance matrix including the admittance terms, after altering their positions, together with the introduced nullor–mirror elements, represents the synthesized circuit, such that admittance terms represent passive elements whereas nullor–mirror elements give an ideal representation for active elements.

In this paper, a new systematic approach is presented for the derivation of CCII-based floating simulators, using the generalized synthesis framework by admittance matrix expansion [7, 8]. The synthesized floating simulators can be used to obtain floating coils, FDNRs, and capacitance or

DOI: 10.1002/cta

resistance multipliers according to the types of passive elements employed in the design. However, the suitability of every synthesized circuit for every application is specified according to the types of parasitic elements, associated with the CCIIs, at the circuit terminals. Various CCII types such as the CCII+ [1], differential voltage current conveyor (DVCC) [10], balanced-output CCII [11], and dual-X CCII [12, 13] are used to realize the floating simulators. The synthesized circuits comprise floating simulators that have been reported earlier in the literature, as well as novel circuit realizations. The advantages and drawbacks of the synthesized circuits vary according to the design tradeoffs including the number of active devices, number and values of floating and grounded passive elements, matching requirements, and tunability.

Section 2 provides a brief explanation for the synthesis approach adopted throughout the paper. The floating simulators are synthesized in Section 3, where the floating simulator circuits are classified according to the combination of floating and grounded passive elements, and the suitability of every synthesized circuit to simulate a wide-band floating coil or FDNR is specified according to the types of parasitic elements at its terminals. In Section 4, SPICE simulations are taken for some novel circuits from those synthesized in Section 3, so that to demonstrate their performance. Finally, conclusions are drawn in Section 5.

2. SYNTHESIS APPROACH

The foundations for the generalized synthesis framework adopted in this paper have been laid down in [4, 5, 7]. Consider a floating simulator, represented by the floating two-port network in Figure 3, with input admittance Y_{in} defined by:

$$Y_{\text{in}} = \frac{Y_1 Y_2}{Y_3} \tag{1}$$

This input admittance expression has three admittance terms, Y_1, Y_2, and Y_3. The type of the floating simulator is specified according to the type of the passive element corresponding to every admittance term. For example, in order to realize a simulated floating inductance $L = C/G_1G_2$, the admittance terms in Equation (2) should be $Y_1 = G_1$, $Y_2 = G_2$, and $Y_3 = sC$; whereas, to simulate an FDNR with $D = C_1C_2/G$, the admittance terms should be $Y_1 = sC_1$, $Y_2 = sC_2$, and $Y_3 = G$.

This ideal abstraction may loosely indicate that any CCII-based floating simulator circuit can always simulate a coil or an FDNR according to the types of the passive elements connected at the simulator terminals. However, due to the frequency-dependent operation of actual circuits, the suitability of a certain CCII-based simulator circuit to simulate a coil or an FDNR is determined by

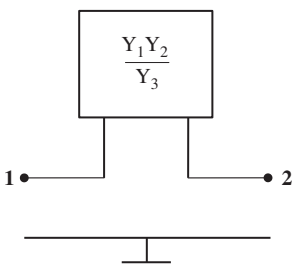

Figure 3. Symbolic representation for two-port floating simulator.

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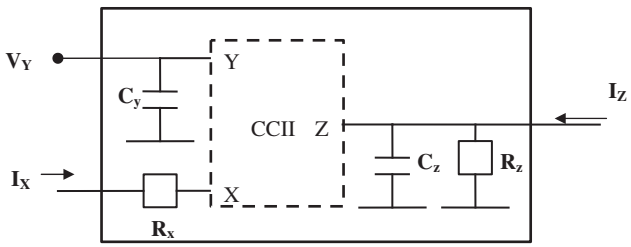

Figure 4. CCII symbolic representation including a modeling for the parasitic impedance components at the CCII terminals.

two important factors. First, the required bandwidth. Second, the types of actual passive elements that will be connected to the terminals of the active devices. The actual CCII parasitic components can be included in the CCII symbolic representation as shown in Figure 4, where the parasitic resistances of the CCII appear in series at the X-terminal and in parallel at the Z-terminal, and the parasitic capacitances appear in parallel at the Y- and Z-terminal [8]. The bandwidth of operation is sensitive to the combination between these parasitic elements and the actual passive elements connected at the terminals of the CCIIs [8]. At high frequencies, the parasitic capacitances become more effective and hence can substantially degrade the operation. Thus, in order to achieve wider bandwidth and better performance at high frequencies for CCII-based circuits, it is required to avoid connecting actual capacitances at CCIIs X-terminals, which have parasitic series resistances, because the resulting low-pass RC sections will introduce inevitable degradation of the performance at high frequencies [8]. Actual capacitances should be connected at Y–Z-terminals so that to absorb the parasitic capacitances at such terminals. Also, actual resistors should be connected at the CCIIs X-terminals so that to absorb the series parasitic resistances. On the other hand, at low frequencies, parasitic capacitances have negligible effects and the impedances of the actual capacitors are relatively low. Thus, at low frequencies, actual capacitors can be connected at the X-terminals without degrading the operation due to their relatively low impedances, while giving a room for actual resistors to be connected at Z-terminals so that to reduce the effect of the very high parallel parasitic resistors there.

The synthesis operations start from the port admittance matrix for the floating simulator in Equation (1), which is given by

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} \dfrac{Y_1 Y_2}{Y_3} & \dfrac{-Y_1 Y_2}{Y_3} \\ \dfrac{-Y_1 Y_2}{Y_3} & \dfrac{Y_1 Y_2}{Y_3} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \tag{2}$$

Then, a single pivotal expansion is applied on the $\pm Y_1 Y_2 / Y_3$ terms in Equation (2), so that every matrix element becomes a single admittance term. The resulting expanded admittance matrices will be

$$\begin{bmatrix} 0 & 0 & Y_1 \\ 0 & 0 & -Y_1 \\ -Y_2 & Y_2 & Y_3 \end{bmatrix} \tag{3}$$

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or

$$\begin{bmatrix} 0 & 0 & -Y_1 \\ 0 & 0 & Y_1 \\ Y_2 & -Y_2 & Y_3 \end{bmatrix} \tag{4}$$

The NAMs in Equations (3) and (4) can be further expanded using conventional matrix operations and NAM representations for pathological elements [4–8], ideally representing active devices, until every group of admittance terms represent either grounded or floating passive elements. Each group of the $\pm Y_1$ and $\pm Y_2$ terms include two admittance terms and hence each one of the terms that belong to the same group can undergo different matrix expansion transformations to independently represent a single passive element. However, there is an important practical constraint that should be taken under consideration when applying this scenario. The values of the resulting passive elements will either be equal or have a common factor and, hence, the actual implementation of these passive elements will entail matching requirements. Thus, these passive elements should be connected in a similar way (either grounded or floating) so that to enable the practical monolithic implementation to satisfy the matching conditions as much as possible.

The Y_3 term in (3) and (4) is a single admittance term located on the diagonal and, hence, it represents a grounded admittance. Additional circuit realizations can be obtained if matrix operations are performed on this Y_3 term to represent a floating admittance. While grounded admittances lend themselves to monolithic integration more than floating ones do, replacing a grounded admittance by a floating one in a design is justified by reducing either the total number of passive elements or the number of active devices. The number of circuit realizations that can be synthesized for circuits with grounded Y_3 present an adequate material to achieve the objectives of this paper. Hence, the synthesized floating simulator circuits in this paper are classified according to the combination of floating and grounded passive elements resulting from the matrix expansion transformations applied on the $\pm Y_1$ and $\pm Y_2$ terms, while Y_3 is always a grounded admittance. This classification will yield four different classes of floating simulator circuits. Systematic synthesis of CCII-based circuits that belong to every class will be presented in the next section.

3. SYNTHESIS OF FLOATING SIMULATORS

3.1. Floating Y_1 and Y_2

Expansion steps are applied to the matrix in Equation (3) to move the $\pm Y_1$ and $\pm Y_2$ terms so that they represent floating admittance terms. Firstly, blank rows and columns 4 and 5 are added

$$\begin{bmatrix} 0 & 0 & Y_1 & 0 & 0 \\ 0 & 0 & -Y_1 & 0 & 0 \\ -Y_2 & Y_2 & Y_3 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix} \tag{5}$$

DOI: 10.1002/cta

A nullator is connected between node 3 and node 5, so that to move the $\pm Y_1$ terms from column 3 to column 5.

$$\begin{bmatrix} 0 & 0 & Y_1 & 0 & 0 \\ 0 & 0 & -Y_1 & 0 & 0 \\ -Y_2 & Y_2 & Y_3 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix} \equiv \begin{bmatrix} 0 & 0 & 0 & 0 & Y_1 \\ 0 & 0 & 0 & 0 & -Y_1 \\ -Y_2 & Y_2 & Y_3 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix} \tag{6}$$

Two current mirrors are used to link node 1 to node 4 and node 2 to node 5, so that to move the Y_1 and $-Y_1$ terms to the locations $(4, 5)$ and $(5, 5)$, respectively.

$$\begin{bmatrix} 0 & 0 & 0 & 0 & Y_1 \\ 0 & 0 & 0 & 0 & -Y_1 \\ -Y_2 & Y_2 & Y_3 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix} \equiv \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ -Y_2 & Y_2 & Y_3 & 0 & 0 \\ 0 & 0 & 0 & 0 & -Y_1 \\ 0 & 0 & 0 & 0 & Y_1 \end{bmatrix} \tag{7}$$

Then, a nullator is used to retrieve the missing $\pm Y_1$ terms from the column corresponding to the reference node.

$$\begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ -Y_2 & Y_2 & Y_3 & 0 & 0 \\ 0 & 0 & 0 & 0 & -Y_1 \\ 0 & 0 & 0 & 0 & Y_1 \end{bmatrix} \equiv \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ -Y_2 & Y_2 & Y_3 & 0 & 0 \\ 0 & 0 & 0 & Y_1 & -Y_1 \\ 0 & 0 & 0 & -Y_1 & Y_1 \end{bmatrix} \tag{8}$$

Now, the $\pm Y_1$ terms in Equation (8) represent a floating admittance Y_1 connected between nodes 4 and 5. The NAM in (8) can be further expanded in a similar scheme, so that the $\pm Y_2$ terms

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represent a floating admittance Y_2 connected between nodes 6 and 7

$$\begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ -Y_2 & Y_2 & Y_3 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & Y_1 & -Y_1 & 0 & 0 \\ 0 & 0 & 0 & -Y_1 & Y_1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}$$

$$\equiv \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & Y_3 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & Y_1 & -Y_1 & 0 & 0 \\ 0 & 0 & 0 & -Y_1 & Y_1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & Y_2 & -Y_2 \\ 0 & 0 & 0 & 0 & 0 & -Y_2 & Y_2 \end{bmatrix} \tag{9}$$

The resulting NAM in Equation (9) represents the nullor–mirror circuit shown in Figure 5(a). Since the nullor–mirror elements are connected in a closed loop, they can be mapped as current conveyors in two different ways, resulting in the two CCII-based realizations shown in Figure 5(b) and (c). The circuit in Figure 5(b) is more suitable for realizing a wide-band simulated floating coil, because Y_3 will be a capacitance C connected at a Y–Z-terminal absorbing the parasitic capacitances at this terminal, and hence, avoid extra poles introduced by the parasitic capacitances at this Y–Z terminal. On the other hand, if a wide-band floating FDNR is to be simulated, then the circuit in Figure 5(c) would be a better contender for operation at high frequencies, because

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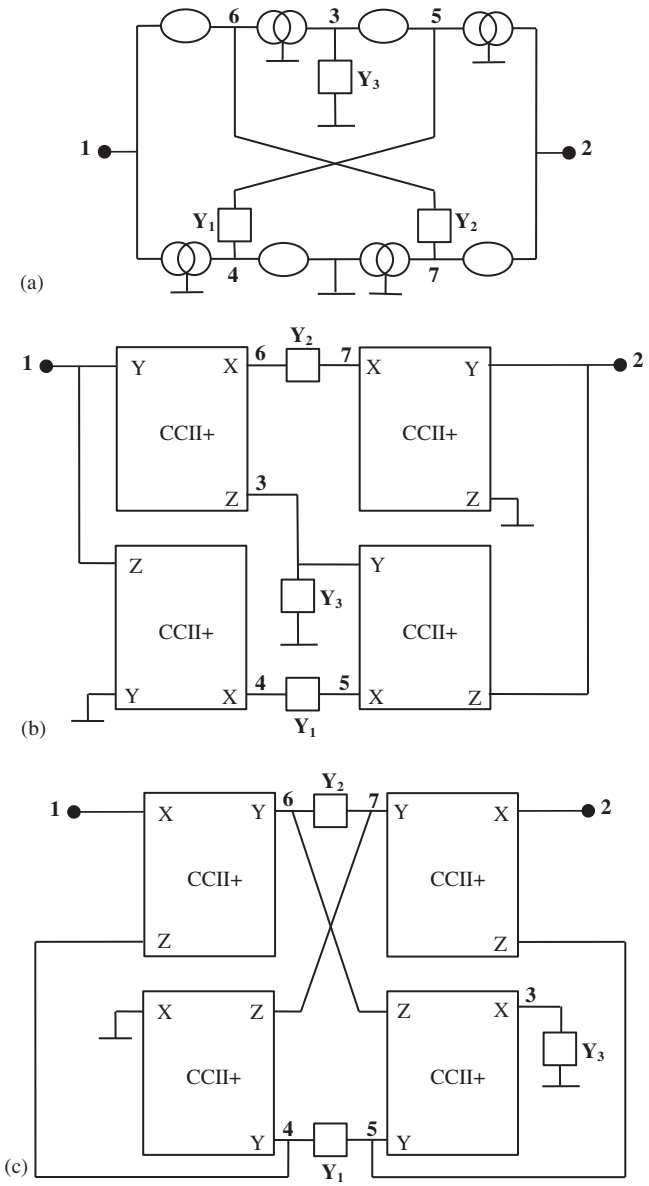

Figure 5. (a) The nullor–mirror circuit for the NAM in Equation (9); (b) and (c) equivalent CCII-based realizations.

Y_1 and Y_2 will be two actual capacitors connected at two Y–Z-terminals and Y_3 will be a conductance connected at an X-terminal. A simulated floating inductance using the circuit in Figure 5(b) has been reported before in [3, 14], whereas, a novel CCII-based floating wide-band FDNR can be obtained using the circuit in Figure 5(c).

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The balanced output CCII [11] is a four-port active device which is defined by the following matrix equation

$$\begin{bmatrix} I_Y \\ V_X \\ I_{Z+} \\ I_{Z-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & -1 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_{Z+} \\ V_{Z-} \end{bmatrix} \tag{10}$$

The symbolic and pathological representations of the balanced output CCII are shown in Figure 6. The pathological representation of the balanced output CCII can be ideally described in a NAM (by combining the NAM representations of the CCII+ and the CCII−) using infinity-variables as follows

$$\begin{array}{c} \\ X \\ Z+ \\ Z- \end{array} \begin{array}{c} \begin{array}{cccc} X & & Y & \end{array} \\ \begin{bmatrix} \ddots & \vdots & \cdots & -\infty_i & \vdots \\ \cdots & \infty_i & \cdots & -\infty_i & \cdots \\ \vdots & \infty_i & \cdots & -\infty_i & \vdots \\ \cdots & -\infty_i & \cdots & \infty_i & \ddots \end{bmatrix} \end{array} \tag{11}$$

Using the above NAM representation for the balanced output CCII, the extra expansion steps introduced in Equation (9) to represent a floating admittance Y_2 using the $\pm Y_2$ terms in Equation (8) can be replaced by the following expansion scheme

$$\begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ -\infty_1 & 0 & 0 & 0 & 0 & \infty_1 \\ -Y_2+\infty_1 & Y_2 & Y_3 & 0 & 0 & -\infty_1 \\ 0 & 0 & 0 & Y_1 & -Y_1 & 0 \\ 0 & 0 & 0 & -Y_1 & Y_1 & 0 \\ \infty_1 & 0 & 0 & 0 & 0 & -\infty_1 \end{bmatrix} \equiv \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ -\infty_1 & Y_2 & 0 & 0 & 0 & -Y_2+\infty_1 \\ \infty_1 & 0 & Y_3 & 0 & 0 & -\infty_1 \\ 0 & 0 & 0 & Y_1 & -Y_1 & 0 \\ 0 & 0 & 0 & -Y_1 & Y_1 & 0 \\ \infty_1 & -Y_2 & 0 & 0 & 0 & Y_2-\infty_1 \end{bmatrix} \tag{12}$$

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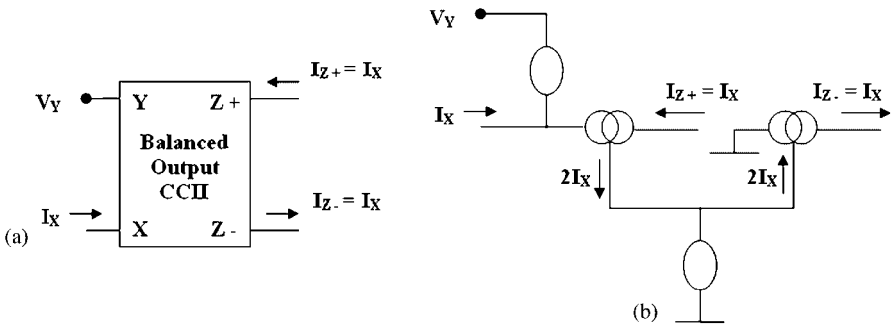

Figure 6. The balanced output CCII: (a) symbol and (b) nullor-mirror representation.

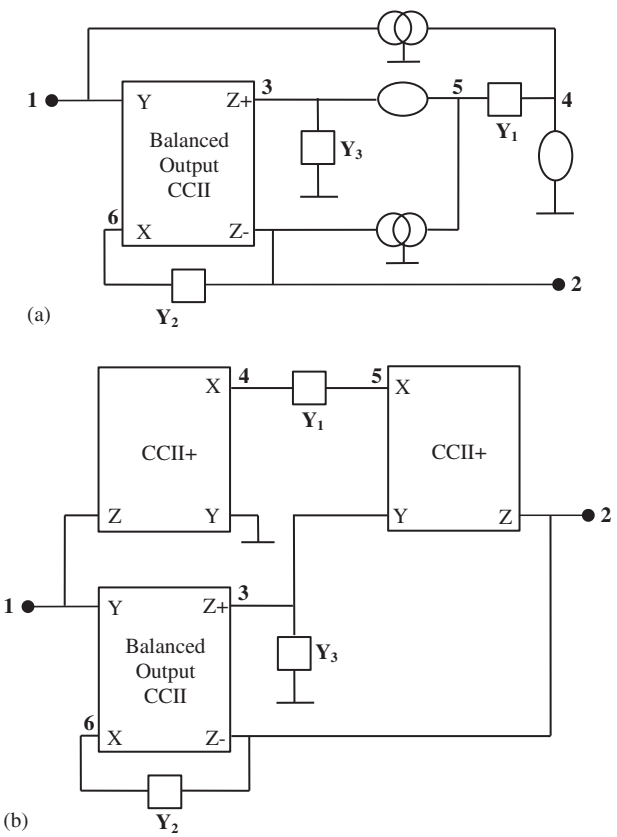

Figure 7. (a) The nullor–mirror circuit described by Equation (12) and (b) equivalent CCII-based realization.

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Now, the $\pm Y_2$ terms in Equation (12) represent a floating admittance Y_2 connected between nodes 2 and 6. Although the nullators and current mirrors are represented using the bracket notation, which is more suitable for synthesis [4], the balanced output CCII is represented in the NAM using the infinity-variables so that to distinguish between the ideal representation of the balanced output CCII and the other nullor–mirror elements. The resulting nullor–mirror circuit described by Equation (12) is shown in Figure 7(a). On mapping the pathological pairs in Figure 7(a) with their equivalent types of current conveyors, a novel floating simulator realization using a balanced output CCII and two CCIIs positive is obtained, as drawn in Figure 7(b). For a wide bandwidth, the novel CCII-based floating simulator in Figure 7(b) can better simulate a floating coil than an FDNR.

The active building-block in Figure 8(a) is a special case from the fully differential CCII (FDCCII) introduced in [12] and it has been republished under the name dual-X CCII in [13], without referring to [12]. It is a five-port active device which is defined by the following matrix equation

$$\begin{bmatrix} I_Y \\ V_{X_1} \\ V_{X_2} \\ I_{Z_1} \\ I_{Z_2} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ -1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} V_Y \\ I_{X_1} \\ I_{X_2} \end{bmatrix} \tag{13}$$

The pathological representation of the dual-X CCII is shown in Figure 8(b). The nullator, voltage mirror, and two current mirrors in the ideal description of the dual-X CCII can be used to expand the matrix in Equation (5), so that the $\pm Y_1$ terms represent a floating admittance $Y_{1/2}$ connected between nodes 4 and 5 as follows:

$$\begin{bmatrix} 0 & 0 & \left(\frac{Y_1}{2}\right)+\left(\frac{Y_1}{2}\right) & 0 & 0 \\ 0 & 0 & \left(\frac{-Y_1}{2}\right)+\left(\frac{-Y_1}{2}\right) & 0 & 0 \\ -Y_2 & Y_2 & Y_3 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix} \equiv \begin{bmatrix} 0 & 0 & 0 & \frac{-Y_1}{2} & \frac{Y_1}{2} \\ 0 & 0 & 0 & \frac{Y_1}{2} & \frac{-Y_1}{2} \\ -Y_2 & Y_2 & Y_3 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix}$$

$$\equiv \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ -Y_2 & Y_2 & Y_3 & 0 & 0 \\ 0 & 0 & 0 & \frac{Y_1}{2} & \frac{-Y_1}{2} \\ 0 & 0 & 0 & \frac{-Y_1}{2} & \frac{Y_1}{2} \end{bmatrix} \tag{14}$$

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Then, the $\pm Y_2$ terms can represent a floating admittance Y_2 using the expansion steps in Equation (9) or (12), resulting in the expanded NAMs in Equation (15) and (16), respectively.

$$
\begin{bmatrix}
0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 \\
-Y_2 & Y_2 & Y_3 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & Y_1/2 & -Y_1/2 & 0 & 0 \\
0 & 0 & 0 & -Y_1/2 & Y_1/2 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0
\end{bmatrix}
\equiv
\begin{bmatrix}
0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & 0 & Y_3 & 0 & 0 & 0 & 0 \\
0 & 0 & 0 & Y_1/2 & -Y_1/2 & 0 & 0 \\
0 & 0 & 0 & -Y_1/2 & Y_1/2 & 0 & 0 \\
0 & 0 & 0 & 0 & 0 & Y_2 & -Y_2 \\
0 & 0 & 0 & 0 & 0 & -Y_2 & Y_2
\end{bmatrix}
\tag{15}
$$

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$$
\begin{bmatrix}
0 & 0 & 0 & 0 & 0 & 0 \\
-\infty_1 & 0 & 0 & 0 & 0 & \infty_1 \\
-Y_2+\infty_1 & Y_2 & Y_3 & 0 & 0 & -\infty_1 \\
0 & 0 & 0 & Y_1/2 & -Y_1/2 & 0 \\
0 & 0 & 0 & -Y_1/2 & Y_1/2 & 0 \\
\infty_1 & 0 & 0 & 0 & 0 & -\infty_1
\end{bmatrix}
\equiv
\begin{bmatrix}
0 & 0 & 0 & 0 & 0 & 0 \\
-\infty_1 & Y_2 & 0 & 0 & 0 & -Y_2+\infty_1 \\
\infty_1 & 0 & Y_3 & 0 & 0 & -\infty_1 \\
0 & 0 & 0 & Y_1/2 & -Y_1/2 & 0 \\
0 & 0 & 0 & -Y_1/2 & Y_1/2 & 0 \\
\infty_1 & -Y_2 & 0 & 0 & 0 & Y_2-\infty_1
\end{bmatrix}
\tag{16}
$$

Note that in Equation (15), the brackets representing the dual-X CCII are drawn using continuous lines, while the brackets representing other nullor–mirror elements are drawn using dashed lines, so that to distinguish them. The nullor–mirror circuit described by expanded NAM in Equation (15) and its equivalent CCII-based circuit and the simulator circuit represented by the NAM in Equation (16) are shown in Figures 9 and 10, respectively. If the resulting CCII-based circuits are used to simulate wide-band floating coils, then the $Y_{1/2}$ admittance will be a conductance $G_{1/2}$ connected between the two X-terminals of the dual-X CCII. It has been shown in [13] that the balanced differential voltage between the X-terminals of the dual-X CCII can cancel the even-order nonlinearities caused by triode NMOS transistors. Hence, the conductance $G_{1/2}$ to be connected between the two X-terminals can be realized by a triode NMOS transistor M_1 and its value is controlled by the gate voltage V_G, such that

$$G_{1/2}=2\mu_n C_{\text{ox}}(W/L)(V_G-V_{Tn}) \tag{17}$$

where V_{Tn} is the NMOS transistor threshold voltage. The resulting two novel simulated floating coils are shown in Figure 11. Although the value of the equivalent resistance for the conductance $G_{1/2}$ is double the resistance used in the previous realizations of Figures 5 and 7 (equivalent to conductance G_1) to obtain the same value of simulated inductance, but the CCII-based realizations in Figure 11 offer the advantage of reducing the number of passive elements by using a triode NMOS transistor, without suffering from nonlinearities, to realize $G_{1/2}$. Thus, these simulated floating coils are more amenable to monolithic integration. Also, the value of $G_{1/2}$, and hence the value of the simulated inductance, can be controlled using V_G. Therefore, in addition to the advantage of wide bandwidth, the two circuits in Figures 9(b) and 10 can better simulate a floating inductance so that to benefit from the advantages given by using the dual-X CCII in terms of monolithic implementation on chip and tunability.

DOI: 10.1002/cta

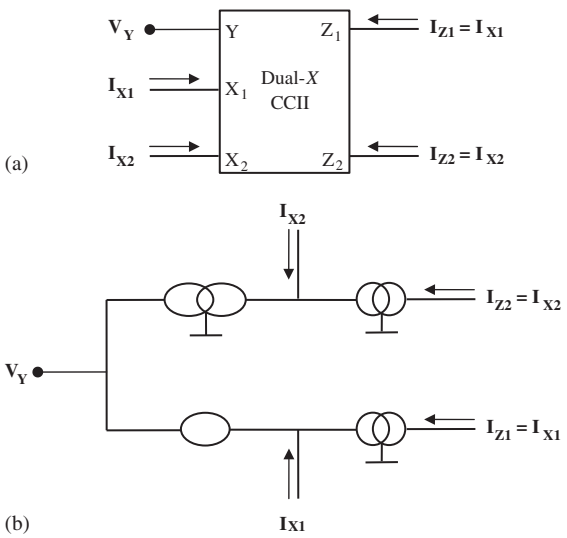

Figure 8. The dual-*X* CCII: (a) symbolic representation and (b) pathological representation.

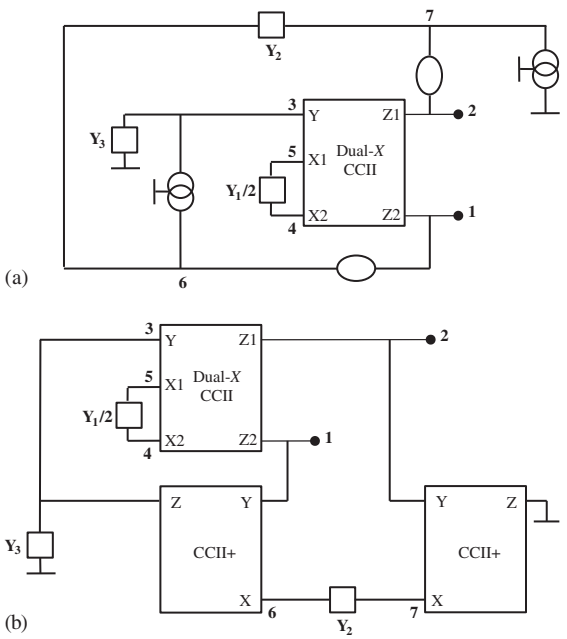

Figure 9. (a) The nullor–mirror circuit described by expanded NAM in Equation (15) and (b) equivalent CCII-based circuit.

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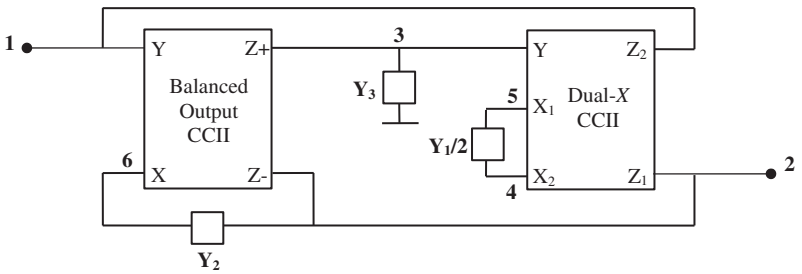

Figure 10. The CCII-based floating simulator circuit represented by the NAM in Equation (16).

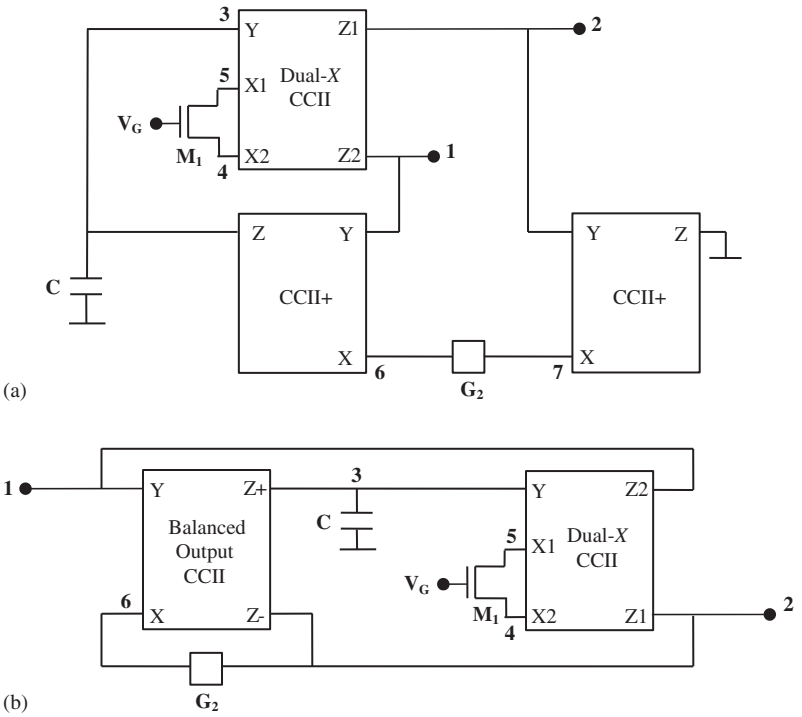

Figure 11. (a) Voltage-controlled simulated floating coil based on the circuit in Figure 9(b) and (b) voltage-controlled simulated floating coil based on the circuit in Figure 10.

Comparing the two floating inductance simulators in Figure 11 with each other, the circuit in Figure 11(b) is shown to be more optimized in terms of number of active elements, because two CCII+s in Figure 11(a) are replaced by a single balanced output CCII in Figure 11(b). Although the balanced output CCII has more terminals than the CCII+, but they share the same core feeding their common terminals, and hence the additional active devices in the balanced output CCII, introduced by the extra Z-terminal, are less than the active devices in a complete CCII+.

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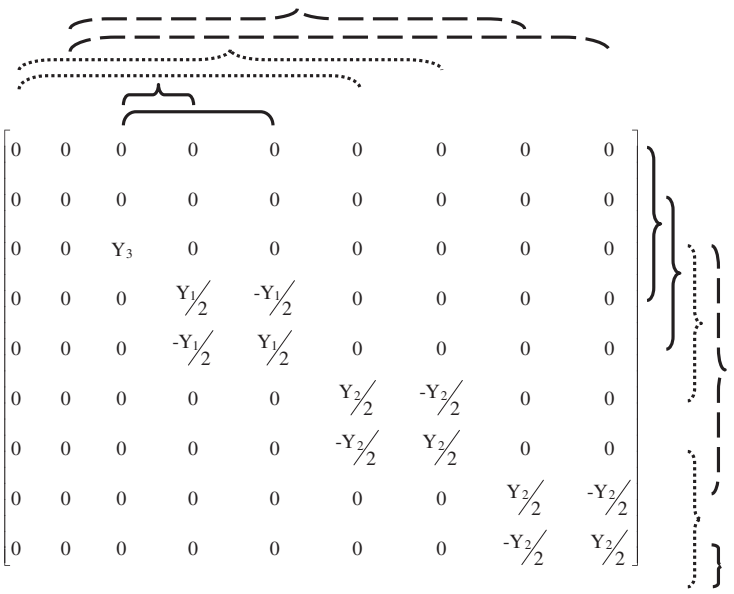
The NAM in Equation (14) can be expanded in an alternative way, such that two dual-X CCIIs are used to move the $\pm Y_2$ terms so that they represent two floating Y_2 admittances as follows:



$$\begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & Y_3 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & Y_1/2 & -Y_1/2 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -Y_1/2 & Y_1/2 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & Y_2/2 & -Y_2/2 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & -Y_2/2 & Y_2/2 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & Y_2/2 & -Y_2/2 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & -Y_2/2 & Y_2/2 \end{bmatrix} \tag{18}$$

where every set of brackets, drawn using the same line type, represents a single dual-X CCII. The equivalent CCII-based circuit described by the NAM in Equation (18) is shown in Figure 12. The dual-X CCII-based circuit in Figure 12 can be used to simulate a novel resistorless wide-band floating inductance that can be tuned by varying the voltage on the gates of the NMOS transistors connected between the X-terminals of every CCII. Thus, this circuit is more suitable for monolithic integration than those in Figure 11 because it is free of resistors. Also, this circuit offers a wider tuning range for the value of the simulated inductance because the values of the two equivalent conductances realized by M_1, M_2, and M_3 can be tuned independently by varying the gate voltages V_{G1} and V_{G2}. These advantages come at the expense of using a larger number of active devices, where three dual-X CCIIs are used in the circuit realization. It is known that the dual-X CCII is a large active device with many terminals and contains many transistors. The matching requirement imposed on the two transistors M_2 and M_3 cannot be considered a basic drawback for this circuit because satisfying matching conditions for active devices on chip can be achieved normally by today's monolithic technologies. Also, the realizations of the CCII devices used in the circuits already contain current-mirrors and differential-pairs, which impose matching requirements as well.

3.2. *Floating Y_2 (or Y_1) and grounded Y_1 (or Y_2)*

In this class of floating simulators, the same expansion steps used to move the $\pm Y_2$ terms in the previous class can be used, because Y_2 is floating in both classes. The difference between the two classes is that Y_1 was floating in the previous class while it will be grounded in this one. The NAM in Equation (3) can be expanded using the infinity-variables representation of the balanced

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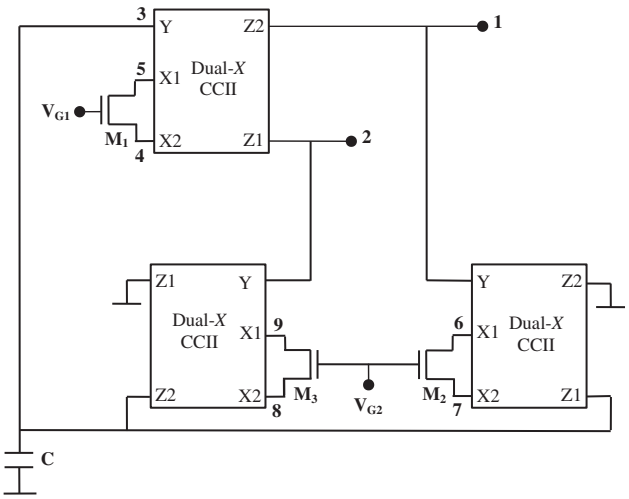

Figure 12. Novel resistorless simulated floating inductance circuit.

output CCII, so that the $\pm Y_1$ terms represent a grounded admittance Y_1 as follows:

$$\begin{bmatrix} 0 & 0 & Y_1 & 0 \\ 0 & 0 & -Y_1 & 0 \\ -Y_2 & Y_2 & Y_3 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix} \equiv \begin{bmatrix} 0 & 0 & Y_1+\infty_1 & -\infty_1 \\ 0 & 0 & -Y_1-\infty_1 & \infty_1 \\ -Y_2 & Y_2 & Y_3 & 0 \\ 0 & 0 & -\infty_1 & \infty_1 \end{bmatrix} \equiv \begin{bmatrix} 0 & 0 & \infty_1 & -\infty_1 \\ 0 & 0 & -\infty_1 & \infty_1 \\ -Y_2 & Y_2 & Y_3 & 0 \\ 0 & 0 & Y_1-\infty_1 & \infty_1 \end{bmatrix}$$

$$\equiv \begin{bmatrix} 0 & 0 & \infty_1 & -\infty_1 \\ 0 & 0 & -\infty_1 & \infty_1 \\ -Y_2 & Y_2 & Y_3 & 0 \\ 0 & 0 & -\infty_1 & Y_1+\infty_1 \end{bmatrix} \tag{19}$$

The next step is to expand the NAM in Equation (19), so that the $\pm Y_2$ terms represent a floating Y_2 admittance. In order to realize optimized CCII-based simulator circuits with reasonable number of active devices, the NAM in Equation (19) can be expanded using the expansion steps in Equation (9) or (12), yielding the final expanded NAMs in Equation (20) or (21), respectively.

$$\begin{bmatrix} 0 & 0 & \infty_1 & -\infty_1 & 0 & 0 \\ 0 & 0 & -\infty_1 & \infty_1 & 0 & 0 \\ -Y_2 & Y_2 & Y_3 & 0 & 0 & 0 \\ 0 & 0 & -\infty_1 & Y_1+\infty_1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \equiv \begin{bmatrix} 0 & 0 & \infty_1 & -\infty_1 & 0 & 0 \\ 0 & 0 & -\infty_1 & \infty_1 & 0 & 0 \\ 0 & 0 & Y_3 & 0 & 0 & 0 \\ 0 & 0 & -\infty_1 & Y_1+\infty_1 & 0 & 0 \\ 0 & 0 & 0 & 0 & Y_2 & -Y_2 \\ 0 & 0 & 0 & 0 & -Y_2 & Y_2 \end{bmatrix} \tag{20}$$

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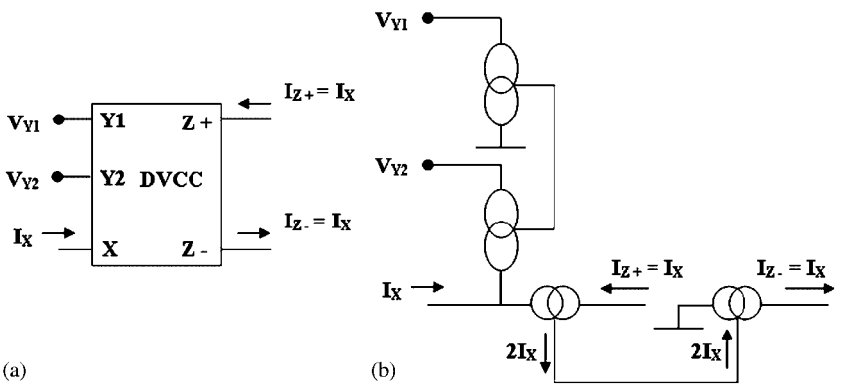

Figure 13. The differential voltage current conveyor: (a) symbol and (b) nullor–mirror representation.

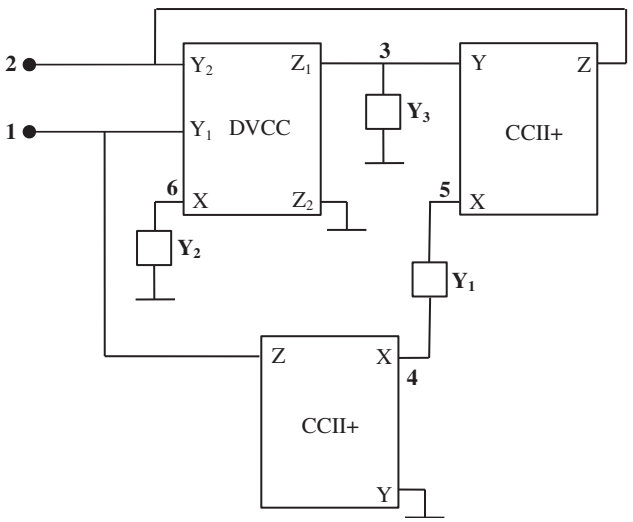

Figure 14. Novel floating simulator circuit using a single DVCC and two CCII+s.

$$\begin{bmatrix} 0 & 0 & \infty_1 & -\infty_1 & 0 \\ -\infty_2 & 0 & -\infty_1 & \infty_1 & \infty_2 \\ -Y_2+\infty_2 & Y_2 & Y_3 & 0 & -\infty_2 \\ 0 & 0 & -\infty_1 & Y_1+\infty_1 & 0 \\ \infty_2 & 0 & 0 & 0 & -\infty_2 \end{bmatrix} \equiv \begin{bmatrix} 0 & 0 & \infty_1 & -\infty_1 & 0 \\ -\infty_2 & Y_2 & -\infty_1 & \infty_1 & -Y_2+\infty_2 \\ \infty_2 & 0 & Y_3 & 0 & -\infty_2 \\ 0 & 0 & -\infty_1 & Y_1+\infty_1 & 0 \\ \infty_2 & -Y_2 & 0 & 0 & Y_2-\infty_2 \end{bmatrix} \tag{21}$$

The CCII-based floating simulator circuit represented by the NAMs in Equation (20) has been reported in [15], but the CCIIs were replaced by second-generation current controlled conveyors

DOI: 10.1002/cta

(CCCIIs) to obtain a resistorless simulated floating inductor. Also, the circuit represented by the NAM in Equation (21) has been proposed in [16] to simulate a floating inductance using a grounded capacitance.

The symbolic and pathological representations of the differential voltage current conveyor (DVCC) [10] are shown in Figure 13. The DVCC can be ideally represented in a NAM using infinity-variables as follows:

$$\begin{array}{c} \\ X \\ Z_1 \\ Z_2 \end{array} \begin{array}{c} \begin{array}{ccccc} X & & Y_1 & & Y_2 \end{array} \\ \begin{bmatrix} \ddots & \vdots & \cdots & \vdots & \cdots & \vdots & \ddots \\ \cdots & \infty_i & \cdots & -\infty_i & \cdots & \infty_i & \cdots \\ \cdots & \infty_i & \cdots & -\infty_i & \cdots & \infty_i & \cdots \\ \cdots & -\infty_i & \cdots & \infty_i & \cdots & -\infty_i & \cdots \\ \ddots & \vdots & \cdots & \vdots & \cdots & \vdots & \ddots \end{bmatrix} \end{array} \tag{22}$$

The NAM in Equation (8) can be expanded using the NAM representation for the DVCC to obtain a grounded Y_2 as follows:

$$\begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ -Y_2+\infty_1 & Y_2-\infty_1 & Y_3 & 0 & 0 & -\infty_1 \\ 0 & 0 & 0 & Y_1 & -Y_1 & 0 \\ 0 & 0 & 0 & -Y_1 & Y_1 & 0 \\ \infty_1 & -\infty_1 & 0 & 0 & 0 & -\infty_1 \end{bmatrix} \equiv \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ \infty_1 & -\infty_1 & Y_3 & 0 & 0 & -Y_2-\infty_1 \\ 0 & 0 & 0 & Y_1 & -Y_1 & 0 \\ 0 & 0 & 0 & -Y_1 & Y_1 & 0 \\ \infty_1 & -\infty_1 & 0 & 0 & 0 & -\infty_1 \end{bmatrix}$$

$$\equiv \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ \infty_1 & -\infty_1 & Y_3 & 0 & 0 & -\infty_1 \\ 0 & 0 & 0 & Y_1 & -Y_1 & 0 \\ 0 & 0 & 0 & -Y_1 & Y_1 & 0 \\ \infty_1 & -\infty_1 & 0 & 0 & 0 & Y_2-\infty_1 \end{bmatrix} \tag{23}$$

The novel CCII-based floating simulator represented by the NAM in Equation (23) is shown in Figure 14.

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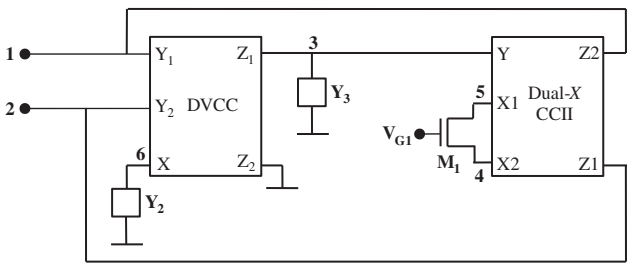

Figure 15. Novel floating simulator circuit using a DVCC and a dual-X CCII.

Another synthesis solution, starting from the NAM in Equation (3), can be obtained using a dual-X CCII to move the $\pm Y_1$ and a DVCC to move the $\pm Y_2$ terms as follows:

$$\begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ \infty_1 & -\infty_1 & Y_3 & 0 & 0 & -\infty_1 \\ 0 & 0 & 0 & Y_1/2 & -Y_1/2 & 0 \\ 0 & 0 & 0 & -Y_1/2 & Y_1/2 & 0 \\ \infty_1 & -\infty_1 & 0 & 0 & 0 & Y_2-\infty_1 \end{bmatrix} \tag{24}$$

The CCII-based floating simulator represented by the NAM in Equation (24) is shown in Figure 15. This circuit is better than the one in Figure 14 because it has no floating passive elements and the value of the floating simulator can be tuned electronically using the control voltage at the gate of M_1.

3.3. Grounded Y_1 and Y_2

The most optimized combination of CCII devices to obtain a CCII-based floating simulator using grounded admittances Y_1, Y_2, and Y_3 from the NAM in Equation (3) is to use a balanced output CCII to represent a grounded admittance Y_1 and use a DVCC to represent grounded admittance Y_2. The NAM in Equation (3) can be expanded using the infinity-variable representation of the

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balanced output CCII to obtain a grounded Y_1 using the $\pm Y_1$ terms as follows:

$$\begin{bmatrix} 0 & 0 & Y_1 & 0 & 0 \\ 0 & 0 & -Y_1 & 0 & 0 \\ -Y_2 & Y_2 & Y_3 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix} \equiv \begin{bmatrix} 0 & 0 & Y_1+\infty_1 & -\infty_1 & 0 \\ 0 & 0 & -Y_1-\infty_1 & \infty_1 & 0 \\ -Y_2 & Y_2 & Y_3 & 0 & 0 \\ 0 & 0 & -\infty_1 & \infty_1 & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix}$$

$$\equiv \begin{bmatrix} 0 & 0 & \infty_1 & Y_1-\infty_1 & 0 \\ 0 & 0 & -\infty_1 & -Y_1+\infty_1 & 0 \\ -Y_2 & Y_2 & Y_3 & 0 & 0 \\ 0 & 0 & -\infty_1 & \infty_1 & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix}$$

$$\equiv \begin{bmatrix} 0 & 0 & \infty_1 & -\infty_1 & 0 \\ 0 & 0 & -\infty_1 & \infty_1 & 0 \\ -Y_2 & Y_2 & Y_3 & 0 & 0 \\ 0 & 0 & -\infty_1 & Y_1+\infty_1 & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix} \tag{25}$$

The above NAM can be expanded further using the infinity-variable representation for the DVCC so that the $\pm Y_2$ terms represent a grounded admittance Y_2 as follows:

$$\begin{bmatrix} 0 & 0 & \infty_1 & -\infty_1 & 0 \\ 0 & 0 & -\infty_1 & \infty_1 & 0 \\ -Y_2+\infty_2 & Y_2-\infty_2 & Y_3 & 0 & -\infty_2 \\ 0 & 0 & -\infty_1 & Y_1+\infty_1 & 0 \\ \infty_2 & -\infty_2 & 0 & 0 & -\infty_2 \end{bmatrix}$$

$$\equiv \begin{bmatrix} 0 & 0 & \infty_1 & -\infty_1 & 0 \\ 0 & 0 & -\infty_1 & \infty_1 & 0 \\ \infty_2 & -\infty_2 & Y_3 & 0 & -Y_2-\infty_2 \\ 0 & 0 & -\infty_1 & Y_1+\infty_1 & 0 \\ \infty_2 & -\infty_2 & 0 & 0 & -\infty_2 \end{bmatrix}$$

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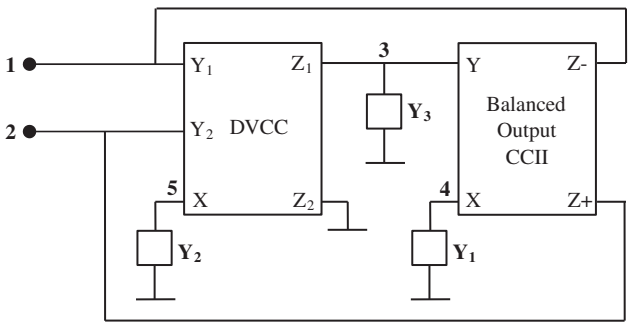

Figure 16. Novel floating simulator circuit using a DVCC and a balanced output CCII.

$$\equiv \begin{bmatrix} 0 & 0 & \infty_1 & -\infty_1 & 0 \\ 0 & 0 & -\infty_1 & \infty_1 & 0 \\ \infty_2 & -\infty_2 & Y_3 & 0 & -\infty_2 \\ 0 & 0 & -\infty_1 & Y_1+\infty_1 & 0 \\ \infty_2 & -\infty_2 & 0 & 0 & Y_2-\infty_2 \end{bmatrix} \tag{26}$$

The circuit described by the NAM in Equation (26) is depicted in Figure 16. This circuit is better than the one in Figure 15 in terms of active devices because, usually, the balanced output CCII comprises less number of MOS transistors than the dual-X CCII, but on the other hand, the circuit in Figure 15 contains only two grounded passive elements and can be tuned electronically.

4. NONIDEAL EFFECTS

Up to this point, the paper has been concerned with synthesis of CCII-based floating simulators taking into consideration only the parasitic components experienced at device terminals. However, there are other nonidealities associated with typical CCII devices represented in voltage and current tracking errors between the Y and X terminals and the X and Z terminals, respectively. In essence, these tracking errors show up as nonunity voltage and current gains between the Y and X terminals and X and Z terminals, respectively. According to the basic definition of infinity-variables [5], these nonunity gains can be represented in the NAM by including the nonideal tracking gains as coefficients for infinity-variables occupying the column corresponding to the Y-terminal (in case of voltage gain error) and the rows occupying the row corresponding to the X-terminal (in case of current gain error). As a simple example, consider the circuit represented by the NAM in (26). Suppose that the balanced output CCII has a voltage transfer error between Y and X terminals and current transfer error between X and Z terminals, such that the

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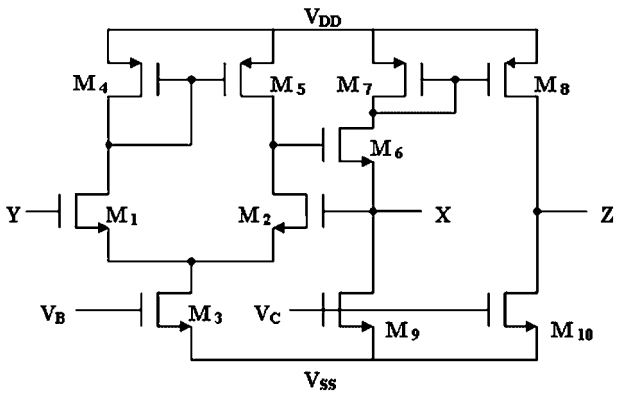

Figure 17. The long tail pair based CCII+ realization reported in [17].

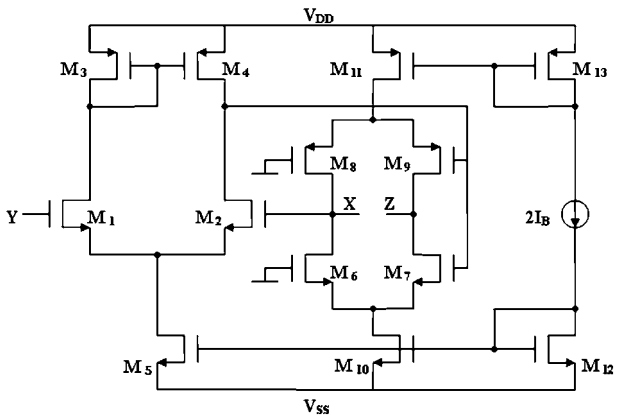

Figure 18. The FCS based CCII− realization reported in [18].

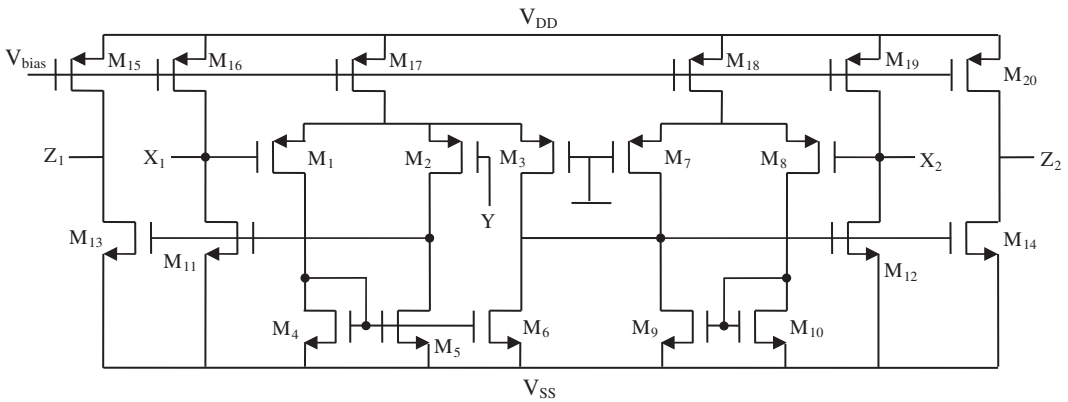

Figure 19. The dual-*X* CCII realization reported in [13].

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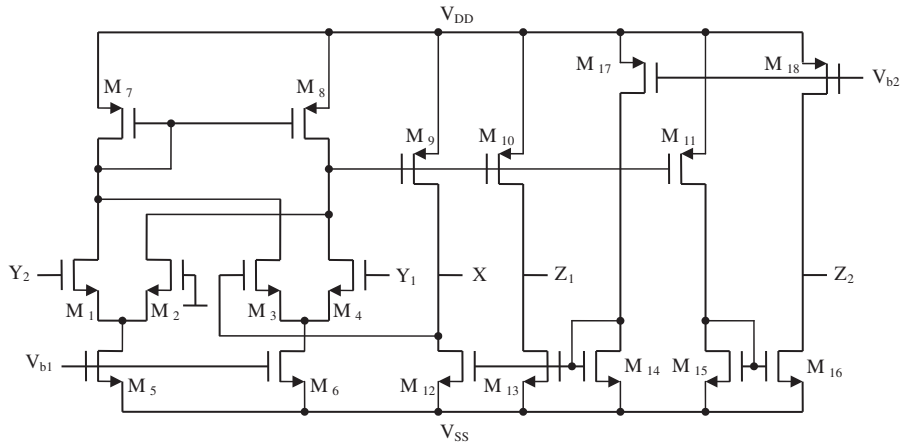

Figure 20. The DVCC realization reported in [10].

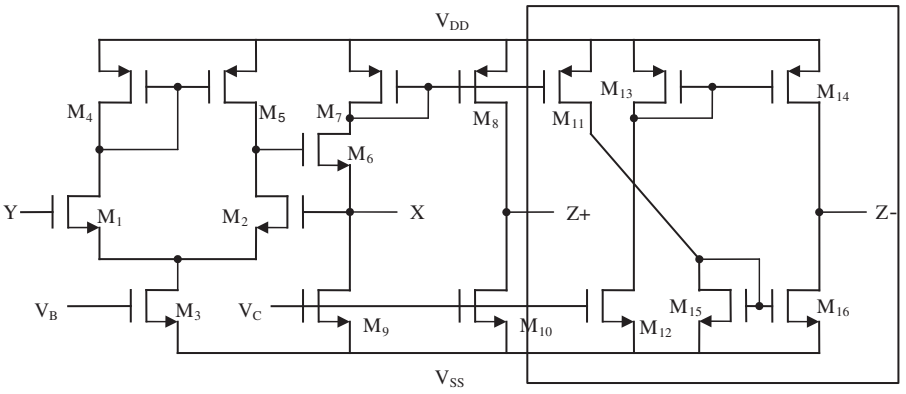

Figure 21. Balanced output CCII realization.

Table I. Dimensions of the MOS transistors in the CCII+ of Figure 17.

NMOS transistors	W (μm)/L (μm)
M_1 and M_2	25/0.5
M_3	8/0.5
M_6	14/0.5
M_9 and M_{10}	4/0.5
PMOS transistors	W (μm)/L (μm)
M_4, M_5, M_7, and M_8	10/0.5

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Table II. Dimensions of the MOS transistors in the CCII− of Figure 18.

NMOS transistors	W (μm)/L (μm)
M_1 and M_2	25/0.5
M_5	20/0.5
M_6 and M7	10/0.5
M_{10} and M_{12}	30/0.75
PMOS transistors	W (μm)/L (μm)
M_3 and M_4	30/1.5
M_8 and M_9	10/0.5
M_{11} and M_{13}	30/0.75

Table III. Dimensions of the MOS transistors in the dual-X CCII of Figure 19.

NMOS transistors	W (μm)/L (μm)
M_4 and M_5	1.5/0.5
M_6, M_9, and M_{10}	3/0.5
M_{11}, M_{12}, M_{13}, and M_{14}	6/0.5
PMOS transistors	W (μm)/L (μm)
M_1 and M_2	1/0.5
M_3, M_7, and M_8	2/0.5
M_{15}, M_{16}, M_{19}, and M_{20}	6/0.5
M_{17} and M_{18}	12/0.5

Table IV. Dimensions of the MOS transistors in the DVCC of Figure 20.

NMOS transistors	W (μm)/L (μm)
M_1, M_2, M_3 and M_4	25/0.5
M_5 and M_6	8/0.5
M_{12}, M_{13}, M_{14}, M_{15}, and M_{16}	4/0.5
PMOS transistors	W (μm)/L (μm)
M_7, M_8, M_9, M_{10}, M_{11}, M_{17}, and M_{18}	10/0.5

Table V. Dimensions of the MOS transistors in the balanced output CCII of Figure 21.

NMOS transistors	W (μm)/L (μm)
M_1 and M_2	25/0.5
M_3	8/0.5
M_6	14/0.5
M_9 and M_{10}	4/0.5
M_{15} and M_{16}	4/4
PMOS transistors	W (μm)/L (μm)
M_4, M_5, M_7, and M_8	10/0.5
M_{13} and M_{14}	10/4

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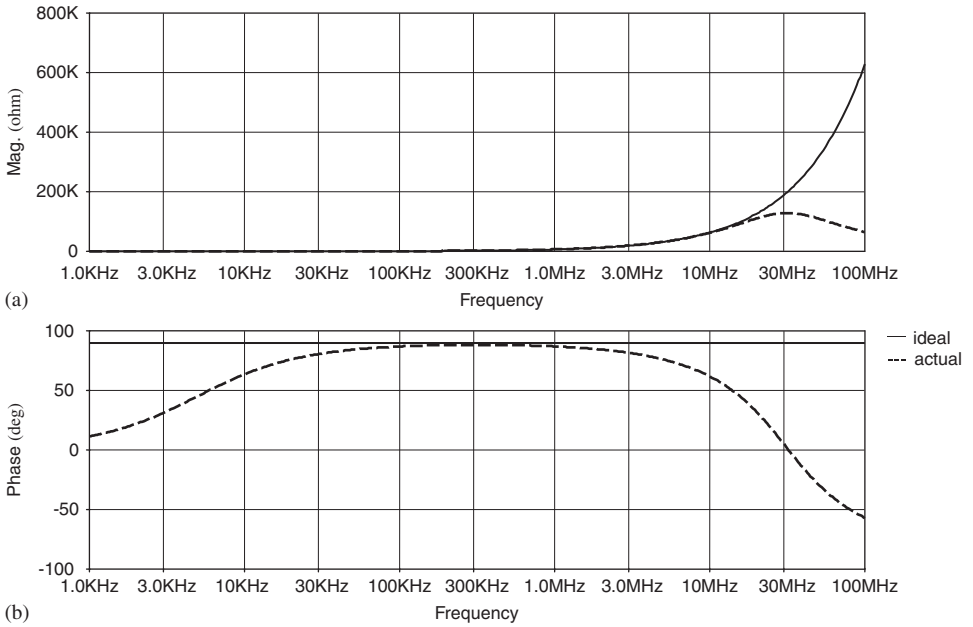

Figure 22. Magnitude and phase responses for the impedance of a 1 mH floating inductance realized using the circuit in Figure 7(b).

actual characteristics of the balanced output CCII are given by the following equation

$$\begin{bmatrix} I_Y \\ V_X \\ I_{Z+} \\ I_{Z-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ \alpha & 0 & 0 & 0 \\ 0 & \beta & 0 & 0 \\ 0 & -\beta & 0 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_{Z+} \\ V_{Z-} \end{bmatrix} \tag{27}$$

where α and β are not equal to unity. These nonunity transfer gains will cause the operation of the actual balanced output CCII device to deviate from the ideal operation according to how much these values are far from the ideal unity gains. This effect can be easily incorporated into the NAM representation as follows:

$$\equiv \begin{bmatrix} 0 & 0 & \alpha\infty_1 & -\infty_1 & 0 \\ 0 & 0 & -\alpha\infty_1 & \infty_1 & 0 \\ \infty_2 & -\infty_2 & Y_3 & 0 & -\infty_2 \\ 0 & 0 & -\alpha\beta\infty_1 & Y_1+\beta\infty_1 & 0 \\ \infty_2 & -\infty_2 & 0 & 0 & Y_2-\infty_2 \end{bmatrix} \tag{28}$$

Then, the actual performance of the circuit, considering the transfer errors between the actual device terminals, can be easily predicted analytically from the NAM representation obtained after including

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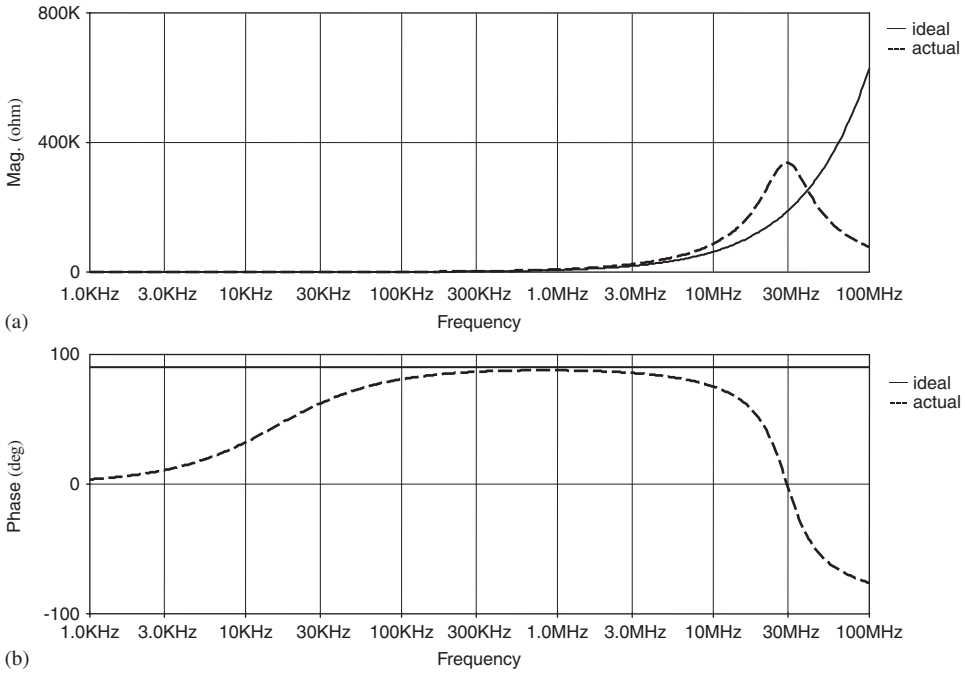

Figure 23. Magnitude and phase responses for the impedance of a 1 mH floating inductance realized using the simulated coil in Figure 11(a).

the nonideal gain effects. The actual values of α and β depend on the actual implementation of the device (transistor level) and can be obtained from characterization measurements carried on by simulations or experimental characterization of device prototypes.

However, in the process of designing CCII-based circuits, such types of errors are not considered in the design phase. In essence, CCII devices are usually designed and implemented with very small (almost negligible) gain tracking error and the transfer gains are almost unity in the bands of interest. The main concern is the parasitic elements associated with the actual device terminals, which have been discussed in details in Section 2. Recall that parasitic elements at device terminals give rise to parasitic poles and zeros resulting in lower frequency limit and upper frequency limit for the proper operation of the circuit such that the circuit performance is significantly deteriorated out of this band. Detailed analysis for calculating the lower and upper frequency limit from the NAM representation has been given in [8]. This effect will be illustrated clearly in the simulations given in the next section, especially in the phase responses of the simulated circuits. However, the resulting responses are aligned with typical performances achieved for floating simulator circuits in terms of phase and magnitude response.

5. SIMULATION RESULTS

In this section, SPICE simulations are performed to demonstrate the performance of the novel CCII-based floating simulators synthesized in the previous section. The circuits are simulated

DOI: 10.1002/cta

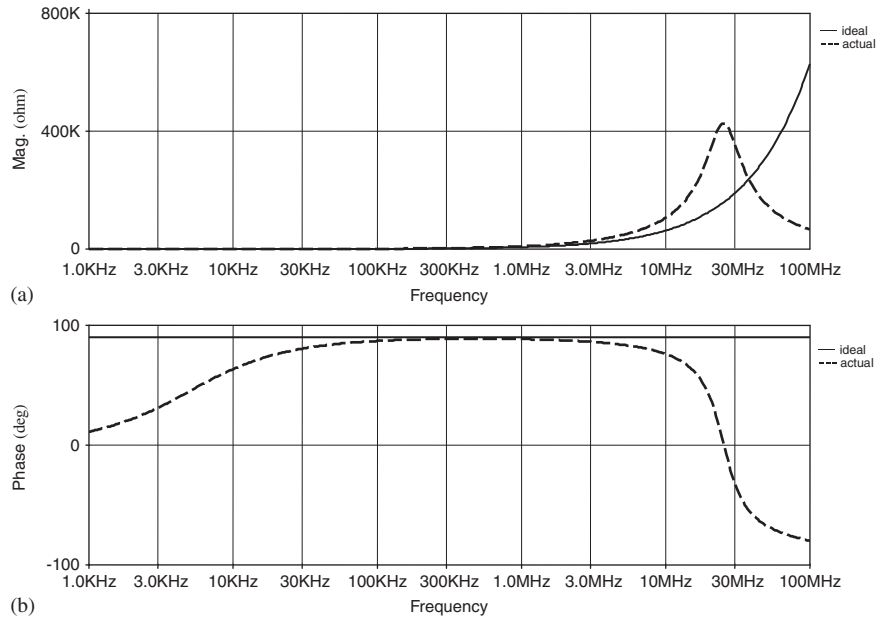

Figure 24. Magnitude and phase responses for the impedance of a 1 mH floating inductance realized using the simulated coil in Figure 11(b).

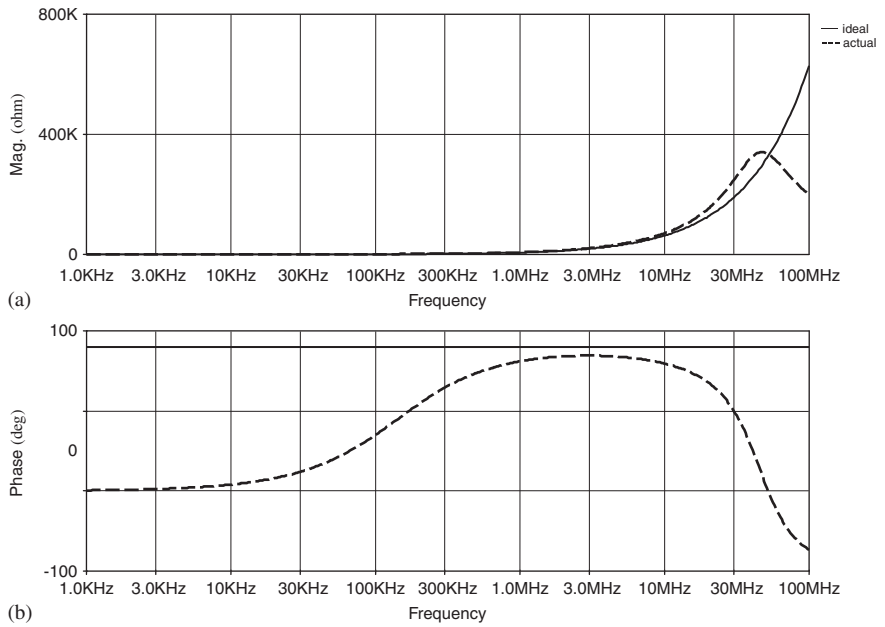

Figure 25. Magnitude and phase responses for the impedance of a 1 mH floating inductance realized using the resistorless simulated inductance in Figure 12.

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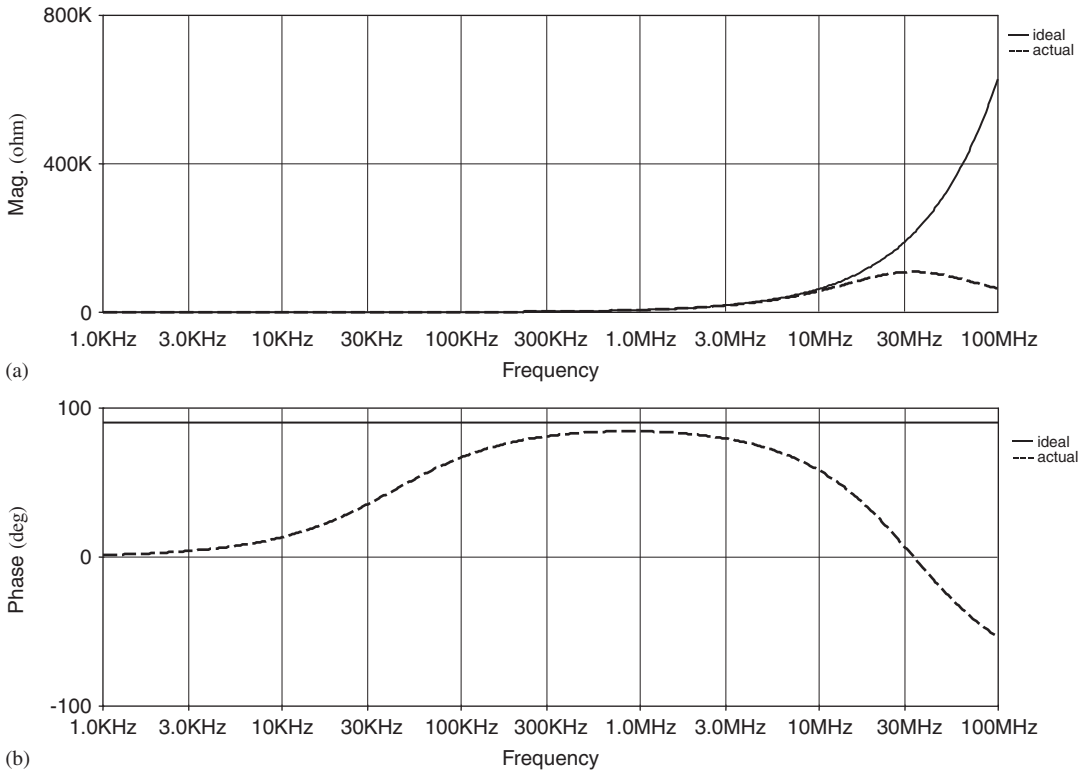

Figure 26. Magnitude and phase responses for the impedance of a 1 mH floating inductance simulated using the circuit in Figure 14.

with a symmetrical dc power supply voltages $V_{DD} = -V_{SS} = 1.5\,\text{V}$ in the TSMC 0.25-μm CMOS process provided by MOSIS. The long tail pair based CCII+ realization in [17], the floating current source (FCS) based CCII−realization in [18], the dual-X CCII realization in [13], and the DVCC realization in [10], shown in Figures 17–20, respectively, are used in the simulations. The balanced output CCII realization used in the simulations is obtained by adding an extra cross-coupled stage to the long tail pair based CCII+ realization, so that to provide inverting current at the negative Z-terminal ($Z-$), as shown in Figure 21. For the CCII+ and the balanced output CCII, the bias voltages V_B and V_C are -0.7 and $-0.72\,\text{V}$, respectively. The CCII− is biased using a biasing current $2I_B = 100\,\mu\text{A}$, and compensated using a capacitor $C_1 = 1\,\text{pF}$ connected between the gate of M_7 and the drain of M_{10}. The bias voltage V_{bias} for the dual-X CCII is 0.56 V. The DVCC bias voltages V_{b1} and V_{b2} are -0.52 and 0.32 V, respectively. The dimensions of the MOS transistors in the CCII+, CCII−, Balanced output CCII, dual-X CCII, and DVCC structures are given in Tables I–V, respectively. Level-49 MOS model parameters used for simulations are given in [19].

Detailed analysis for the simulation results of inductance simulator circuits using their NAM representations has been given in [8]. However, our interest in the forecoming simulations will be confined to examine and demonstrate the functionality and operation of the novel synthesized circuits.

DOI: 10.1002/cta

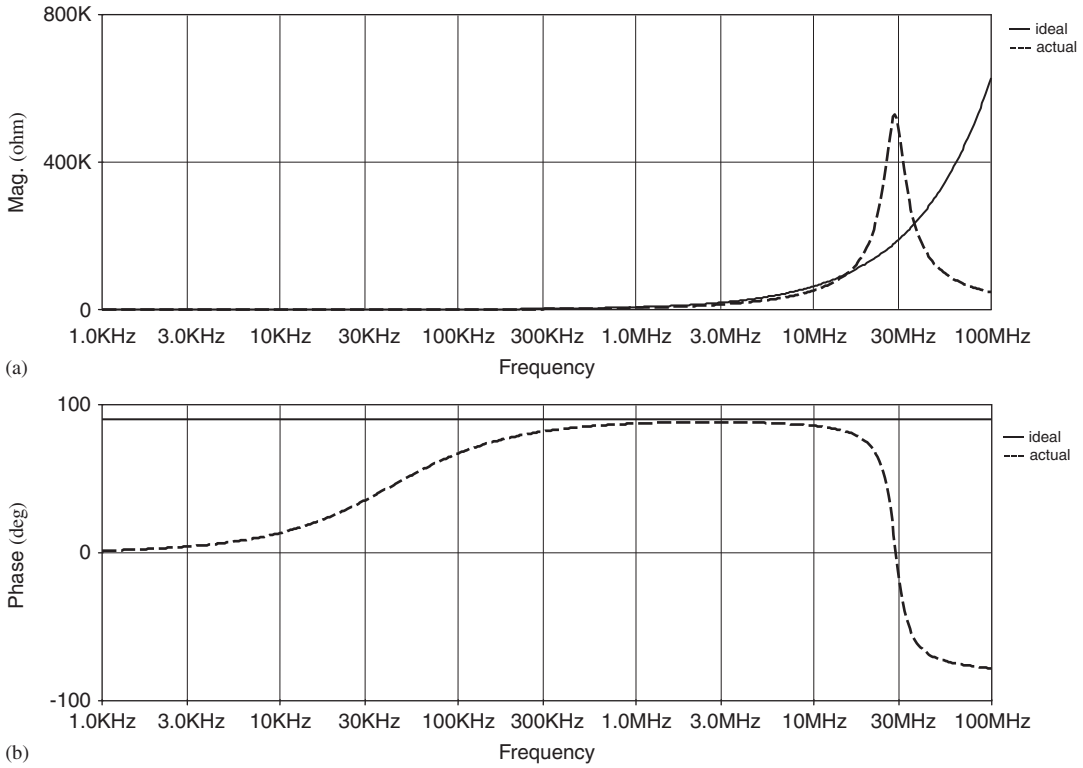

Figure 27. Magnitude and phase responses for the impedance of a 1 mH floating inductance simulated using the circuit in Figure 15.

The circuit in Figure 7(b) is used to simulate a floating coil with $L = 1\,\text{mH}$. The passive elements are selected such that $R_1 = 1/Y_1 = 1\,\text{k}\Omega$, $R_2 = 1/Y_2 = 10\,\text{k}\Omega$, and Y_3 is a capacitance $C = 100\,\text{pF}$. The magnitude and phase responses for the impedance of this simulated floating coil compared with those of an ideal one are depicted in Figure 22.

For the circuits in Figure 11(a) and (b), the passive elements are selected such that $C = 100\,\text{pF}$ and $R_2 = 1/G_2 = 1\,\text{k}\Omega$. The dimensions of the NMOS transistor M_1 are $W/L = 2\,\mu\text{m}/0.5\,\mu\text{m}$. The bias voltage V_G is selected to be 0.78 V so that to realize a resistance $20\,\text{k}\Omega$ across M_1. The simulated inductance to be realized is 1 mH. Note that the higher resistance value is realized using the triode MOS transistor M_1 rather than R_2 so that to avoid the need to implement a high value on-chip floating resistance. The magnitude and phase responses for the impedances of the simulated coils in Figure 11(a) and (b) compared with those of ideal 1 mH inductances are depicted in Figures 23 and 24, respectively. Simulation results show that the bandwidth for the circuit in Figure 11(a) is slightly wider than that of the circuit in Figure 11(b). But this comes at the expense of using more active elements, as explained in the previous section.

For the resistorless floating coil simulator circuit in Figure 12, the dimensions of the NMOS transistors M_1, M_2, and M_3 are $W/L = 2\,\mu\text{m}/0.5\,\mu\text{m}$. The bias voltages V_{G1} and V_{G2} are selected to be 0.78 V so that to obtain a resistance $20\,\text{k}\Omega$ across each one of the triode MOS transistor. Thus,

DOI: 10.1002/cta

the capacitance C is set to 10 pF so that to realize a floating inductance of 1 mH. The magnitude and phase responses for the impedance of the resistorless simulated inductance in Figure 12 compared with those of an ideal 1 mH inductance are given in Figure 25.

To simulate a floating coil using the circuit in Figure 14, the passive elements are selected such that $R_1 = 1/Y_1 = 1\,\text{k}\Omega$, $R_2 = 1/Y_2 = 10\,\text{k}\Omega$, and Y_3 is a capacitance $C = 100\,\text{pF}$. The magnitude and phase responses for the impedance of the resulting simulated floating inductor compared with those of an ideal 1 mH inductance are depicted in Figure 26.

For the novel simulator circuit in Figure 15, the passive elements are selected such that $R_2 = 1/Y_2 = 1\,\text{K}\Omega$, while Y_3 is a capacitance $C = 100\,\text{pF}$. The dimensions of the NMOS transistor M_1 are $W/L = 2\,\mu\text{m}/0.5\,\mu\text{m}$. The bias voltage V_G is selected to be 1 V so that to realize a resistance $10\,\text{K}\Omega$ across M_1. The magnitude and phase responses for the impedances of the resulting 1 mH simulated inductance compared with those of an ideal 1 mH inductance are depicted in Figure 27.

To realize a floating coil using the circuit in Figure 16, the passive elements are selected such that $R_1 = 1/Y_1 = 1\,\text{K}\Omega$, $R_2 = 1/Y_2 = 10\,\text{K}\Omega$, and Y_3 is a capacitance $C = 100\,\text{pF}$. The magnitude and phase responses for the impedance of the resulting simulated floating inductor compared with those of an ideal 1 mH coil are depicted in Figure 28.

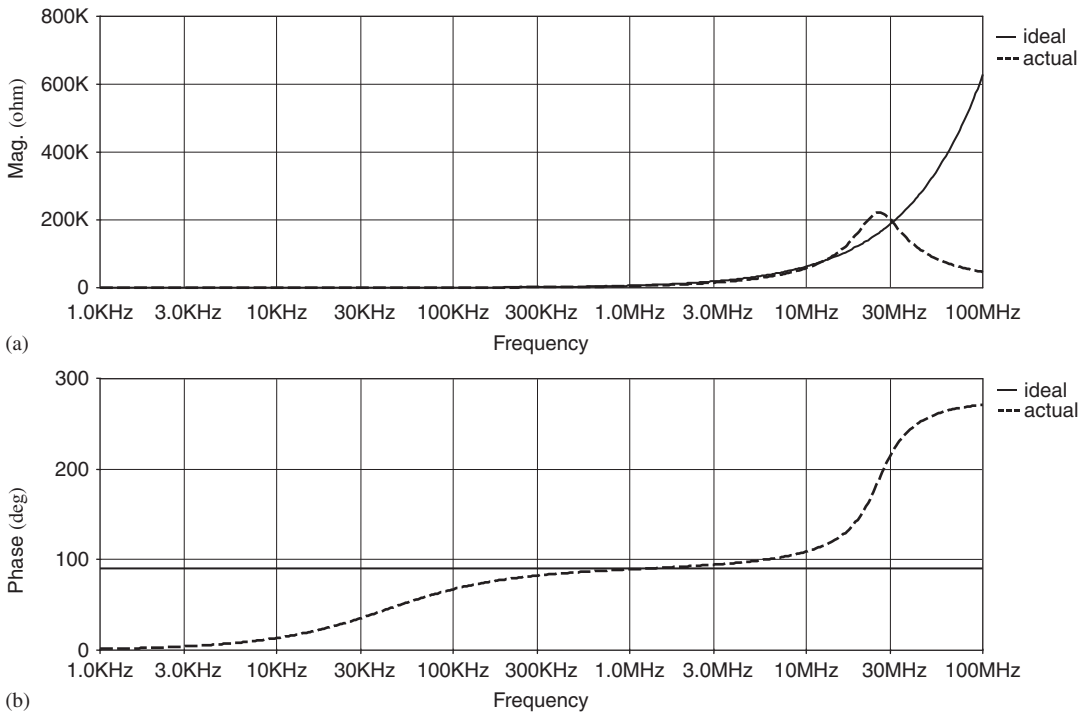

Figure 28. Magnitude and phase responses for the impedance of a 1 mH floating inductance simulated using the circuit in Figure 16.

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6. CONCLUSION

In this paper, the systematic synthesis of CCII-based wide-band floating simulators, using the generalized framework for linear active circuits has been studied. The resulting synthesized floating simulators include circuits that have been reported earlier in the literature in addition to novel floating simulators, using various types of CCII. According to the passive elements used in the realizations, these circuits can be used to simulate floating coils, FDNRs, capacitance multipliers… etc. The merits and drawbacks of the synthesized circuits vary according to the design tradeoffs, including the number of active devices, number and values of floating and grounded passive elements, matching requirements, and tunability. Many other floating inductance circuits [20] that are available in the literature can also be realized using the proposed generation method and are not included to limit the paper length. SPICE simulations have been presented to verify the performance of the new circuits obtained using the systematic synthesis framework, when used to simulate floating inductances. Simulation results indicate that high-performance novel wide-band CCII-based simulated floating coils have been synthesized systematically using the generalized framework. Thus, the potentials of the generalized systematic synthesis framework in synthesizing high-performance novel circuits have been demonstrated through this study.

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DOI: 10.1002/cta